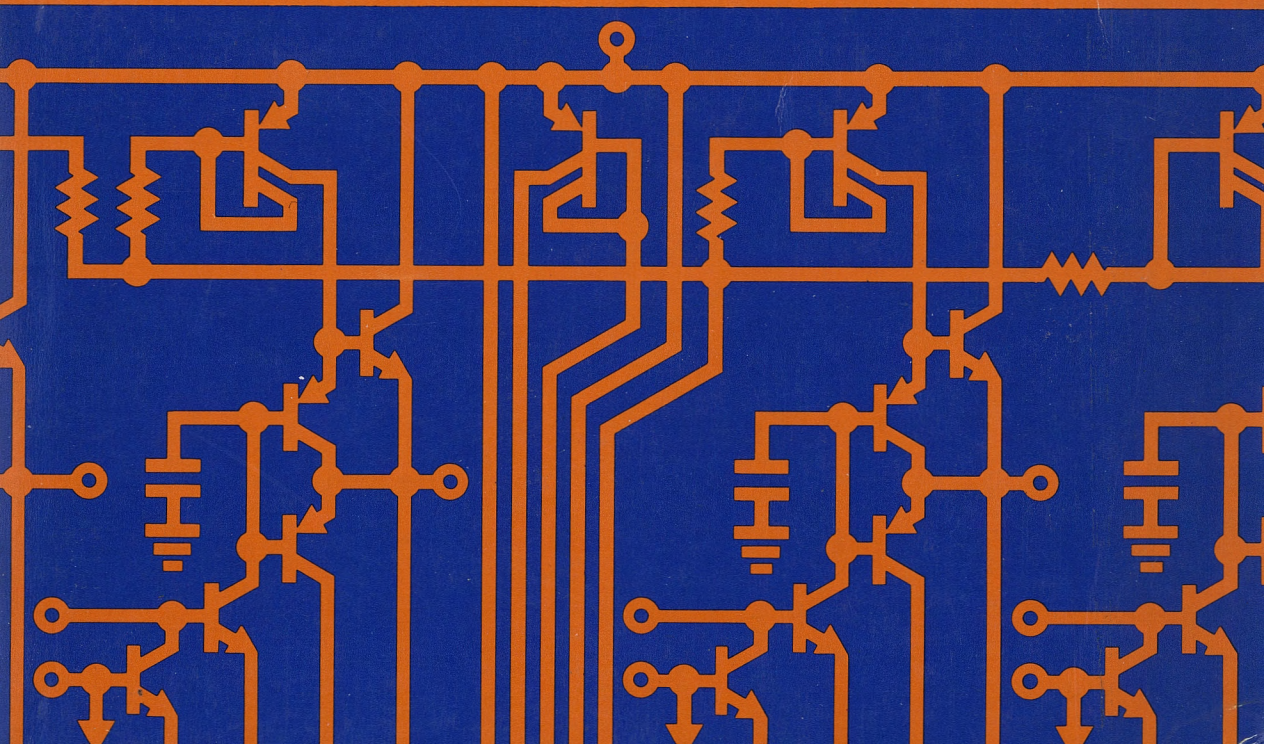
# LINEAR APPLICATIONS

## Volume 2

National



# LINEAR APPLICATIONS Volume 2

# National

**PREFACE** The second volume of National's Linear Applications handbook picks up where Volume I left off. Data sheets, application briefs and pertinent articles published in the 3 years since Volume I was printed are included in this handbook. Volume II retains the same format as Volume I, to facilitate its use.

In this volume, as in Volume I, application schematics call out the generic family, which, by coincidence, is the military temperature range version of the device. Generally, any device in the generic family will work in the circuit. For example, an amplifier marked LM108 refers to the generic 108 family, and does not imply that only military-grade devices will work. Military (or industrial) grade devices need only be considered when their tighter electrical limits or wider temperature range warrant their use. As a reminder to our users, our numbering system is:

| Device No. | Grade | Specified Temperature Range |
|---|---|---|
| LM1XX | Military | $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ |
| LM2XX | Industrial | $-25^{\circ}C \leq T_A \leq +85^{\circ}C$ |
| LM3XX | Commercial | $0^{\circ}C \leq T_A \leq +70^{\circ}C$ |

Because commercial parts are less expensive than military or industrial, these points should be kept in mind when trying to determine the most cost-effective approach to a given design.

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# APPLICATION LITERATURE NUMERICAL LIST

## APPLICATION NOTES



## LINEAR BRIEFS



## APPENDICES

# DEVICE/APPLICATION LITERATURE CROSS-REFERENCE

| DEVICE NUMBER | APPLICATION LITERATURE |
|---|---|
| LH0033 | AN-115 |
| LM101 | AN-132, LB-28 |
| LM104 | AN-110 |
| LM105 | AN-110 |
| LM108 | AN-79, AN-88, AN-110, AN-161, LB-24, LB-28 |
| LM111 | AN-103, LB-32 |
| LM113 | LB-21, LB-23, LB-28 |
| LM114 | LB-21, LB-25 |
| LM216 | AN-132 |
| LM118 | AN-110, AN-115, AN-129, LB-21, LB-23 |
| LM119 | AN-115, LB-23 |
| LM120 | AN-103, AN-115, Appendix III |
| LM121 | AN-79, LB-24, LB-32 |
| LM122 | AN-97 |
| LM124 | AN-88, AN-129 |
| LM125 | AN-82 |
| LM126 | AN-82 |
| LM127 | AN-82 |
| LM140 | AN-103, AN-115 |
| LM143 | AN-103, AN-127 |
| LM158 | AN-116 |
| LM160 | AN-87 |
| LM161 | AN-87 |
| LM195 | AN-110, AN-129, AN-153, AN-161, LB-28 |
| LM199 | AN-161, LB-31 |

| DEVICE NUMBER | APPLICATION LITERATURE |
|---|---|
| LM377 | AN-125 |
| LM378 | AN-125, AN-147 |
| LM379 | AN-125 |
| LM380 | AN-146 |
| LM382 | AN-147 |
| LM386 | LB-29 |
| LM555 | LB-30 |
| LM565 | AN-146 |
| LM566 | AN-146 |
| LM1310 | AN-81 |
| LM1558 | AN-103, AN-116 |
| LM1800 | AN-81, AN-147 |
| LM1820 | AN-147, LB-29 |
| LM1900 | LB-33 |
| LM2907 | AN-162 |
| LM2917 | AN-162 |
| LM3089 | AN-147 |
| LM3909 | AN-154 |
| LM3911 | AN-132, LB-30 |
| LM4250 | AN-88, LB-34 |
| LM78LXX | AN-146 |
| LX5600 | AN-132, LB-27, LB-30 |
| LX5700 | AN-132, LB-27, LB-30 |
| NSL4944 | AN-153 |
| MM74C04 | AN-88 |

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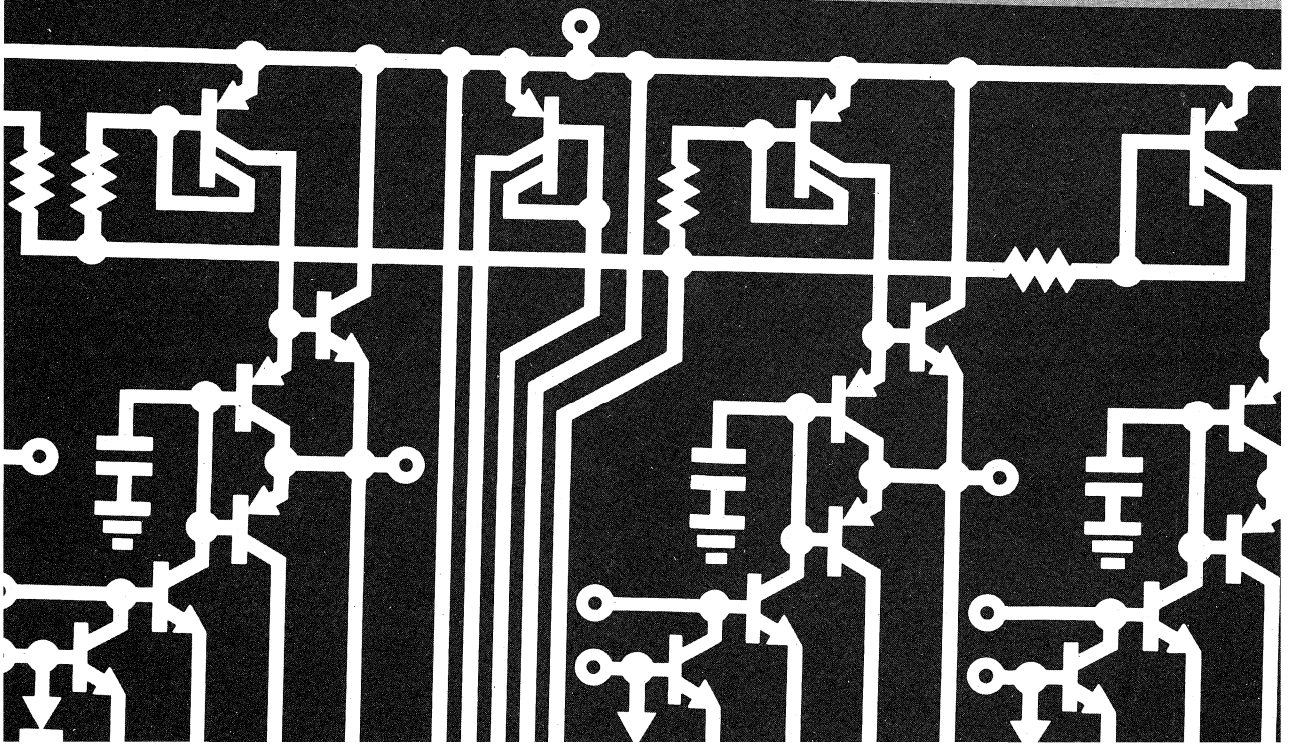
# APPLICATION NOTES



Robert C. Dobkin
FEBRUARY 1973

# IC PREAMP CHALLENGES CHOPPERS ON DRIFT

Since the introduction of monolithic IC amplifiers there has been a continual improvement in DC accuracy. Bias currents have been decreased by 5 orders of magnitude over the past 5 years. Low offset voltage drift is also necessary in a high accuracy circuits. This is evidenced by the popularity of low drift amplifier types as well as the requests for selected low-drift op amps. However, until now the chopper stabilized amplifier offered the lowest drift. A new monolithic IC preamplifier designed for use with general purpose op amps improves DC accuracy to where the drift is lower than many chopper stabilized amplifiers.

## INTRODUCTION

Chopper amplifiers have long been known to offer the lowest possible DC drift. They are not without problems, however. Most chopper amps can be used only as inverting amplifiers, limiting their applications. Chopping can introduce noise and spikes into the signal. Mechanical choppers need replacement as well as being shock sensitive. Further, chopper amplifiers are designed to operate over a limited power supply, limited temperature range.

Previous low-drift op amps do not provide optimum performance either. Selected devices may only meet their specified voltage drift under restrictive conditions. For example, if a 741 device is selected without offset nulling, the addition of a offset null pot can drastically change the drift. Low drift op amps designed for offset balancing have another problem. The resistor network used in the null circuit is designed to null the drift when the offset voltage is nulled. The mechanism to achieve nulled drift depends on the difference in temperature coefficient between the internal resistors and the external null pot. Since the internal resistors have a non-linear temperature coefficient and may vary device to device as well as between manufacturers, it can only approximately null offset drift. The problem gets worse if the external null pot has a TC other than zero.

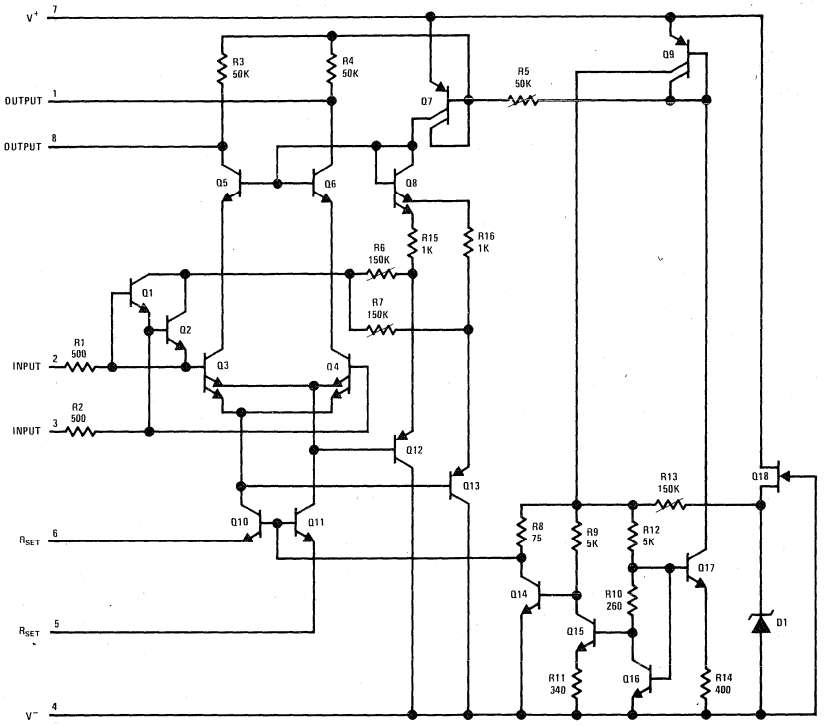
A new IC preamplifier is now available which can give drifts as low as $0.2\mu V/^{\circ}C$. It is used with conventional op amps and eliminates the problems associated with older devices. As well as improving the DC input characteristics of the op amp, loop-gain is increased when an LM121 is used. This further improves overall accuracy since DC gain error is decreased.

The LM121 preamp is designed to give zero drift when the offset voltage is nulled to zero. The operating current of the LM121 is programmable by the value of the null network resistors. The drift is independent of the value of the nulling network so it can be used over a wide range of operating currents while retaining low drift. The operating current can be chosen to optimize bias current, gain, speed, or noise while still retaining the low drift. Further, since the drift is independent of the match between external and internal resistors when the offset is nulled, lower and more predictable drifts can be expected in actual use. The input is fully differential, overcoming many of the problems with single ended chopper-amps. The device also has enough common mode rejection ratio to allow the low drift to be fully utilized.

## CIRCUIT DESCRIPTION

The LM121 is a well matched differential amplifier utilizing super-gain transistors as the input devices. A schematic is shown in Figure 1. The input signal is applied to the bases of $Q_3$ and $Q_4$ through protection resistors $R_1$ and $R_2$. $Q_3$ and $Q_4$ have two emitters to allow offset balancing which will be explained later. The operating current for the differential amplifier is supplied by current sources $Q_{10}$ and $Q_{11}$. The operating current is externally programmed by resistors connected from the emitters of $Q_{10}$ and $Q_{11}$ to the negative supply. Input transistors $Q_3$ and $Q_4$ are cascoded by transistors $Q_5$ and $Q_6$ to keep the collector base voltage on the input stage equal to zero. This eliminates leakage at high operating temperatures and keeps the common mode input voltage from appearing across the low breakdown super-gain input transistors. Additionally, the cascode improves the common mode rejection of the differential amplifier. $Q_1$ and $Q_2$ protect the input against large differential voltages.

The output signal is developed across resistive loads $R_3$ and $R_4$. The total collector current of the input is then applied to the base of a fixed gain PNP, $Q_7$. The collector current of $Q_7$ sets the operating current of $Q_8$, $Q_{12}$, and $Q_{13}$. These transistors are used to set the operating voltage of the cascode, $Q_5$ and $Q_6$. By operating the cascode biasing transistors at the same operating current as the input stage, it is possible to keep collector base voltage at zero; and therefore, collector-base leakage remains low over a wide current range. Further, this minimizes the effects of $V_{BE}$ variations and finite transistor current gain. At high operating currents the collector base voltage of the input stage is increased by about 100 mV due to the drop across $R_{15}$ and $R_{16}$. This prevents the input transistors from saturating under worst case conditions of high current and high operating temperature.




*PIN CONNECTIONS SHOWN ON DIAGRAM AND TYPICAL APPLICATIONS ARE FOR TO-5 PACKAGE.

**FIGURE 1. Schematic Diagram of the LM121**

The rest of the devices comprise the turn-on and regulator circuitry. Transistors $Q_{14}$, $Q_{15}$, and $Q_{16}$ form a 1.2V regulator for the bases of the input stage current source. By fixing the bases of the current sources at 1.2V, their output current changes proportional to absolute temperature. This compensates for the temperature sensitivity of the input stage transconductance. Temperature compensating the transconductance makes the preamp more useful in some applications such as an instrumentation amplifier and minimizes bandwidth variations with temperature. The regulator is started by $Q_{18}$ and its operating current is supplied by $Q_{17}$ and $Q_9$, Figure 2 shows the LM121 chip.

### Offset Balancing

The LM121 was designed to operate with an offset balancing network connected to the current source transistors. The method of balancing the offset also minimizes the drift of the preamp. Unlike earlier devices such as the LM725, the LM121 depends only upon the highly predictable emitter base voltages of transistors to achieve low drift. Devices like the LM725 depend on the match between internal resistor temperature coefficient and the external null pot as well as the input stage transistors characteristics for drift compensation.

The input stage of the LM121 is actually two differential amplifiers connected in parallel, each having a fixed offset. The offset is due to different

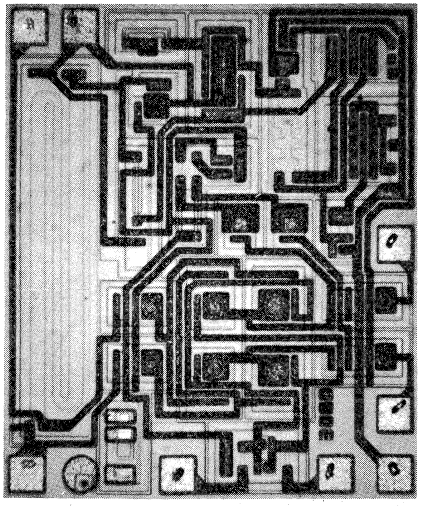


**FIGURE 2. LM121 Chip**

areas for the transistor emitters. The offset for each pair is given by:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{A_1}{A_2}$$

where k is Boltzmann's constant T is absolute temperature, q is the charge on an electron, and $A_1$ and $A_2$ are emitter areas. Because of the offset, each pair has a fixed drift. When the pairs are connected in parallel, if they match, the offsets and drift cancel. However, since matching is not perfect, the emitters of the pairs are not connected in parallel, but connected to independent current sources to allow offset balancing. The offset and drift effect of each pair is proportional to its operating current, so varying the ratio of the current from current sources will vary both the offset and drift. When the offset is nulled to zero, the drift is nulled to below $1\mu V/^{\circ}C$.

The offset balancing method used in the LM121 has several advantages over conventional balancing schemes. Firstly, as mentioned earlier, it theoretically zeros the drift and offset simultaneously. Secondly, since the maximum balancing range is fixed by transistor areas, the effect of null network variations on offset voltage is minimized. Resistor shifts of one percent only cause a $30\mu V$ shift in offset voltage on the LM121, while a one percent shift in collector resistors on a standard diff amp causes a $300\mu V$ offset change. Finally, it allows the value of the null network to set the operating current.

**Achieving Low Drift**

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted. In many cases, the low drift of the op amp is completely swamped by external effects while the amplifier is blamed for the high drift.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Whenever dissimilar metals are joined, a thermocouple results. The voltage generated by the thermocouple is proportional to the temperature difference between the junction and the measurement end of the metal. This voltage can range between essentially zero and hundred of microvolts per degree, depending on the metals used. In any system using integrated circuits a minimum of three metals are found: copper, solder, and kovar (lead material of the IC).

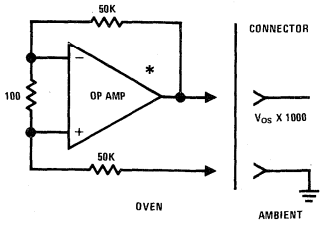
Nominally, most parts of a circuit are at the same temperature. However, a small temperature gradient can exist across even a few inches — and this is a big problem with low level signals. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally are the package-to printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

For example, a very low drift amplifier was constructed and the output monitored over a 1 minute period. During the 1 minute it appeared to have input referred offset variations of $\pm 5\mu V$. Shielding the circuit from air currents reduced this to $\pm 0.5\mu V$. The $10\mu V$ error was due to thermal gradients across the circuit from air currents.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evenohm or managanin are best since they only generate about $2\mu V/^{\circ}C$ referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example a gain of 1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a $50\mu V$ error. Most precision resistors use different material for different ranges of resistor values. It is not unexpected that resistors differing by a factor of 1000, do not track perfectly with temperature. For best results insure that the gain fixing resistors are of the same material or have tracking temperature coefficients.

Testing low drift amplifiers is also difficult. Standard drift testing techniques such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method — do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signals through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal. The circuit in Figure 3 will yield good results if well constructed.




*OP AMP SHOWN IN FIGURE 9.

**FIGURE 3. Drift Measurement Circuit**

## Performance

It is somewhat difficult to specify the performance of the LM121 since it is programmable over a wide range of operating currents. Changing the operating current varies gain, bias current, and offset current – three critical parameters in a high accuracy system. However, offset voltage and drift are virtually independent of the operating current.

Typical performance at an operating current of 20μA is shown in Table I. Figures 4 and 5 show how the bias current, offset current, and gain change as a function of programming current. Drift is guaranteed at 1μV/°C independent of the operating current.

**TABLE I. Typical Performance at an Operating Current of 10μA Per Side**

| | |
|---|---|
| Offset Voltage | Nulled |
| Bias Current | 7 nA |
| Offset Current | 0.5 nA |
| Offset Voltage Drift | 0.3μV/°C |
| Common Mode Rejection Ratio | 125 dB |
| Supply Voltage Rejection Ratio | 125 dB |
| Common Mode Range | ±13V |
| Gain | 20V/V |
| Supply Current | 0.5 mA |

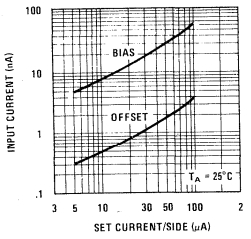



**FIGURE 4. Bias and Offset Current vs Set Current**

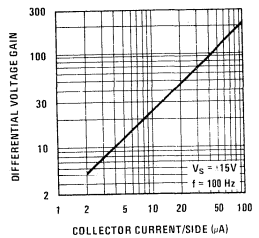



**FIGURE 5. Gain vs Set Current**

Over a temperature range of −55°C to +125°C the LM121 has less than 1μV/°C offset voltage drift when nulled. It is important that the offset voltage is accurately nulled to achieve this low drift. The drift is directly related to the offset voltage with 3.8μV/°C drift resulting from every millivolt of offset. For example, if the offset is nulled to 100μV, about 0.4μV/°C will result – or twice the typically expected drift. This drift is quite predictable and could even be used to cancel the drift elsewhere in a system. Figure 6 shows drift as a function of offset voltage. For critical applications selected devices can achieve 0.2μV/°C.

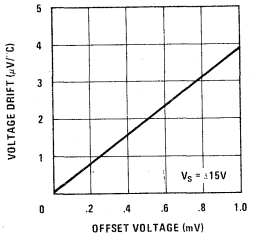



**FIGURE 6. Drift vs Offset Voltage**

Figures 7 and 8 show the bias current, offset current, and gain variation over a −55°C to +125°C temperature range. These performance characteristics do not tell the whole story. Since the LM121

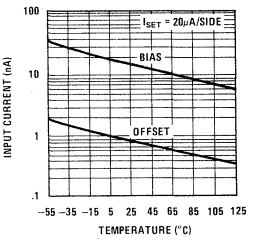



**FIGURE 7. Bias and Offset Current vs Temperature**

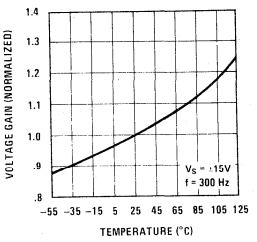



**FIGURE 8. Gain vs Temperature for the LM121**

is used with an operational amplifier, the op amp characteristics must be considered for over-all amplifier performance.

## Op Amp Effects

The LM121 is nominally used with a standard type of operational amplifier. The op amp functions as the second and ensuing stages of the amplifying system. When the LM121 is connected to an op amp, the two devices may be treated (and used) just as a single op amp. The inputs of the combination are the inputs of the LM121 and the output is from the op amp. Feedback, as with any op amp, is applied back to the inputs. Figure 9 shows the general configuration of an amplifier using the LM121.

The offset voltage and drift of the op amp used have an effect on overall performance and must be considered. (The bias and offset currents of today's op amp are low enough to be ignored.) Although the exact effects of the op amp stage are difficult and tedious to calculate, a few approximations will show the sources of drift.

Op amp drift is perhaps the most important source of error. Drift of the op amp is directly reduced by the gain of the LM121. The drift referred to the input is given by:

$$\text{input drift} = \frac{\text{op amp drift}}{\text{LM121 gain}} + \text{LM121 drift.}$$

If the op amp has a drift of 10$\mu$V/°C and the LM121 is operated at a gain of $A_V$ = 50, there will be a 0.2$\mu$V/°C component of the total drift due to the op amp. It is therefore important that the LM121 be operated at relatively high gain to minimize the effects of op amp drift. Lower gains for the LM121 will give proportionately less reduction in op amp drift. Of course, a moderately low drift op amp such as the LM108A eases the problem.

Op amp offset voltage also has an effect on total drift. For purpose of analysis assume the LM121 to be perfect with no offset or drift of its own. Then any offset seen when the LM121 is connected to an op amp is due to the op amp alone. The offset is equal to:

$$\text{offset voltage} = \frac{\text{op amp offset}}{\text{LM121 gain}}$$

or the offset is reduced by the gain of the LM121. For example, with a gain of 50 for the LM121, 2 mV of offset on the op amp appears as 40$\mu$V of offset at the LM121 input. Unlike offset due to a mismatch in the LM121, this 40$\mu$V of offset does not cause any drift. However, when the system is nulled so the offset at the input of the LM121 is zero, 40$\mu$V of imbalance has been inserted into the LM121. The imbalance caused by nulling the offset induced by the op amp will cause a drift of about 0.14$\mu$V/°C. With the system nulled the drift due to op amp will cause a drift of about 0.15$\mu$V/°C. With the system nulled the drift due to op amp offset can be expressed as:

$$\text{drift } (\mu\text{V/°C}) = \frac{\text{op amp offset (mV)}}{\text{LM121 gain}} (3.6\mu\text{V/°C}).$$

In actual operation, drift due to op amp offsets will usually be better than predicted. This is because offset voltage and drift are not independent. With the LM121 there is a strong, predictable, correlation between offset and drift. Also, there is a correlation with op amps, but it is not as strong. The drift of the op amp tends to cancel the drift induced in the LM121 when the system is nulled.

In the previous example the drift due to the op amp offset was 0.15$\mu$V/°C. If the op amp has a drift of 3.6$\mu$V/°C per millivolt of offset (like the LM121) it will have a drift of 7.2$\mu$V/°C. This drift is reduced by the gain of the LM121 ($A_V$ = 50) to 0.14$\mu$V/°C. This 0.14$\mu$V/°C will cancel the 0.14$\mu$V/°C drift due to balancing the LM121. Since op amps do not always have a strong correlation between offset and drift, the cancellation of drifts is not total. Once again, high gain for the LM121 and a low offset op amp helps achieve low drifts.

## Frequency Compensation

The additional gain of the LM121 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. This is because the additional gain introduced by the LM121 must be rolled-off before the phase shift through the LM121 and op amp reaches 180°. The additional compensation depends on the gain of the LM121 as well as the closed loop gain of the system. Two frequency compensation techniques are shown here that will operate with any op amp that is unity gain stable.

When the closed loop gain of the op amp with the LM121 is less than the gain of the LM121 alone, more compensation is needed. The worst case situation is when there is 100% feedback – such as a voltage follower or integrator – and the gain of the LM121 is high. When high closed loop gains are used – for example $A_V$ = 1000 – and only an additional gain of 100 is inserted by the LM121, the frequency compensation of the op amp will usually suffice.

The basic circuit of the LM121 in Figure 9 shows two compensation capacitors connected to the op amp (disregarding the 30 pF frequency compensation for the op amp alone). The capacitor from pin

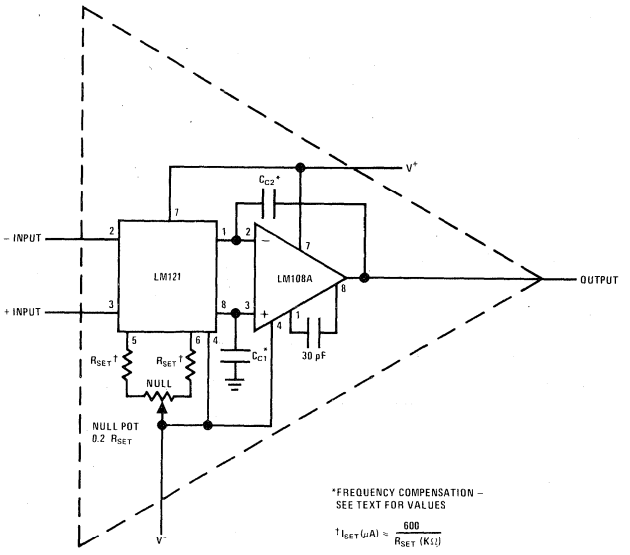



**FIGURE 9. General Purpose Amplifier Using the LM121**

6 to pin 2 around the op amp acts as an integrating capacitor to roll off the gain. Since the output of the LM121 is differential, a second capacitor is needed to roll off pin 3 of the op amp. These capacitors are $C_{C1}$ and $C_{C2}$ in Figure 9.

With capacitors equal, the circuit retains good AC power supply rejection. The approximate value of the compensation capacitors is given by:

$$C_C = \frac{8}{10^6 \, A_{CL} \, R_{SET}} \text{ farads}$$

where $R_{SET}$ is the current set resistor from each current source and where $A_{CL}$ is closed loop gain. Table II shows typical capacitor values.

An alternate compensation scheme was developed for applications requiring more predictable and smoother roll off. This is useful where the amplifier's gain is changed over a wide range. In this case $C_{C1}$ is made large and connected to $V^+$ rather than ground. The output of the LM121 is rendered single ended by a 0.01$\mu$F bypass capacitor to $V^+$. Overall frequency compensation then is achieved by an integrating capacitor around the op amp:

$$\text{Bandwidth at unity gain} \cong \frac{12}{2\pi \, R_{SET} \, C}$$

$$\text{for 0.5 MHz bandwidth } C = \frac{4}{10^6 \, R_{SET}}$$

**TABLE II. Typical compensation capacitors for various operating currents and closed loop gains. Values given apply to LM101A, LM108, and LM741 type amplifiers.**

| CLOSED LOOP GAIN | CURRENT SET RESISTOR | | | | |
|---|---|---|---|---|---|
| | 120 kΩ | 60 kΩ | 30 kΩ | 12 kΩ | 6 kΩ |
| $A_V = 1$ | 68 pF | 130 pF | 270 pF | 680 pF | 1300 pF |
| $A_V = 5$ | 15 pF | 27 pF | 50 pF | 130 pF | 270 pF |
| $A_V = 10$ | 10 pF | 15 pF | 27 pF | 68 pF | 130 pF |
| $A_V = 50$ | 1 pF | 3 pF | 5 pF | 15 pF | 27 pF |
| $A_V = 100$ | | 1 pF | 3 pF | 5 pF | 10 pF |
| $A_V = 500$ | | | 1 pF | 1 pF | 3 pF |
| $A_V = 1000$ | | | | | |

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz. If closed loop gain is greater than unity "C" may be decreased to:

$$C = \frac{4}{10^6 A_{CL} R_{SET}}$$

**Applications**

No attempt will be made to include precision op amp applications as they are well covered in other literature. The previous sections detail frequency compensation and drift problems encountered in using very low drift op amps. The circuit shown in Figure 9 will yield good results in almost any op amp application. However, it is important to choose the operating current properly. From the curves given it is relatively easy to see the effects of current changes. High currents increase gain and reduce op amp effects on drift. Bias and offset current also increase at high current. When the operating source resistance is relatively high, errors due to high bias and offset current can swamp offset voltage drift errors. Therefore, with high source impedances it may be advantageous to operate at lower currents.

Another important consideration is output common mode voltage. This is the voltage between the outputs of the LM121 and the positive power supply. Firstly, the output common mode voltage must be within the operating common mode range of the output op amp. At currents above 10μA there is no problems with the LM108, LM101, and LM741 type devices. Higher currents are needed for devices with more limited common mode range, such as the LM118. As the operating current is increased, the positive common mode limit for the LM121 is decreased. This is because there is more voltage drop across the internal 50k load resistors. The output common mode voltage and positive common mode limits are about equal and given by:

$$\text{Output common mode voltage positive common mode limit} \approx V^+ - 0.6V^+ \frac{0.65 \times 50k\Omega}{R_{SET}}$$

If it is necessary to increase the common mode output voltage (or limit), external resistors can be connected in parallel with the internal 50kΩ resistors. This should only be done at high operating currents (80μA) since it reduces gain and diverts part of the input stage current from the internal biasing circuitry. A reasonable value for external resistors is 50kΩ.

The external resistors should be of high quality and low drift, such as wirewound resistors, since they will affect drift if they do not track well with temperature. A 20ppm/°C difference in external resistor temperature coefficient will introduce an additional 0.3μV/°C drift.

An unusually simple gain of 1000 instrumentation amplifier can be made using the LM121. The amplifier has a floating, full differential, high impedance input. Linearity is better than 1%, depending upon input signal level with maximum error at maximum input. Gain stability, as shown in Figure 10, is about ±2% over a −55°C to +125°C temperature range. Finally, the amplifier has very low drift and high CMRR.

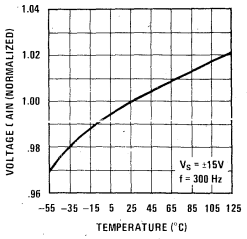



**FIGURE 10. Instrumentation Amplifier Gain vs Temperature**

Figure 11 shows a schematic of the instrumentation amplifier. The LM121 is used as the input stage and operated open-loop. It converts an input voltage to a differential output current at pins 1 and 8 to drive an op amp. The op amp acts as a current to voltage converter and has a single-ended output.

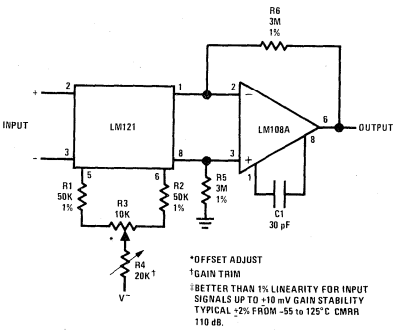



**FIGURE 11. Gain of 1000 Instrumentation Amplifier**

Resistors $R_1$ and $R_2$ with null pot $R_3$ set the operating current of the LM121 and provide offset adjustment. $R_4$ is a fine trim to set the gain at 1000. There is very little interaction between the gain and null pots.

This instrumentation amplifier is limited to a maximum input signal of ±10 mV for good linearity. At high signal levels the transfer characteristic of the LM121 become rapidly non-linear, as with any differential amplifier. Therefore, it is most useful as a high gain amplifier.

Since feedback is not applied around the LM121, CMRR is not dependent on resistor matching. This eliminates the need for precisely matched resistor as with conventional instrumentation amplifiers. Although the linearity and gain stability are not as good as conventional schemes, this amplifier will find wide application where low drift and high CMRR are necessary.

A precision reference using a standard cell is shown in Figure 12. The low drift and low input current of the LM121A allow the reference amplifier to buffer the standard cell with high accuracy. Typical long term drift for the LM121 operating at constant temperature is less than 2$\mu$V per 1000 hours.

To minimize temperature gradient errors, this circuit should be shielded from air currents. Good single-point wiring should also be used. When power is not applied, it is necessary to disconnect the standard cell from the input of the LM121 or it will discharge through the internal protection diodes.

## CONCLUSIONS

A new preamplifier for operational amplifiers has been described. It can achieve voltage drifts as low as many chopper amplifiers without the problems associated with chopping. Operating current is programmable over a wide range so the input characteristics can be optimized for the particular application. Further, using a preamp and a conventional op amp allows more flexibility than a single low-drift op amp.

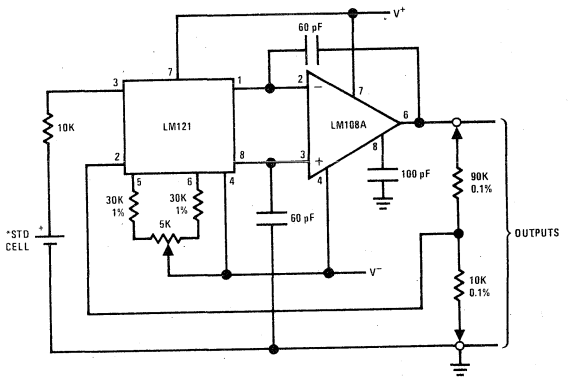



FIGURE 12. 10V Reference

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JUNE 1973

# LM1800 (LM1310, LM1310E*) PHASE LOCKED LOOP FM STEREO DEMODULATOR

## INTRODUCTION

The LM1800 is a phase locked loop FM stereo demodulator built on a single monolithic die. In addition to separating left (L) and right (R) signal information from the detected IF output, the LM1800 features automatic stereo/monaural switching, 45 dB power supply rejection, and a 100 mA stereo indicator lamp driver. Particularly attractive is the low external part count and total elimination of coils. A single inexpensive potentiometer performs all tuning. The resulting FM stereo system delivers high fidelity sound while still meeting the cost requirements of inexpensive stereo receivers.

Figures 1 and 2 outline the role played by the LM1800 in the FM stereo receiver. The frequency domain plot shows that the composite input waveform contains L+R information in the audio band and L-R information suppressed carrier modulated on 38 kHz. A 19 kHz pilot tone, locked to the 38 kHz subcarrier at the transmitter, is also included. SCA information occupies a higher band but is of no importance in the consumer FM receiver.

The block diagram of the LM1800 shows the composite input signal applied to the audio frequency amplifier, which acts as a unity gain buffer to the decoder section. A second amplified signal is capacitively coupled to two phase detectors — one in the phase locked loop and the other in the stereo switching circuitry. In the phase locked loop, the output of the 76 kHz voltage controlled oscillator (VCO) is frequency divided twice (to 38 then 19 kHz), forming the other input to the loop phase detector. The output of the loop phase detector adjusts the VCO to precisely 76 kHz. The 38 kHz output of the first frequency divider becomes the regenerated subcarrier which demodulates L-R information in the decoder section. The amplified composite and an "in phase" 19 kHz signal, generated in the phase locked loop, drive the "in phase" phase detector. When the loop is locked, the DC output voltage of this phase detector measures pilot amplitude. For pilot signals sufficiently strong to enable good stereo reception the trigger latches, applying regenerated subcarrier to the decoder and powering the stereo indicator lamp. Hysteresis, built into the trigger, protects against erratic stereo/monaural switching and the attendant lamp flicker.

In the monaural mode (electronic switch open) the decoder outputs duplicate the composite input signal except that the de-emphasis capacitors (from pins 3 and 6 to ground) roll off with the load resistors at 2 kHz. In the stereo mode (electronic switch closed), the decoder demodulates the L-R information, matrixes it with the L+R information, then delivers buffered separated L and R signals to output pins 4 and 5 respectively.

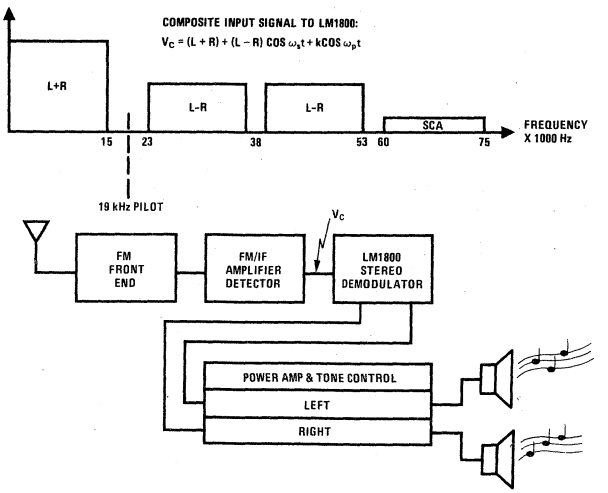



**FIGURE 1. FM Receiver Block Diagram and Frequency Spectrum of LM1800 Input Signal**

*The information contained in this application note also generally applies to LM1310, LM1310E.

## CIRCUIT DESCRIPTION

The complex circuit schematic of Figure 13 is more easily understood by reducing it to four subsections:

Regulator and Audio Amplifier
Phase Locked Loop
Stereo/Monaural Switching Circuitry
Decoder and Output Section

### Regulator and Audio Amplifier

Transmission of power supply ripple and noise has plagued users of integrated FM stereo demodulators in the past. The introduction of a voltage regulator on the chip, along with improvements in the decoder output circuitry, provides excellent supply rejection, eliminating the need for costly supply filtering. Figure 3 shows an equivalent schematic of the 5.8V regulator. $Z_2$ holds the voltage across

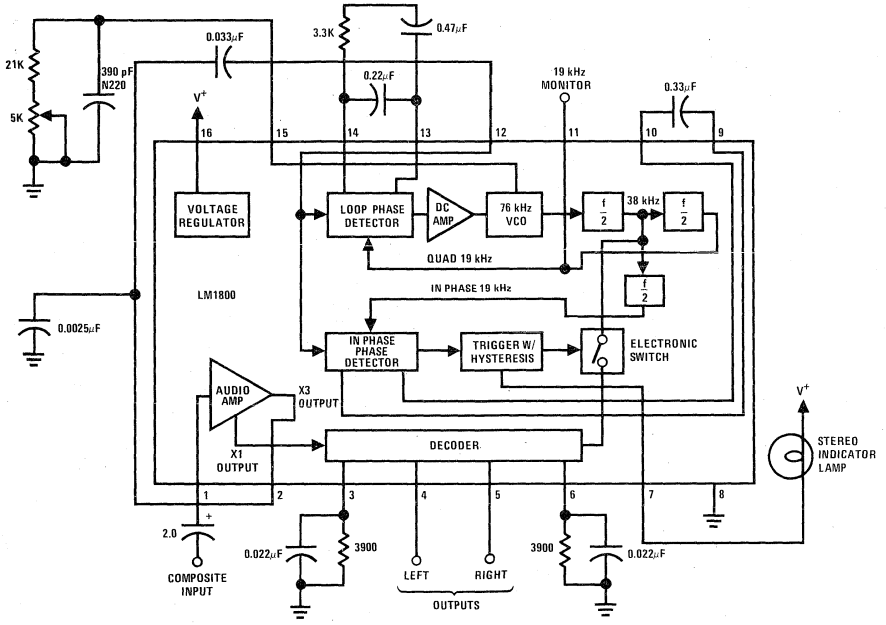



FIGURE 2. LM1800 Block Diagram

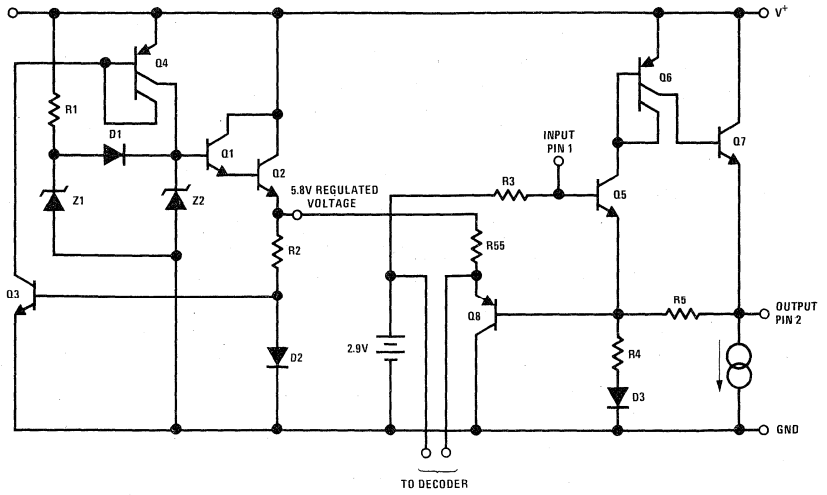



FIGURE 3. Regulator and Audio Amplifier

$R_2$ constant, thereby establishing a constant current through $D_2$, $Q_3$ and $Q_4$. The current through $Z_2$ then depends on the voltage drop across $Z_2$ and not on the supply line. $R_1$, $Z_1$ and $D_1$ assure startup after which the voltage across $D_1$ drops to zero, disconnecting $R_1$ from the remainder of the regulator circuitry.

The audio amp is biased internally by 2.9V through $R_3$ to the base of $Q_5$. Since the emitter current of $Q_5$ is much less than that of $Q_7$ and the base current of $Q_8$ is also negligible, current through $R_4$ approximately equals that through $R_5$. The DC quiescent voltage at the output pin becomes:

$$V_{P2} = V_{E5} + (V_{E5} - 0.7)\ R_5/R_4 = 5.4 \text{ volts}$$

and gain to a dynamic input is:

$$A_{\text{pin 1 - pin 2}} = 1 + R_5/R_4 = 3.0$$

A second signal path of unity gain exists through $Q_5$ and $Q_8$. The potential at $Q_8$'s emitter is also approximately 2.9V, providing conveniently biased drive to the decoder section. $R_3$ sets the input resistance at typically 45 kΩ.

### Phase Locked Loop

A phase locked loop is a feedback system comprised of a phase detector, a low pass filter, and an error amplifier in the forward transmission path while a voltage controlled oscillator provides the feedback element. Figure 4 illustrates a simplified loop. Without an input signal the error voltage drops to zero. The VCO then oscillates at some free running frequency, $f_O$. As an input signal is introduced, the phase detector compares the phase (and frequency, since frequency is the time derivative of phase) of the input signal with that of the VCO, generating an error voltage related to the frequency difference. The error signal is filtered

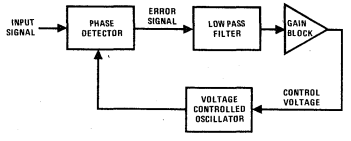



**FIGURE 4. Basic Phase Locked Loop Block Diagram**

and amplified before it is applied to the control input of the VCO. The control voltage forces the VCO frequency to move in the direction that reduces the frequency difference between the input signal and $f_O$. For free running frequencies sufficiently close to the incoming signal, the nature of loop feedback causes the VCO to synchronize to exactly the incoming frequency. Some finite phase difference exists between the two signals. This phase difference is necessary to generate the corrective error voltage for the VCO.

The LM1800 operates on precisely this principle except that the VCO free runs at approximately four times the frequency of the incoming pilot. Two frequency dividers provide a signal at the phase detector input sufficiently close in frequency to the 19 kHz pilot tone to accomplish lock. The loop provides sufficient gain to keep the phase error small, and the frequency dividers generate accurate 50% duty cycle waveforms, both necessary requirements for good stereo demodulation.

### VCO

Consider the voltage controlled oscillator scheme outlined in Figure 5. At turn-on the non-inverting input rises rapidly to 1.2V as set by the resistor divider ($R_{13}/R_{15}$), while the external capacitor holds the inverting input low. The output quickly rises to 5.8V and begins charging the capacitor through $R_{11}$. The output simultaneously lifts the non-inverting input rapidly to 4.7V. When the voltage across the capacitor also reaches 4.7V, the output drops low, reverse biasing the diodes while the capacitor begins discharging through the potentiometer. With the output low, the non-inverting input is again resistively set at 1.2V until the capacitor discharges and the cycle repeats. The capacitor voltage decays about twenty times slower than it charges, resulting in a repetition rate dominated by the external RC time constant.

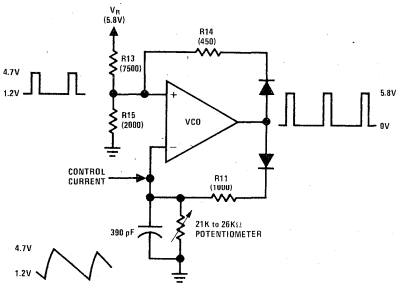



**FIGURE 5. Equivalent Circuit of VCO**

When the VCO is in its high state, the output is clamped at the regulated voltage. This causes the temperature coefficient of the trip points to be dependent on only the regulated voltage, resulting in an oscillation frequency quite independent of temperature.

Figure 6 details the frequency dividers used to transform the short duty cycle 76 kHz waveform into precisely 50% duty cycle 38 and 19 kHz waveforms. To understand their operation, first consider $Q_{24}/Q_{25}$ saturated while $Q_{23}/Q_{26}$ are in cutoff. As the trigger goes low the collector voltage for $Q_{25}/Q_{26}$ collapses and conduction in them ceases. Since $Q_{23}/Q_{24}$ are bistable by themselves, $Q_{24}$ remains saturated and $Q_{23}$ cutoff. With the trigger in this low state, the base of $Q_{24}$ sits at one base-emitter voltage (0.7V) while the base of $Q_{23}$ is at the saturation voltage of $Q_{24}$

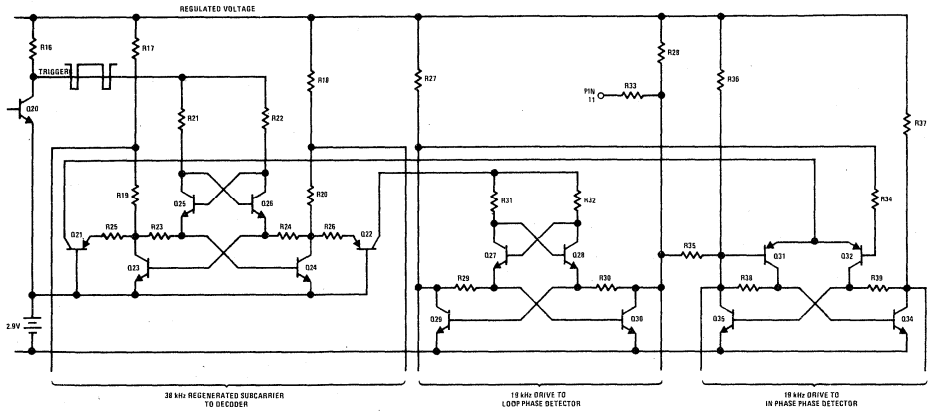



**FIGURE 6. Frequency Dividers**

(0.2V). On the rising edge of the trigger pulse, $Q_{26}$ conducts before $Q_{25}$ because of the different voltages on their emitters. $Q_{26}$ saturates and drives enough current through $R_{24}$ to saturate $Q_{23}$ while $Q_{24}$ goes to cutoff. Thus $Q_{23}/Q_{24}$ change state on every rising edge of a trigger pulse, dividing the repetition rate of the trigger signal by two. The other two frequency dividers function similarly except that the third one is slaved in quadrature

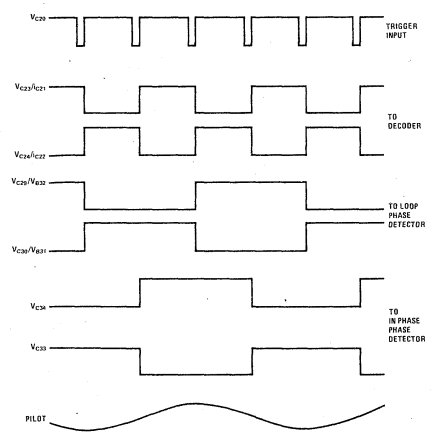



**FIGURE 7. Frequency Divider Waveforms**

with the second. Figure 7 shows the waveforms throughout the divider string.

### Loop Phase Detector

The loop phase detector is shown equivalently in Figure 8. Consider the loop phase detector where the toggle is driven in quadrature with the pilot.

The waveforms show that zero volts DC appears across the capacitor. Any deviation from this quadrature relationship produces a voltage, which

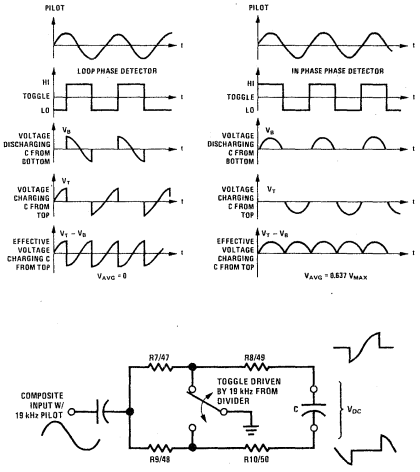



**FIGURE 8. Phase Detector Performance**

is a function of phase difference, across the capacitor. A second condition results when the toggle is driven in phase with the pilot. In this case the DC voltage across the capacitor measures pilot tone amplitude and is used to drive the stereo-monaural switching circuitry.

The DC amplifier in the phase locked loop is standard differential with push-pull output, maintaining excellent temperature stability in the loop.

### Stereo/Monaural Switching Circuitry

Composite inputs sufficiently large for good quality stereo switch the LM1800 into the stereo mode

via the circuitry of Figure 9. The differential pair $Q_{47}/Q_{48}$ is driven by the DC output of the "in phase" phase detector. When the phase locked loop is locked, this differential input voltage to $Q_{47}/Q_{48}$ is proportional to pilot amplitude (as explained in previous section and Figure 8). The emitter area of $Q_{47}$ is five times larger than that of $Q_{48}$, building in 40 mV offset voltage. Until the base of $Q_{48}$ is 40 mV higher than the base of $Q_{47}$, collector current in $Q_{47}$ is larger than collector current in $Q_{48}$. Transistor design of $Q_{49}$ constrains its beta to unity. So long as $I_{C47}$ is larger than $I_{C48}$, $Q_{49}$ remains in saturation (holding $Q_{50}$ in cutoff). When the 40 mV offset voltage is overcome in $Q_{47}/Q_{48}$, $Q_{49}$ comes out of saturation and $Q_{50}$ enters conduction. $Q_{50}$, $Q_{51}$, $D_5$, and $R_{51}$ form a positive feedback loop which regenerates when $Q_{50}$ is allowed to conduct. $R_{51}$ is chosen to halt the regeneration process at $I_{C51}$ = 30$\mu$A. The latched loop current drives the lamp driver Darlington ($Q_{54}/Q_{55}$) as well as $Q_{57}$ (via $Q_{52}$ and $Q_{53}$). The signal to the decoder switches from common to differential mode 38 kHz and stereo demodulation begins. Should the input composite waveform decrease by 6 dB, the differential voltage back at $Q_{47}/Q_{48}$ reduces to 20 mV. Under this condition the current flowing from $Q_{49}$ into $Q_{51}$ (as $Q_{49}$ returns toward saturation) is sufficient to unlatch the loop, prohibiting drive to both $Q_{57}$ and $Q_{54}/Q_{55}$. The signal driving the decoder returns to common mode 38 kHz and monaural reception resumes. $R_{52}$ and $Q_{56}$ limit cold lamp surge currents to about 250 mA.

**Decoder and Output Section**

The basic decoder section shown in Figure 10 has been used previously in the LM1304, LM1305, LM1307, LM1307E series, and is well described in reference 2. In an effort to transform the rigor into intuition, consider first $Q_{43}$, $Q_{44}$, and the emitter matrix resistors ($R_{44}$, $R_{45}$, $R_{46}$). Under small signal conditions the emitter of $Q_{43}$ remains at a constant voltage while the emitter of $Q_{44}$ tracks the composite input waveform applied to its base. Analysis of the simplified circuit shown in Figure 11 produces the current waveforms through $R_{44}$ and $R_{45}$. These currents are not equal and opposite as in a standard multiplier because $R_{46}$ in no way approximates a current source. Rather, the currents through $R_{44}$ and $R_{45}$ can be shown to be related by a constant:

$$K = I_{R44}/I_{R45} = R_{46}/(R_{45} + R_{46})$$

For NPN transistors operating in their active regions, collector current approximately equals emitter current, then:

$$I_{C43} = KI_{C44}$$

Since the upper quad transistors ($Q_{39}$, $Q_{40}$, $Q_{41}$, $Q_{42}$) operate as antiphase switches, the base current resulting through $Q_{38}$ becomes the sum of $I_{C44}$ gated by $Q_{42}$ and $I_{C43}$ gated by $Q_{40}$. These upper quad transistors alternately pass or block the currents flowing in $Q_{43}$ and $Q_{44}$. This gating

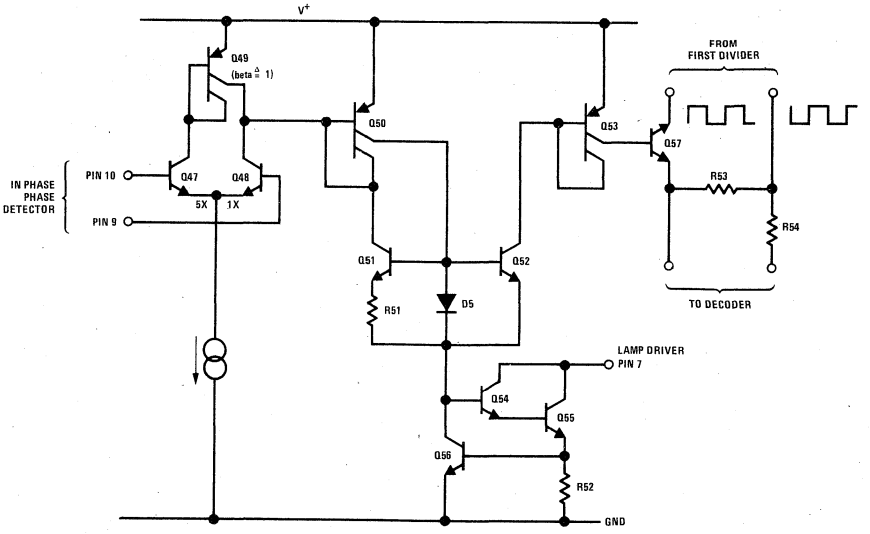



**FIGURE 9. Stereo/Monaural Switch**

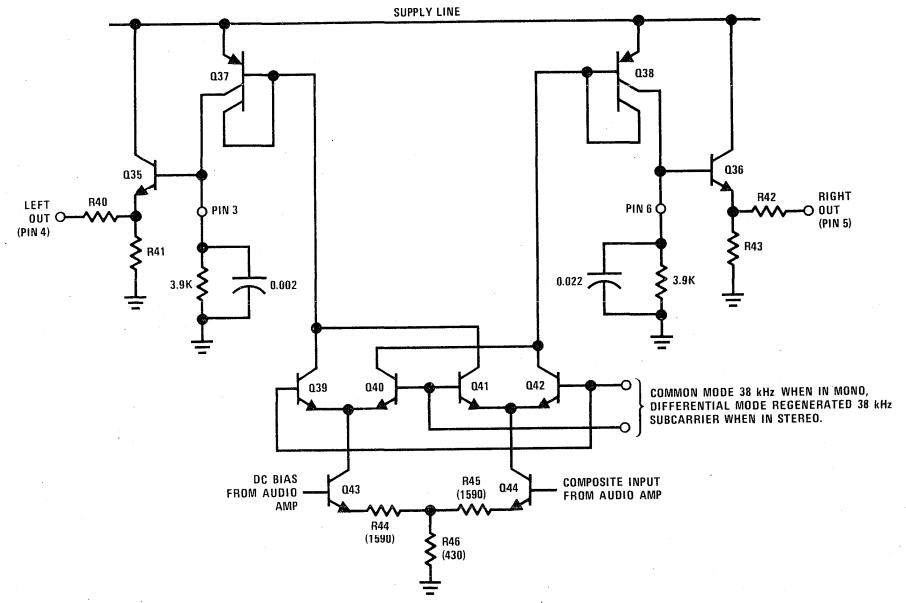



**FIGURE 10. Decoder and Output Section**

action is represented mathematically in Figure 12. Applying the gating function to the currents in $Q_{43}$ and $Q_{44}$:

$$I_{B38} = V_C \left[\frac{1}{2} - \frac{2}{\pi} \cos \omega_s t\right] - K V_C \left[\frac{1}{2} + \frac{1}{\pi} \cos \omega_s t\right]$$

where $V_C$ = composite input signal

and $\omega_s$ = subcarrier (38 kHz)

Substituting the expression for $V_C$ (given in Figure 1), carrying out the algebra, and retaining only the low frequency terms gives:

$$I_{B38} = L\left[0.5 - 0.5K - \frac{K+1}{\pi}\right] + R\left[0.5 - 0.5K + \frac{K+1}{\pi}\right]$$

Equating the coefficient of the left (L) term to zero, yields a value for K of 0.22. Thus designing the matrix resistors $R_{44}$, $R_{45}$, $R_{46}$ to give this value for K cancels all left information from the $Q_{38}$ current. The base current of $Q_{38}$ then is proportional to the right (R) separated signal.

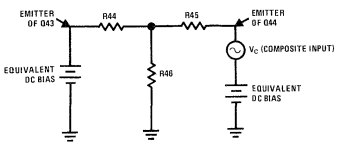
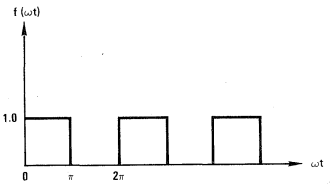



**FIGURE 11. Equivalent Circuit for Decoder Matrix**




$$f(\omega t) = \frac{1}{2} + \frac{2}{\pi} \sum \frac{1}{n} \cos n\omega t$$

$$= \frac{1}{2} + \frac{2}{\pi} \cos \omega t + \ldots$$

**FIGURE 12. Fourier Analysis of Decoder Switching Waveform**

Similar analysis can be performed to show that the base current of $Q_{37}$ contains only left (L) separated signal. Amplification and level shifting of these base currents occurs in fixed beta transistors $Q_{37}$ and $Q_{38}$, and the resultant currents drive external grounded loads at pins 3 and 6. Since the collector currents of $Q_{37}$ and $Q_{38}$ depend only on their respective base currents, supply ripple and noise are rejected from the output pins. $Q_{35}$ and $Q_{36}$ serve as output buffers with $R_{40}$ and $R_{42}$ setting the output resistance at typically 1300Ω.

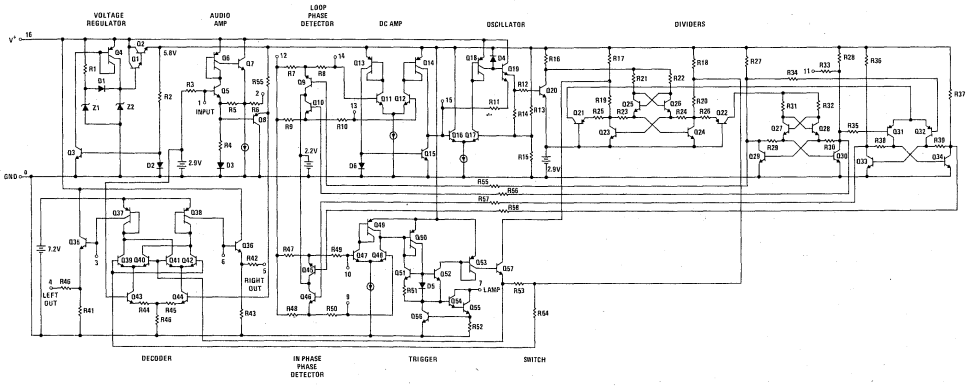



**FIGURE 13. LM1800 Equivalent Schematic**

In the monaural mode the upper quad transistors are driven by a common mode signal which causes all four transistors to conduct equally. This passes the composite input directly to the outputs where the de-emphasis capacitors serve to roll off the higher frequency unwanted information. Further, the LM1800 offers improved distortion over earlier integrated demodulators. As the signal driving the base of $Q_{44}$ increases in amplitude, the AC currents through $Q_{43}$ and $Q_{44}$ become a significant percentage of the DC bias currents. In this manner the transconductance of $Q_{43}$ and $Q_{44}$ is modulated by the incoming signal resulting in second harmonic distortion. To reduce this effect, the base bias potentials of $Q_{43}$ and $Q_{44}$ and the matrix resistor values have been raised above the levels used in earlier demodulators. The loss in gain that this implies is recovered in the PNP level shifting transistors.

## CIRCUIT PERFORMANCE

The circuit in Figure 14 illustrates the simplicity of designing an FM stereo demodulation system using the LM1800. $R_3$ and $C_3$ establish an adequate loop capture range and a low frequency well damped natural loop resonance. $C_8$ has the effect of shunting phase jitter, a dominant cause of high frequency channel separation problems. Recall that the 38 kHz subcarrier regenerates by phase locking the output of a 19 kHz divider to the pilot tone. Time delays through the divider result in the 38 kHz waveform leading the transmitted subcarrier. Addition of capacitor $C_9$ (0.0025$\mu$F) at pin 9 introduces a lag at the input to the phase lock loop, compensating for these frequency divider delays. The output resistance of the audio amplifier is designed at 500$\Omega$ to facilitate this connection.

Table I and Figures 15 through 27 detail typical performance resulting from this basic hookup. The excellent supply rejection characteristics shown, coupled with the fact that supply current drain is nearly independent of supply voltage, somewhat simplifies receiver power supply requirements. The low drain current, even for a 24V supply, results in cooler circuit operation and increased reliability. Figure 22 shows that increasing the size of input coupling capacitor $C_6$ improves low frequency channel separation by reducing the phase shift of the lower frequency components in the composite waveform.

Figure 27 illustrates an interesting characteristic of the LM1800: channel separation increases as the VCO is detuned in either direction. The separation peaks change in size for different signal frequencies and change in position (% detuning) for changing composite amplitudes. If the VCO free running frequency is set at precisely 19 kHz, separation remains constant over a wide range of composite amplitude levels, signal frequencies, temperature changes, and component drifts. The 19 kHz monitor available to the customer at pin 11 can be fed into a frequency counter for accurate adjustment of the VCO free running frequency. If a frequency counter is not available, the VCO can be adjusted by utilizing the fact that capture range is symmetrical about the incoming pilot:

(a) rotate frequency adjust pot full CCW
(b) insert weak composite input signal
(c) rotate pot CW until stereo lamp comes on, note position of pot ($R_x$)
(d) remove composite and rotate pot full CW
(e) reinsert weak composite input signal
(f) rotate pot CCW until stereo lamp comes on again, note position of pot ($R_y$)
(g) set pot midway between $R_x$ and $R_y$.

Figure 28 is included for the user who is willing to sacrifice some performance, particularly channel separation at high input levels and low frequencies to eliminate two external capacitors and reduce the electrolytic input coupling cap size.

On either circuit, some improvement in channel separation can be attained by altering the VCO

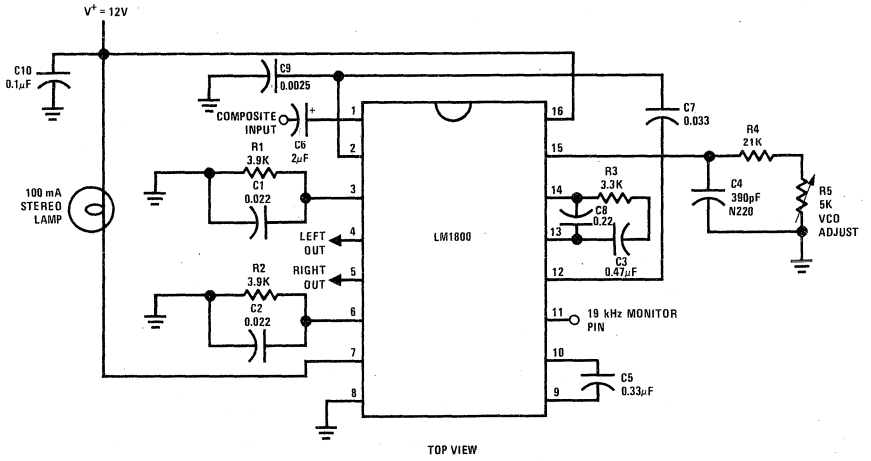



**FIGURE 14. Typical Application Circuit**

**TABLE 1.**

| PARAMETERS | CONDITIONS | TYP | UNITS |
|---|---|---|---|
| Supply Current | Lamp "OFF" | 21 | mA |
| Lamp Driver Saturation Voltage | 100 mA Lamp Current | 1.3 | V |
| Lamp Driver Leakage Current | | 1 | nA |
| Pilot Level for Lamp "ON" | Pin 11 Adjusted for 19 kHz ±10 Hz | 16 | mV |
| Pilot Level for Lamp "OFF" | Pin 11 Adjusted for 19 kHz ±10 Hz | 8 | mV |
| Stereo Lamp Hysteresis | | 6 | dB |
| Stereo Channel Separation | 100 Hz (Note 1) | 40 | dB |
| | 1000 Hz (Note 1) | 45 | dB |
| | 10000 Hz (Note 1) | 45 | dB |
| Monaural Channel Unbalance | 200 mVrms, 1000 Hz Input | 0.3 | dB |
| Recovered Audio | 200 mVrms, 400 Hz Input | 190 | mVrms |
| Total Harmonic Distortion | 500 mVrms, 1000 Hz Monaural Input | 0.5 | % |
| Capture Range | 25 mV of 19 kHz pilot | ±4 | % of $f_0$ |
| Supply Ripple Rejection | 600 mVrms, 200 Hz Ripple | 45 | dB |
| Dynamic Input Resistance | | 45 | kΩ |
| Dynamic Output Resistance | | 1300 | Ω |
| SCA Rejection | 200 mVrms Composite at 67 kHz | 50 | dB |
| Ultrasonic Frequency Rejection | Combined 19 and 38 kHz | 33 | dB |

**Note 1:** The stereo input signal is made by summing 123 mVrms left or right modulated signal with 25 mVrms of 19 kHz pilot tone, measuring all voltages with an average responding meter calibrated in rms, the resulting waveform is about 800 mVp-p. VCO adjusted to 19kHz ±10Hz.

**FIGURE 15. Supply Drain**

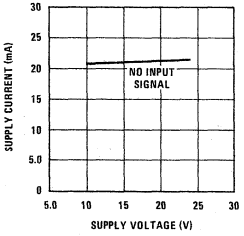



**FIGURE 16. Total Harmonic Distortion**

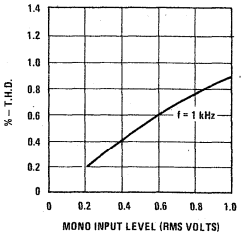



**FIGURE 17. Supply Ripple Rejection**

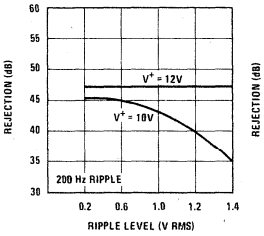



**FIGURE 18. Supply Ripple Rejection**

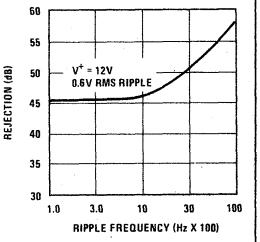



**FIGURE 19. VCO Temperature Stability**

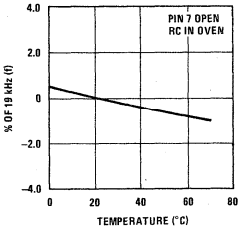



**FIGURE 20. VCO Supply Sensitivity**

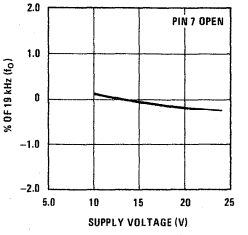



**FIGURE 21. Pilot Level For Lamp On**

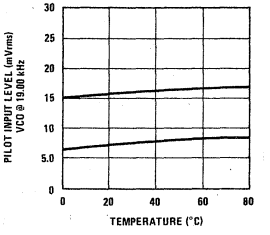



**FIGURE 22. Channel Separation**

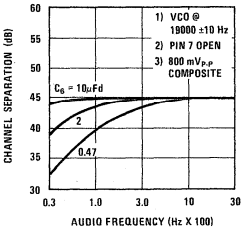



**FIGURE 23. Channel Separation**

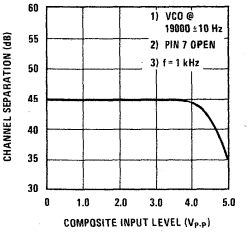



**FIGURE 24. Output Frequency Spectrum**

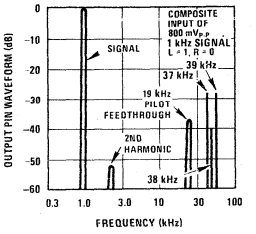



**FIGURE 25. Capture Range**

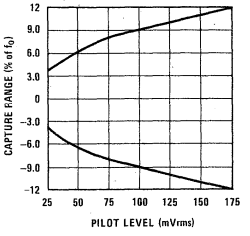



**FIGURE 26. Lamp Driver Characteristics**

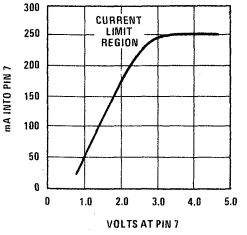
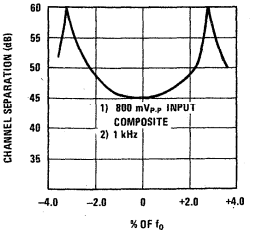



**FIGURE 27. Channel Separation and VCO Tuning**



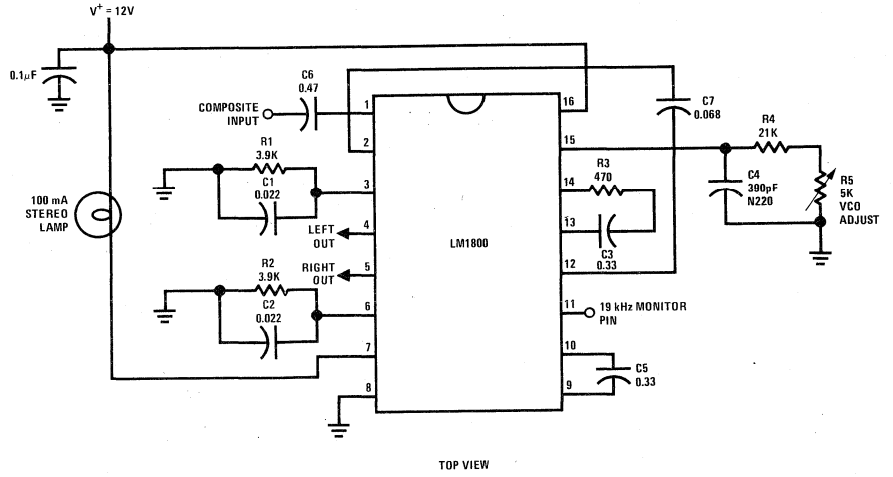



**FIGURE 28. Minimum Parts Count Application Circuit**

slightly. The loop gain can be shown to decrease for a decrease in VCO resistance ($R_4$ + $R_5$ in Figure 14). Maintaining a constant RC product, while increasing the capacity from 390 pF to 510 pF narrows the capture range by about 25%. Although the resulting system has slightly improved channel separation, it is more sensitive to VCO tuning.

When the circuits so far described are connected in an actual FM receiver, channel separation often suffers due to imperfect frequency response of the IF stage. The input lead network of Figure 29

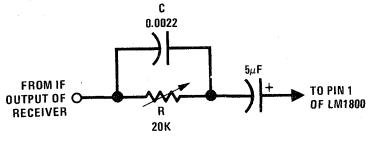



**FIGURE 29. Compensation for Receiver IF Rolloff**

can be used to compensate for roll off in the IF and will restore high quality stereo sound. Should a receiver designer prefer a stereo/monaural switching point different than those programmed into the LM1800 (pilot: 16 mVrms on, 8.0 mVrms off typical), the circuit of Figure 30 provides the desired flexibility.

The user who wants slightly increased voltage gain through the demodulator can increase the size of the load resistors ($R_1$ and $R_2$ of Figure 14 or 28), being sure to correspondingly change the de-emphasis capacitors ($C_1$ and $C_2$). Loads as high as 5600Ω may be used (gain of 1.4). Performance of the LM1800 is virtually independent of the supply voltage used (from 10 to 24V) due to the on chip regulator.

Although the circuit diagrams show a 100 mA indicator lamp, the user may desire an LED. This presents no problem for the LM1800 so long as a resistor is connected in series to limit current to a safe value for the LED. The lamp or LED can be powered from any source (up to 24V), and need not necessarily be driven from the same supply as the LM1800.

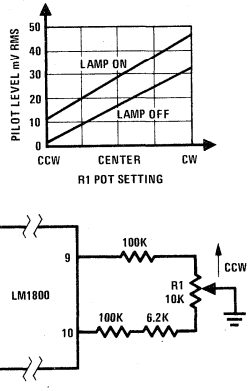



**FIGURE 30. Stereo/Monaural Switch Point Adjustment**

Utilization of the phase locked loop principle enables the LM1800 to demodulate FM stereo signals without the use of troublesome and expensive coils. The numerous features available on the demodulator make it extremely attractive in a variety of home and automotive receivers. Indeed the LM1800 represents a new generation in integrated stereo FM demodulators.

## REFERENCES

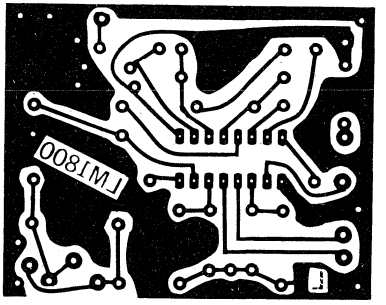

1. Blaser, L. and Cocke, W., *"The μA758, A Phase Locked Loop FM Stereo Multiplex Decoder."* Fairchild Application Note 319, June 1972.

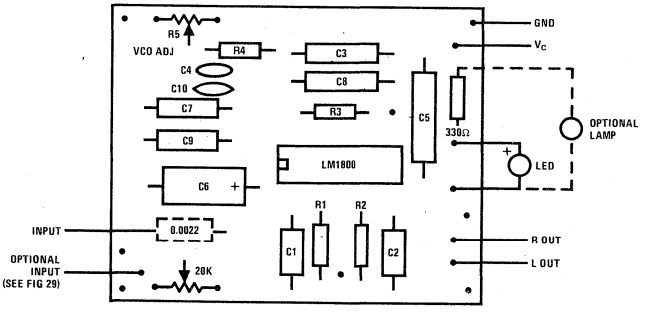
2. Hector Gasquet, *"A Monolithic Integrated FM Stereo Decoder System."* Motorola Application Note AN-432A.

3. Michael J. Gay, *"A Monolithic Phase-Lock-Loop Stereo Decoder."* IEEE Transactions on Broadcast and TV Receivers, Vol. BTR-17, No. 3, August 1971.

4. Thomas B. Mills, *"The Phase Locked Loop IC as a Communication System Building Block."* National Semiconductor Application Note AN-46, June 1971.

5. *"Phase Locked Loops Applications Book,"* Signetics Corporation, 1972.


**Printed Circuit Board Layout for Circuit of Figure 14.**

Todd Smathers
Nello Sevastopoulos
MAY 1974

# LM125/LM126/LM127 PRECISION DUAL TRACKING REGULATORS

## INTRODUCTION

The LM125, LM126, and LM127 family of devices are precision, dual, tracking, monolithic voltage regulators. Each provides separate positive and negative regulated outputs, thus simplifying dual power supply designs. Operation requires few or no external components depending on the application. Internal settings provide fixed output voltages: the LM125 at ±15V, the LM126 at ±12V, and the LM127 at +5.0V and −12V for use in MOS applications.

Each regulator is protected from excessive internal power dissipation by a thermal shutdown circuit which turns off the regulator whenever the chip reaches a preset maximum temperature. Other features include both internal and external current limit sensing for device protection while operating with or without external current boost. For applications requiring more current than the internal current limit will allow, boosted operation is possible with the addition of a one NPN pass transistor per regulator. External resistors sense load current for controlling the limiting circuitry. Internal frequency compensation is provided on both positive and negative regulators. The internal voltage reference pin is brought out to facilitate noise filtering when desired.

## CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the basic dual tracking regulator. A voltage reference establishes a fixed dc level, independent of supply or temperature variations, at the non-inverting input to the negative regulator Error Amplifier. The Error Amplifier drives the Output Control Circuit which includes the high current output transistors, current limiting, and thermal shutdown circuitry.

The negative regulator output voltage is established by comparing the Voltage Reference against a fraction of the output as set by $R_A$ and $R_B$.

To achieve the desired tracking action of the positive regulator, a voltage established between the positive and negative regulator outputs by resistors $R_C$ and $R_D$ is compared to ground by the positive regulator Error Amplifier. This insures

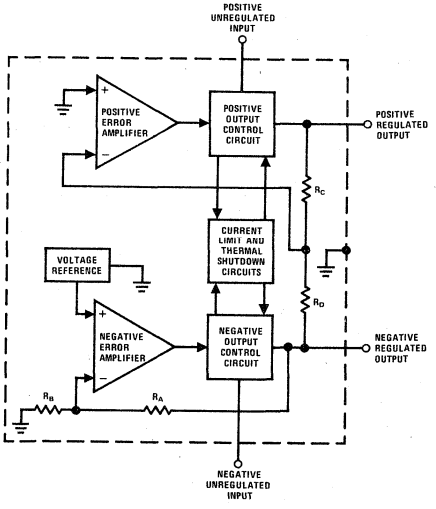



**FIGURE 1. Block Diagram for the Basic Dual Tracking Regulator**

that the positive regulator output voltage will always equal the negative regulator output voltage multiplied by the ratio of $R_C$ to $R_D$. This ratio is unity for the LM125 ($V_O$ = ±15V), and LM126 ($V_O$ = ±12V), and equals 5/12 for the LM127. The positive regulator Output Control Circuit is essentially the same as that in the negative regulator.

The current limit and thermal shutdown circuitry sense the output load current and die temperature

respectively and switch off all output drive capability upon reaching their predetermined limits.

Figure 2 gives a more detailed picture of the negative regulator circuitry. The temperature compensated reference voltage appears at the non-inverting input of the differential amplifier, Q19 and Q20, while an error signal proportional

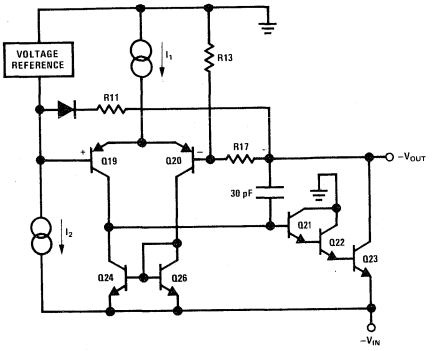



**FIGURE 2. Simplified Negative Regulator**

to any change in output voltage is applied to the other input. This error signal is amplified by the differential amplifier, Q19 and Q20, and by the triple Darlington Q21, Q22, Q23 to produce a current change through R13 and R17 which brings the output voltage back to its original value. Loop gain is high, typically 88 dB at low output currents, so a 30 pF compensating capacitor is used to guarantee stability. Since $-V_{OUT}$ is the output of a high gain feedback amplifier, high supply rejection is ensured.

Figure 3 shows the basic positive regulator. This is actually an inverting operational amplifier.

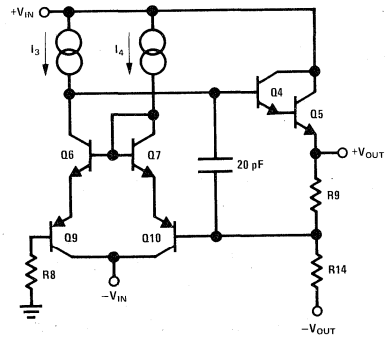



**FIGURE 3. Simplified Positive Regulator**

The negative regulated voltage ($-V_{OUT}$) is applied to the current summing input through R14 while the output ($+V_{OUT}$) is fed-back via R9. Then $+V_{OUT}$ is simply $-$ (R9/R14) ($-V_{OUT}$). Any change in the positive regulator output will create an error signal at the base of Q10 which will be amplified and sent to the voltage follower, Q4 and Q5, forcing the output voltage to track the input voltage. Here the loop gain is on the order of 66 dB so a compensating capacitor of approximately 20 pF is used to ensure amplifier stability.

The circuitry used for regulator start up, biasing, temperature sensing, and thermal shutdown is shown in Figure 4. The field effect transistor Q28, is initially ON allowing the negative input voltage to force current through zener diode Q34. When enough current flows to fully establish the zener voltage, transistor Q29, Q30 and Q31 turn on and bias up all current sources. The zener voltage also decreases the gate to source voltage of the FET, pinching it off to a lower current value to reduce quiescent power dissipation.

The thermal sensing and shutdown circuitry is comprised of Q34, Q29, Q35, Q32, Q37, Q38, R27, R29, R30, R31, and R33. The voltage divider made up of R29 and R30 provides a relatively fixed bias voltage $V_1$ at the bases of Q35 and Q36, holding them in the OFF state. When the chip temperature increases to a maximum permissible level, the base to emitter voltage of Q35 and/or Q36 will have decreased sufficiently so that $V_1$ is now high enough to turn them ON. This causes a voltage drop across R27 sufficient to turn on Q32 which switches Q37 and Q38 to a conducting state shunting all output drive current to $-V_{IN}$. The regulator output voltages are then clamped to zero. Transistors Q35 and Q36 are located on the chip near the regulator output devices so they will see the maximum temperatures reached on the chip, ensuring that neither regulator will ever see more than this preset maximum temperature. The collectors of Q35 and Q36 are tied together so that if either regulator reaches the thermal shutdown temperature, both regulators will shutdown. This ensures that the device can never be destroyed because of excessive internal power dissipation in either regulator.

Figure 5 shows the current limiting circuitry used in the positive regulator; the negative regulator current limiter is identical. The internal current limiter is comprised of Q8 and R5; the external current limiter is comprised of Q11 and an external resistor $R_{CL}$. Both operate in a similar manner. As the output current through Q5 increases, the voltage drop across resistor R5 eventually turns ON Q8 and shunts all base drive away from the output devices, Q4 and Q5. The maximum load current available with this circuit is approximately 250 mA at $T_j = 25°C$ (see Figure 9).

The external current limiting circuit works in a similar manner. Here the output current is sensed across the external resistor $R_{CL}$. When the voltage

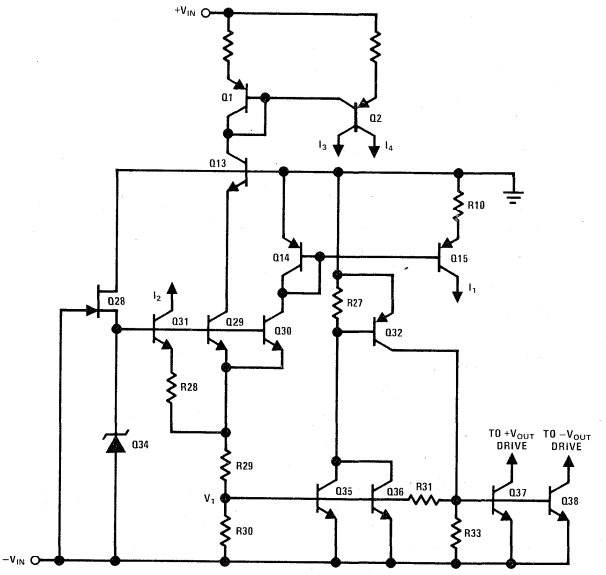



**FIGURE 4. Start-up, Biasing and Thermal Shutdown Circuitry**

drop across $R_{CL}$ is sufficient to turn ON transistor Q11, the output drive current is switched away from the output devices Q4 and Q5. This externally set current limit is particularly valuable when used with an external current boosting pass transistor where the current limit could be set to protect that transistor from excessive power dissipation.

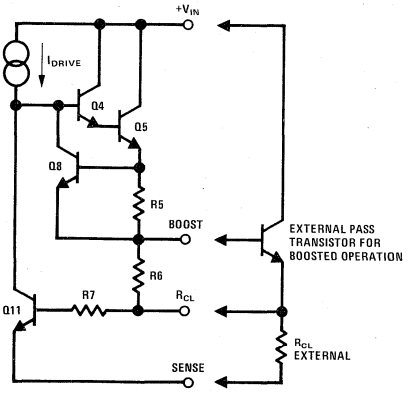



**FIGURE 5. Positive Regulator Current Limiting Circuitry**

The constant voltage reference circuit is shown in Figure 6. Zener diode $Z_1$ has a positive temperature coefficient of known value. $V_{BE}$ of Q18 (negative temperature coefficient) is multiplied by the ratio of R18 and R19 and added to the positive TC of $Z_1$ to produce a near zero TC voltage reference. Current source $I_2$ is used only during start-up.

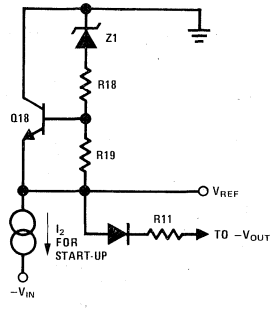
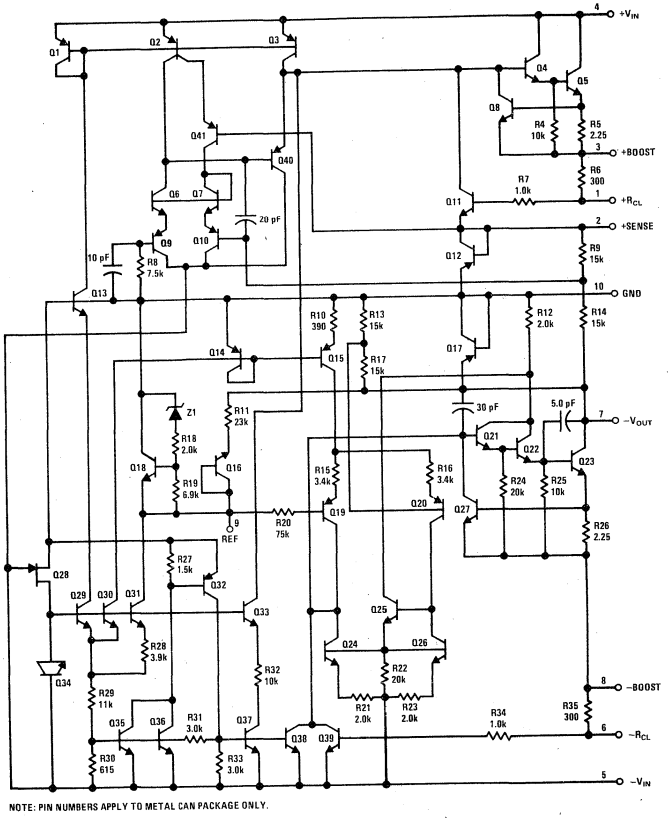



**FIGURE 6. Voltage Reference Circuitry**

Figure 7 shows the complete schematic of the LM125, LM126, LM127 family of dual regulators. Diodes Q12 and Q17 protect the output transistors, plus any external pass devices used, from breakdown in the event the positive and negative regulated outputs become shorted. Transistors Q6 and Q7 offer full differential voltage gain with the convenience of single ended output. Transistors Q13 and Q33 insure that operation with ±30V input is possible. Q24 and Q26 in the negative regulator amplifier provide single ended output from a differential input with no loss in gain.

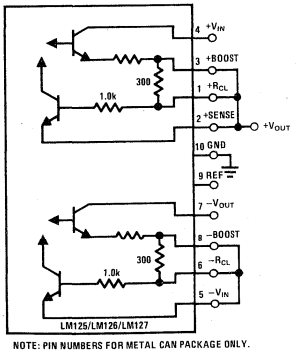



NOTE: PIN NUMBERS APPLY TO METAL CAN PACKAGE ONLY.

**FIGURE 7. LM125/LM126/LM127**

## APPLICATIONS

The basic dual regulator is shown connected in Figure 8. The only connections required other than plus and minus inputs, outputs, and ground



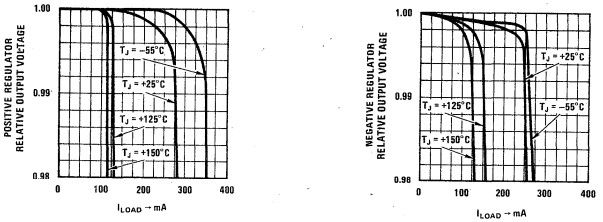

NOTE: PIN NUMBERS FOR METAL CAN PACKAGE ONLY.

**FIGURE 8. Basic Dual Regulator**

are to complete the output current paths from $+R_{CL}$ to $+V_{OUT}$ and from $-R_{CL}$ to $-V_{IN}$. These may be a direct shorts if the internal preset current limit is desired, or resistors may be used to set the maximum current at some level less than the internal current limit. The internal 300Ω resistors from pins 3 to 1 and pins 8 to 6 should be shorted as shown when no external pass transistors are used. To improve line ripple rejection and transient response, filter capacitors may be added to the inputs, outputs, or both, depending on the unregulated input available. If a very low noise output voltage is desired, a capacitor may be connected from the reference voltage pin to ground. Thus shunting noise generated by the reference zener. Figure 9 shows the internal current limiting characteristics for the basic regulator circuit of Figure 8.

## HIGH CURRENT REGULATOR

For applications requiring more supply current than can be delivered by the basic regulator, an external NPN pass transistor may be added to each regulator. This will increase the maximum output current by a factor of the external transistor beta. The circuit for current boosted operation is shown in Figure 10.




(A) (B)

**FIGURE 9. Internal Current Limiting Characteristics**

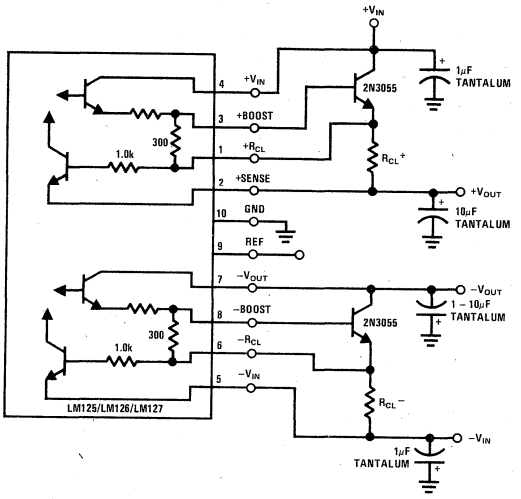



**FIGURE 10. Boosted High Current Regulator**

In the boosted mode, current limiting is often a necessary requirement to insure that the external pass device is not overheated or destroyed. Experience shows this to be the usual cause of IC regulator failure. If the regulator output is grounded the pass device may fail and short, destroying the regulator. To limit the maximum output current, a series resistor ($R_{CL}$ in Figure 10) is used to sense load current. The regulator will current limit when the voltage drop across $R_{CL}$ equals the current limit sense voltage found in Figure 11. Figure 12 shows the external current limiting characteristics unboosted and Figure 13 shows the external current limiting characteristics in the boosted mode.

To ensure circuit stability at high currents in this configuration, it may be necessary to bypass each input with low inductance, tantalum capacitors to prevent forming resonant circuits with long input leads. A $C \geq 1\mu F$ is recommended. The same problem can also occur at the regulator output where a $C \geq 10\mu F$ tantalum will ensure stability and increase ripple rejection.

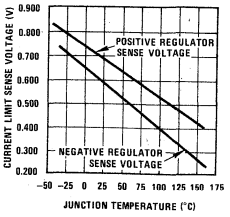


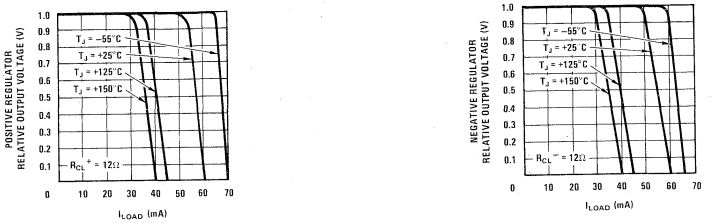

**FIGURE 11. Current Limit Sense Voltage for a 0.1% Change in Regulated Output Voltage**

The 2N3055 pass device is low in cost and maintains a reasonably high beta at collector currents up to several amps. The devices 2N3055 may be of either planar or alloy junction construction. The planar devices, have a high $f_T$ providing more stable operation due to low phase shift. The

alloy devices, with $f_T$ typically less than 1.0 MHz, may require additional compensation to guarantee stability. The simplest of compensation for the slower devices is to use output filter capacitor values greater than 50μF (tantalum). An alternative is to use an RC filter to create a leading phase response to cancel some of the phase lag of the devices. The stability problem with slower pass transistors, if it occurs at all, is usually seen only on the negative regulator. This is because the positive regulator output stage is a conventional Darlington while the negative output stage contains three devices in a modified triple Darlington connection giving slightly more internal phase shift. Additional compensation may be added to the negative regulator by connecting a small capacitor in the 100 pF range from the negative boost terminal to the internal reference. Since the positive regulator uses the negative regulator output for a reference, this also offers some additional indirect compensation to the positive regulator.

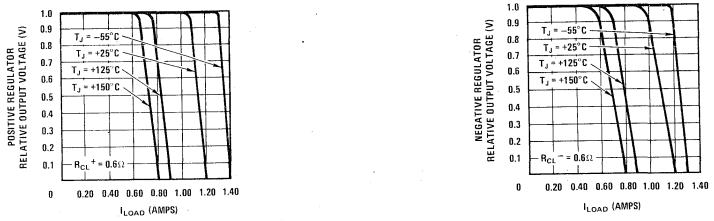
## 7 AMP REGULATOR

In Figure 14 the single external pass transistor has been replaced by a conventional Darlington




(A) (B)

**FIGURE 12. External Current Limiting Characteristics- Unboosted**




(A) (B)

**FIGURE 13. External Current Limiting Characteristics- Boosted**

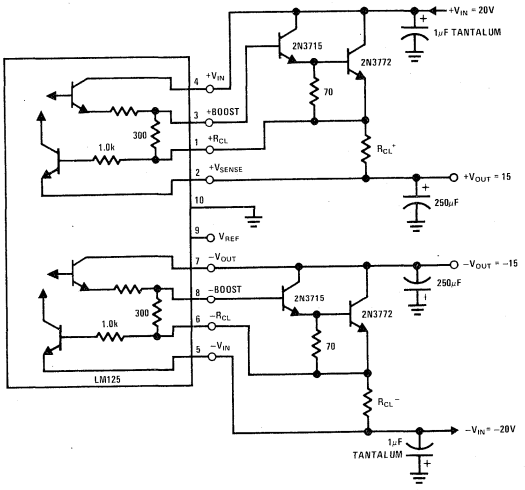



**FIGURE 14. High Current Regulator Using a Darlington Pair for Pass Elements**

using a 2N3715 and a 2N3772. With this configuration the output current can reach values to 10A with very good stability. The external Darlington stage increases the minimum input-output voltage differential to 4.5V. When current limit protection resistor is used, as in Figure 14, the maximum output current is limited by power dissipation of the 2N3772 (150W at 25°C). During normal operation this is $(V_{IN}-V_{OUT})\ I_{OUT}$ (W), but it increases to $V_{IN}\ I_{SC}$ (W) under short circuit conditions. The short circuit output current is then:

$$I_{SC} = \frac{P_{MAX}\ (T_C = 25^\circ C)}{V_{IN}}$$

$$= \frac{150W}{20V\ (min)} = 7.5A\ max.$$

$I_L$ could be increased to 10A or more only if $I_{SC} < I_L$. A foldback current limit circuit will accomplish this. The typical load regulation is 40 mV from no load to a full load. ($T_j$ = 25°C, pulsed load with 20 ms $t_{ON}$ and 250 ms $t_{OFF}$.)

## FOLDBACK CURRENT LIMITING

In many regulator applications, the normal operation power dissipation in the pass device can easily be multiplied by a factor of ten or more when the output is shorted. This may destroy the pass device, and possibly the regulator, unless the heat sink is oversized to handle this fault condition. A foldback current limiting circuit reduces short circuit output current to a fraction of the full load output current thus avoiding the need for larger heat sink. Figure 15 shows a foldback current limiting circuit on both positive and negative regulators.

The foldback current limiting, a fraction of the output voltage must be used to oppose the voltage across the current limit sense resistor. Current limiting does not occur until the voltage across the sense resistor is higher than this opposing voltage by the amount shown in Figure 11. When the output is grounded, the opposing voltage is no longer present so current limiting occurs at a lower level. This is accomplished in Figure 15 by using a programmable current source to give a constant voltage drop across R5 for the negative regulator, and by a simple resistor divider for the positive regulator. The reason for the difference between the two is that the negative regulator current limiting circuit is located between the output pass transistor and the unregulated input while the positive regulator current limiter is between the output pass transistor and the regulated output.

The operation of the positive foldback circuit is similar to that described in NSC application note AN-23. A voltage divider R1 and R2 from $V_E$ to ground creates a fixed voltage drop across R1 opposite in polarity to the drop across $R_{CL}{}^+$. When the load current increases to the point where the drop across $R_{CL}{}^+$ is equal to the drop across R1 plus the current limit sense voltage given in Figure 11, the positive regulator will begin to current limit. As the positive output begins to drop, the voltage across R1 will also decrease so that it now requires less load current to produce the current limit sense voltage. With

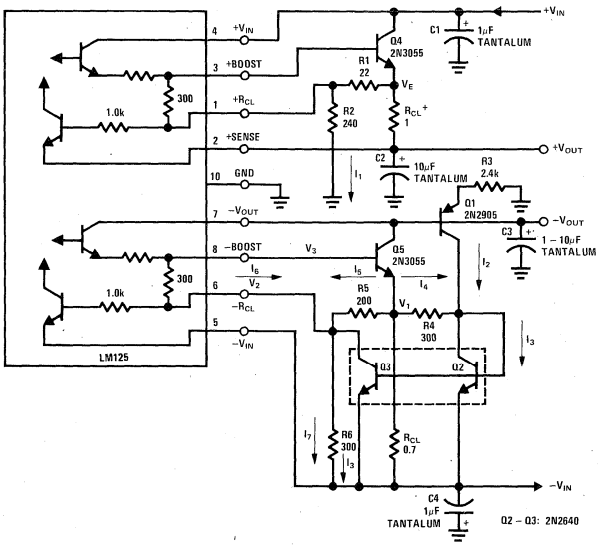



**FIGURE 15. Foldback Current Limiting Circuit**

the regulator output fully shorted to ground ($+V_{OUT} = 0$) the current limit will be set by the value of $+R_{CL}$ alone.

If $\frac{I_{FB}}{I_{SC}} \leq 5$

then the following equations can be used for calculating the positive regulator foldback current limiting resistors.

$$R_{CL}^{+} = \frac{V_{SENSE}}{I_{SC}} \quad (1)$$

where $V_{SENSE}$ is from Figure 11.

At the maximum load current foldback point:

$$V_{RCL}^{+} = I_{FB}\, R_{CL}^{+} \quad (2)$$

$$V_{R1} = V_{RCL}^{+} - V_{SENSE} \quad (3)$$

$$V_{R1} = I_{FB}\, R_{CL}^{+} - V_{SENSE} \quad (4)$$

Then

$$R1 = \frac{V_{R1}}{I_1} \quad (5)$$

and

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} \quad (6)$$

The only point of caution is to ensure that the total current ($I_1$) through R2 is much greater than the current contribution from the internal 300Ω resistor. This can be checked by:

$$\frac{I_{FB}\, R_{CL}^{+}}{300} \ll I_1 \quad (7)$$

Note: The current from the internal 300Ω resistor is $V_{3\text{-}1}/300\Omega$, but $V_{3\text{-}1} = V_{BE} + V_{RCL} - V_{SENSE}^{+}$ assuming $V_{BE} \approx V_{SENSE}^{+}$ at the foldback point, $V_{3\text{-}1} \approx V_{RCL}^{+} = I_{FB}\, R_{CL}^{+}$.

Design example: 2 amp regulator LM125 positive foldback current limiting (see Figure 15).

Given:

$I_{FOLDBACK} = 2.0A$

$I_{SHORT\text{-}CIRCUIT} = 500$ mA

$V_{SENSE}$ (See Figure 11)

$+V_{IN} = 25V$

$+V_{OUT} = 15V$

$\beta_{PASS\ DEVICE} = 70$

$\theta_{JA} = 150^{\circ}C/W$

$T_A = 50^{\circ}C$

With a beta of 70 in the pass device and a maximum output current of 2.0A the regulator must deliver:

$$\frac{2A}{\beta} = \frac{2A}{70} = 29\ mA$$

The LM125 power dissipation will be calculated ignoring any negative output current for this example.

$$P_{LM125} = (V_{IN} - V_{OUT})\, I_{OUT}$$
$$= (25 - 15)\ 29\ mA$$
$$= 290\ mW$$

$$T_{RISE} @ \theta_{JA} = 150^{\circ}C/W = 150^{\circ}C \times 0.29 = 44^{\circ}C$$

$$T_J = T_A + T_{RISE} = 50^{\circ}C + 44^{\circ}C = 94^{\circ}C$$

From Figure 11:

$V_{SENSE} @ (T_J = 94^{\circ}C) = 520$ mW

From equation (1)

$$R_{CL}^{+} = \frac{V_{SENSE}}{I_{SC}} = \frac{520\ mV}{500\ mA} \cong 1\Omega$$

From equation (2)

$$V_{RCL}^{+} = I_{FB}\, R_{CL}^{+} = 2A \cdot 1\Omega = 2V$$

From equation (3)

$$V_{R1} = V_{RCL}^{+} - V_{SENSE}$$

$$V_{R1} = 2V - 520\ mV = 1.480V$$

A value for $I_1$ can now be found from equation (7)

$$\frac{I_{FB}\, R_{CL}^{+}}{300} = \frac{2A \cdot 1\Omega}{300\Omega} = 6.6\ mA$$

So set $I_1 = 10 \times 6.6\ mA = 66\ mA$

From equations (5) and (6)

$$R1 = \frac{V_{R1}}{I_1} = \frac{1.480V}{66\ mA} \cong 22\Omega$$

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} = \frac{15 + 0.520}{66\ mA}$$

$$\cong 240\Omega$$

The foldback limiting characteristics are shown in Figure 16 for the values calculated above at various operating temperatures.

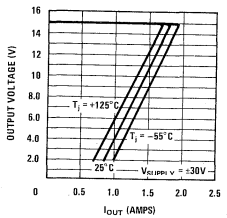



**FIGURE 16. Positive Regulator Foldback Current Limiting Characteristics**

The negative regulator foldback current limiting works essentially the same way as the positive side. Q1 forces a constant current, $I_2$, determined by $-V_{OUT}$ and R3, through Q2. Transistors Q2 and Q3 are matched so a current identical to $I_3$ will flow through Q3. With the output short-circuited ($-V_{OUT} = 0$), Q1 will be OFF, setting $I_2 = 0$. The load current will be limited when $V_1$ increases sufficiently due to load current to make $V_2$ higher than $-V_{IN}$ by the current limit sense voltage.

The short circuit current is:

$$I_{SC} \simeq \frac{V_{SENSE}}{R_{CL}^-} \qquad (8)$$

For calculating the maximum full load current with the output still in regulation, current $I_2$

$$I_2 = \frac{V_{OUT} - V_{BEQ1}}{R3} \qquad (9)$$

At the point of maximum load current, $I_{FB}$, where the regulator should start folding back:

$$V_1 = -V_{IN} + I_{FB}\ R_{CL}^- \qquad (10)$$

and

$$V_2 = -V_{IN} + V_{SENSE} \qquad (11)$$

The current through Q2 (and Q3) will have increased from $I_2$ by the amount of $I_4$ due to the voltage $V_1$ increasing above its no-load quiescent value. Since the voltage across Q2 is simply the diode drop of a base-emitter junction:

$$I_4 = \frac{[V_1 - (-V_{IN})] - V_{BE}}{R4}$$

Substituting in equation (10) gives:

$$I_4 = \frac{I_{FB}\ R_{CL}^- - V_{BE}}{R4} = \frac{I_{FB}\ R_{CL}^- - V_{BE}}{300\Omega} \qquad (12)$$

The current through Q2 is now

$$I_3 = I_2 + I_4 \qquad (13)$$

and the current through Q3 is:

$$I_3 = I_5 + I_6 - I_7 \qquad (14)$$

The drop accross R5 is found from:

$$V_1 - V_2 = (-V_{IN} + I_{FB}\ R_{CL}^-) - [V_{SENSE} + (-V_{IN})];$$

simplifying,

$$V_1 - V_2 = I_{FB}\ R_{CL}^- - V_{SENSE} \qquad (15)$$

Since $V_{SENSE}$ is the base to emitter voltage drop of the internal limiter transistor, the $V_{SENSE}$ in equation (15) very nearly equals the $V_{BE}$ in equation (12). Therefore the drop across R5 approximately equals the drop across R4. The current through R5, $I_5$, can now be determined as:

$$I_5 = \frac{I_{FB}\ R_{CL}^- - V_{SENSE}}{R5} \qquad (16)$$

Summing the currents through Q3 is now possible assuming the base-emitter drop of the 2N3055 pass device can be given by $V_{BE} \approx V_{SENSE}$:

$$I_6 = \frac{V_3 - V_2}{300} \qquad (17)$$

where $V_3 = V_1 + V_{BE} \approx V_1 + V_{SENSE}$

$$I_6 = \frac{V_1 + V_{SENSE} - V_2}{300}$$

Substituting in equation (15)

$$I_6 = \frac{I_{FB}\ R_{CL}^-}{300}$$

$$I_7 = \frac{V_2 - (-V_{IN})}{R6} = \frac{V_{SENSE}}{R6} \qquad (18)$$

Equating equation (13) with equation (14) and inserting resistor values shown in Figure 15,

$$I_2 + I_4 = I_5 + I_6 - I_7$$

$$I_2 + \frac{I_{FB}\, R_{CL}^- - V_{SENSE}}{300} = I_5 + \frac{I_{FB}\, R_{CL}^-}{300} - \frac{V_{SENSE}}{300} \qquad (19)$$

Canceling, we find:

$$I_2 = I_5 \qquad (20)$$

This is the key to the negative foldback circuit. Current source Q1 forces current $I_2$ to flow through resistor R5. The voltage drop across R5 opposes the normal current limit sense voltage so that the regulator will not current limit until the drop across $R_{CL}^-$ due to load current, equals the controlled drop across R5 plus $V_{SENSE}$ (given in Figure 11). This can be written as:

$$I_{FB} = \frac{V_{SENSE} + I_2\, R5}{R_{CL}^-} \qquad (21)$$

$$I_{FB} = \frac{V_{SENSE} + 200\, I_2}{R_{CL}^-}$$

A design example is now offered:

Given:

$I_{FOLDBACK} = 2.5A$

$I_{SHORT\text{-}CIRCUIT} = 750\ mA$

$V_{SENSE}$ (See Figure 11)

$-V_{IN} = 25V$

$-V_{OUT} = -15V$

$\beta_{PASS\ DEVICE} = 90$

$\theta_{JA} = 150°C/W$

$T_A = 25°C$

The same calculations are used here to figure $V_{SENSE}$ as with the positive regulator foldback example maximum regulator output current is calculated from:

$$I_{OUT} = \frac{2.5\ A}{90} = 28\ mA$$

$$P_{LM125} = (V_{IN} - V_O)\, I_{OUT}$$
$$= 10V \times 28\ mA$$
$$= 280\ mW$$

$$T_{RISE} = 150°C/W \times 0.28W = 42°C$$

$$T_J = T_A + T_{RISE} = 25°C + 42°C = 67°C$$

From Figure 11:

$$V_{SENSE} = 500\ mV$$

From equation (8):

$$R_{CL}^- = \frac{500\ mV}{750\ mA} = 0.68\Omega$$

From equation (21):

$$I_2 = \frac{I_{FB}\, R_{CL}^- - V_{SENSE}}{200\Omega} = 6.0\ mA$$

From equation (9):

$$R3 = \frac{V_{OUT} - V_{BEQ1}}{I_2}$$

$$R3 \simeq \frac{14.3}{6.0\ mA} = 2.4k$$

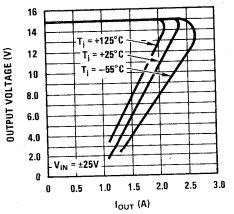



**FIGURE 17. Negative Regulator Foldback Current Limiting Characteristics**

Figure 16 and 17 show the measured foldback characteristics for the values derived in the design examples. The value of R5 is set low so that the magnitude of $I_5$ for foldback is greater than $I_4$ through $I_6$. This reduces the foldback point sensitivity to the TC of the internal 300Ω resistor and any mismatch in the TC of Q2, Q3 or the pass device.

R6 can be computed from equation (18):

$$R6 = \frac{V_{SENSE}^-}{I_7} = \frac{V_{SENSE}^-}{I_5 + I_6 - I_3}$$

combining (13) and (20).

$$R6 = \frac{V_{SENSE}^-}{I_6 - I_4} = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left(\frac{1}{300} - \frac{1}{R4}\right) + \frac{V_{BE}}{R4}} \quad (22)$$

Setting $V_{BE} \simeq V_{SENSE}$ and R4 = 300 to match the internal 300Ω (22) becomes:

$$R6 = R4$$

Also setting $\frac{I_4}{I_5} = \frac{2}{3} \rightarrow R5 = 200$

## A 10 AMP REGULATOR

Figure 18 illustrates the complete schematic of a 10A regulator with foldback current limiting. The design approach is similar to that of the 2A regulator. However, in this design, the current contribution from the internal 300Ω resistor is greater due to the 2 $V_{BE}$ drop across the Darlington pair. Expression (7) becomes:

$$\frac{I_{FB}\, R_{CL}^+ + V_{BE}}{300} << I_1 \; ; \quad (23)$$

and, for the negative regulator, expression (22) becomes:

$$R6 = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left[\frac{1}{300} - \frac{1}{R4}\right] + V_{BE}\left[\frac{1}{300} + \frac{1}{R4}\right]} \quad (24)$$

The disagreement between the theoretical and experimental values for the negative regulator is not alarming. In fact $R_{CL}$ was based on equation (8), which is correct if for zero $V_{OUT}$, $I_5$ is zero as well. This implies:

$$V_{SENSE}\ (\text{at SC}) = \frac{V_{BEQ4} + V_{BEQ5}}{2}\ (\text{at SC})$$

which is a first order approximation.

Figure 19 illustrates the power dissipation in the external power transistor for both sides. Maximum power dissipation occurs between full load and short circuit so the heat sink for the 2N3772 must be designed accordingly, remembering that

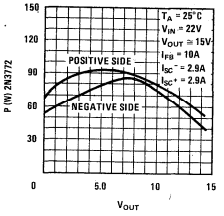



**FIGURE 19. Power Dissipation in the External Pass Transistor (Q5, Q7)**

the 2N3772 must be derated according to 0.86W/°C above 25°C. This corresponds to a thermal resistance junction to case of 1.17°C/W.

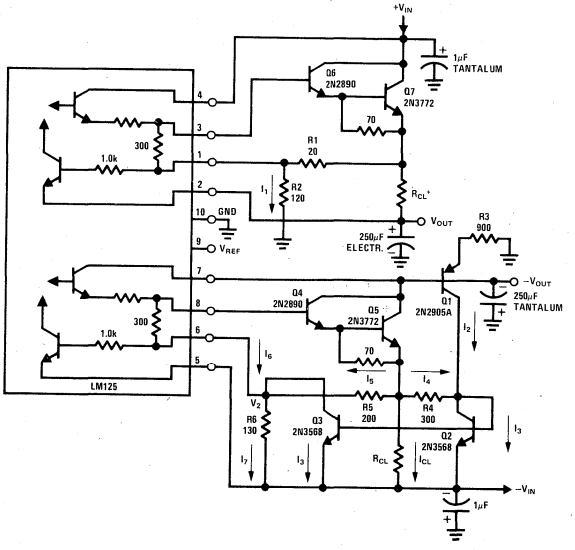



**FIGURE 18. 10A Regulator with Foldback Current Limiting**

**Example**

| Positive Side | Theoretical Value | Experimental Results |
|---|---|---|
| $I_{FB}$ = 10 A | $I_{125}$ = 13 mA | $I_{FB}$ = 9.8 A |
| $I_{SC}$ = 2.5 A | $P_{LM125}$ = 150 mW | $I_{SC}$ = 2.9 A |
| $V_{IN}$ = 22V | $R_{CL}^+$ = 0.26Ω | $R_{CL}^+$ = 0.26Ω |
| $V_{OUT}$ = 15V | R1 = 21Ω | R1: adjusted to 20Ω |
| $\beta = \beta 1\, \beta 2$ = 15 X 50 = 750 min | R2 = 130Ω | R2: adjusted to 120Ω |
| $T_A$ = 25°C | $V_{SENSE}^+$ = 650 mV | |

| Negative Side | Theoretical Value | Experimental Results |
|---|---|---|
| $I_{FB}$ = 10 A | $R_{CL}^-$ = 0.22Ω | $I_{FB}$ = 10 A |
| $I_{SC}$ = 2.5 A | R4 = 300Ω | $I_{SC}$ = 2.9 A |
| $V_{IN}$ = 22V | R5 = 200Ω | $R_{CL}^-$: adjusted to 0.3Ω |
| $V_{OUT}$ = 15V | R6 = 150Ω | R6: adjusted to 130Ω |
| $\beta$ = 800 | R3 = 1.6 kΩ | R3: adjusted to 900Ω |
| $T_A$ = 25° | $V_{SENSE}^-$ = 550 mV | |
| $\frac{I_4}{I_5} = \frac{2}{3}$ | | |

**Note:** For this example, in designing each side, the power dissipation of the opposite side has not been taken into the account.

## POSITIVE CURRENT DEPENDENT SIMULTANEOUS CURRENT LIMITING

The LM125/LM126/LM126 uses the negative output as a reference for the positive regulator. As a consequence, whenever the negative output current limits, the positive output follows tracks to within 200 – 800 mV of ground. If, however, the positive regulator should current limit the negative output will remain in full regulation. This imbalance in output voltages could be a problem in some supply applications.

As a solution to this problem, a simultaneous limiting scheme, dependent on the positive regulator output current, is presented in Figure 20. The output current causes an I-R drop across R1 which brings transistor Q1 into conduction. As the positive load current increases $I_1$ increases until the voltage drop across R2 equals the negative current limit sense voltage. The negative regulator will then current limit, and positive side will closely follow the negative output down to a level of 700 – 800 mV. For $V_{OUT}^+$ to drop the final 700 – 800 mV with small output current change, $R_{CL}^+$ should be adjusted so that the positive current limit is slightly larger than the simultaneous limiting. Figure 21 illustrates the simultaneous current limiting of both sides.

The following design equations may be used:

$$R1\, I_{CL}^+ = R3\, I_1 + V_{BEQ1} \tag{25}$$

$$I_1 = \frac{V_{SENSE}^-}{R2} \tag{26}$$

Combining (25) and (26),

$$I_{CL}^+ = \frac{\frac{R3}{R2} V_{SENSE}^- + V_{BEQ1}}{R1} \tag{27}$$

with

$$R_{CL}^+ = \frac{V_{SENSE}^+}{1.1\, I_{CL}^+} \tag{28}$$

The negative current limit (independent of $I_{CL}^+$) can be set at any desired level.

$$I_{CL}^- = \frac{V_{SENSE}^- + V_{DIODE}}{R_{CL}^-} \tag{29}$$

Transistor Q2 turns off the negative pass transistor during simultaneous current limiting.

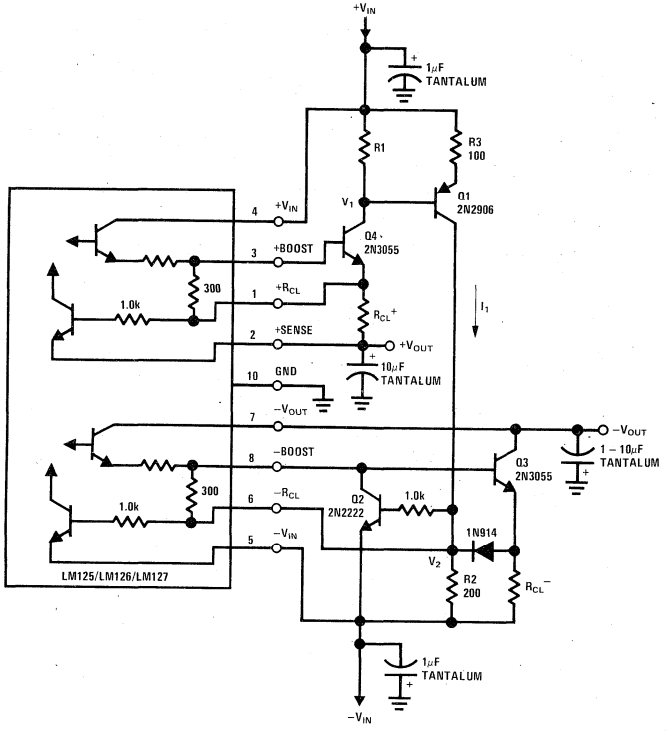



**FIGURE 20. Positive Current Dependent Simultaneous Current Limiting**

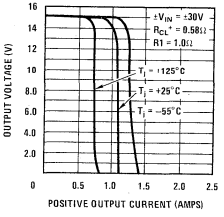



**FIGURE 21. Positive Current Dependent Simultaneous Shutdown**

## ELECTRONIC SHUTDOWN

In some regulated supply applications it is desirable to shutdown the regulated outputs ($\pm V_O = 0$) without having to shutdown the unregulated inputs (which may be powering additional equipment). Various shutdown methods may be used. The simplest is to insert a relay, a saturated bipolar device, or some other type switch in series with either the regulator inputs or outputs. The switch must be able to open and close under maximum load current which, may be several amps.

As an alternate solution, the internal reference voltage of the regulator may be shorted to ground. This will force the positive and negative outputs to approximately +700 mV and +300 mV respectively. Both outputs are fully active so the full output current can still be supplied into a low impedance load. If this is unacceptable, another solution must be found.

The circuit in Figure 22 provides complete electronic shutdown of both regulators. The shutdown control signal is TTL compatible but by adjusting R8 and R9 the regulator may be shutdown at any desired level above 2 $V_{BE}$, calculated as follows:

$$V_T \simeq \left[\frac{R8}{R3\,\beta\,Q4} + \frac{R9}{R3}\right] V_{BE} + 2\,V_{BE} \qquad (30)$$

Positive and negative shutdown operations are similar. When a shutdown signal $V_T$ is applied, Q4 draws current through R3 and D2 establishing a voltage $V_R$ which starts the current sources Q1 and Q2. Assuming that Q1 and Q2 are matched, and making R1 = R2 = R3, the currents $I_1$, $I_2$, $I_3$ are equal and both sides of the regulator shutdown simultaneously.

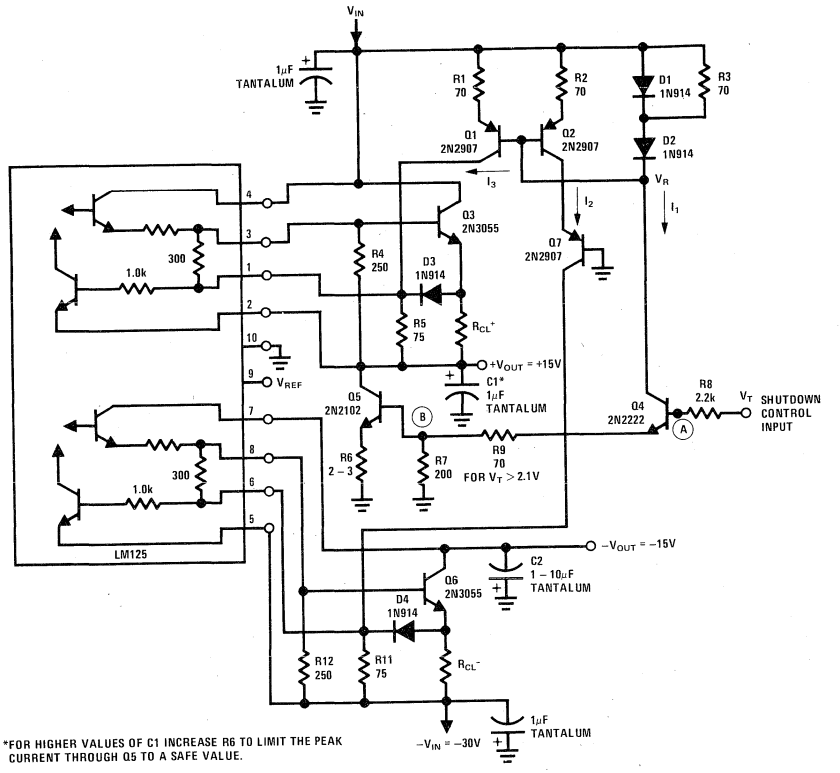



**FIGURE 22. Electronic Shutdown for the Boosted Regulator**

The current $I_3$ creates a drop across R5, which equals or exceeds the limit sense voltage of the positive regulator, causing it to shutdown. Since $I_3$ has no path to ground except through the load, a fixed load is provided by Q5, which is turned on by the variable current source Q4. C1 also discharges through Q5 and current limiting resistor R6. Resistor R4 prevents Q3 turn on during shutdown, which could otherwise occur due to the drop across R5 plus the internal 300Ω resistor. Diode D3 prevents $I_3$ from being shunted through $R_{CL}$.

C2 discharges through the load. Q7 shares the total supply voltage with Q2, thus limiting power dissipation of Q2. Another power dissipation problem may occur when the design is done for $V_T$ = 2.0V for example, and $V_T$ is increased above the preset threshold value. $I_1$ is increased and Q4 has to dissipate $(V_{IN} - 3\ V_{BE} - V_T)\ I_1$ (W). The simplest solution is to increase R8. If this is insufficient, a set of diodes may be added between nodes A and B to clamp. $I_1$ to a reasonable value. This is illustrated in Figure 23:

$$I_1 = \frac{V_{R9}}{R9} \simeq \frac{V_T - V_{BE} - \left[V_T - 2\,V_{BE}\right]}{R9}$$

$$= \frac{V_{BE}}{R9}$$

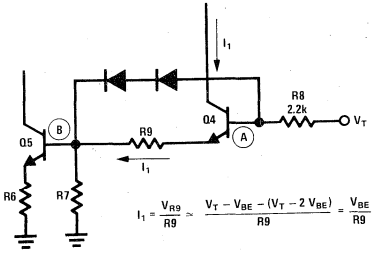



**FIGURE 23.**

So $I_1$ is made independent of $V_T$ and by setting a minimum value of 10 mA (R9 = 70Ω). The regulator will shutdown at any desired level above 3 $V_{BE}$, without overheating transistor Q4. Also using

Figure 23 the diode D1 in Figure 22 may be omitted. The shutdown characteristics of Figure 22 are shown in Figure 24.

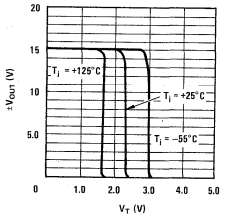



**FIGURE 24. Electronic Shutdown Characteristics**

The normal current limiting current is set by equation (31)

$$I_{CL} = \frac{V_{SENSE} + V_{DIODE}}{R_{CL}} \qquad (31)$$

The same approach is used with the unboosted regulator shown in Figure 25. In this case the voltage sense resistor is the internal 300Ω one. Since output capacitors are no longer required Q3 is just used as a current sink and its emitter load has been removed.

## POWER DISSIPATION

The power dissipation of the LM125 is:

$$P_d = (V_{IN}^+ - V_{OUT}^+)\, I_{OUT}^+ + (V_{IN}^- - V_{OUT}^-)\, I_{OUT}^- + V_{IN}^+ I_S^+ + V_{IN}^- I_S^-$$

where $I_S$ is the standby current.

Ex: ±1A regulator using 2N3055 pass transistors. Assuming a $\beta$ = 100, and ±25V supply,

$$P_d = 400 \text{ mW}.$$

The temperature rise for the TO-5 package will be:

$$T_{RISE} = 0.4 \times 150^\circ\text{C/W} = 60^\circ\text{C}$$

Therefore the maximum ambient temperature is $T_{AMAX} = T_{jMAX} - T_{RISE} = 90^\circ$C. If the device is to operate at $T_A$ above 90°C then the TO-5 package must have a heat sink. $T_{RISE}$ in this case will be:

$$T_{RISE} = P_d\,(\theta_{J\text{-}C} + \theta_{C\text{-}S} + \theta_{S\text{-}A}).$$

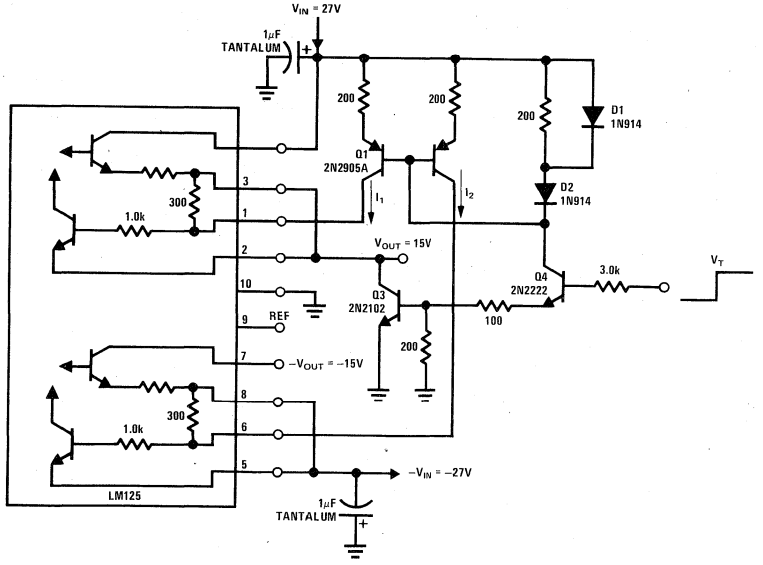



**FIGURE 25. Electronic Shutdown for the Basic Regulator**

Interface Development Group
JUNE 1973

# COMPARING THE HIGH SPEED COMPARATORS

## INTRODUCTION

Several integrated circuit voltage comparators exist which were designed with high speed and complementary TTL outputs as the main objectives. The more common applications for these devices are high speed analog to digital (A to D) converters, tape and disk-file read channels, fast zero-crossing detectors, and high speed differential line receivers. This note compares the National Semiconductor devices to similar devices from other manufacturers.

The product philosophy at National was to create pin-for-pin replacement circuits that could be considered as second-sources to the other comparators, while simultaneously containing the improvements necessary to make a more optimum device for the intended usage. Optimized parameters include speed, input accuracy and impedance, supply voltage range, fanout, and reliability. The LM160/LM260/LM360 are replacement devices for the μA760, while the LM161/LM261/LM361 replace the SE/NE529. Tables I and II compare the critical parameters of the National commercial range devices to their respective counterparts.

## SPEED

Throughout the universe the subject of speed must be approached with caution; the same holds true here. Speed (propagation delay time) is a function

**TABLE I. LM360/μA760C Comparison** $0^\circ \leq T_A \leq +70^\circ C$, $V^+ = +5.0V$, $V^- = -5.0V$

| PARAMETER | LM360 | μA760C | UNITS |
|---|---|---|---|
| Input Offset Voltage | 5.0 | 6.0 | mV max |
| Input Offset Current | 3.0 | 7.5 | μA max |
| Input Bias Current | 20 | 60 | μA max |
| Input Capacitance | 4.0 | 8.0 | pF typ |
| Input Impedance | 17 | 5.0 | kΩ typ @ 1 MHz 25°C |
| Differential Voltage Range | ±5.0 | ±5.0 | V typ |
| Common Mode Voltage Range | ±4.0 | ±4.0 | V typ |
| Gain | 3.0 | 3.0 | V/mV typ 25° |
| Fanout | 4.0 | 2.0 | 74 Series TTL Loads |
| Propagation Delays: | | | |
| (1) 30 $mV_{P-P}$ 10 MHz Sinewave in | 25 | 30 | ns max 25° |
| (2) 2.0 $V_{P-P}$ 10 MHz Sinewave in | 20 | 25 | ns max 25° |
| (3) 100 mV Step + 5.0 mV Overdrive | 14 | 22 | ns typ 25° |

**TABLE II. LM261/NE529 Comparison** $0^\circ \leq T_A \leq +70^\circ C$, $V^+ = +10V$, $V^- = -10V$, $V_{CC} = +5.0V$

| PARAMETER | LM261 | NE529 | UNITS |
|---|---|---|---|
| Input Offset Voltage | 3.0 | 10 | mV max |
| Input Offset Current | 3.0 | 15 | μA max |
| Input Bias Current | 20 | 50 | μA max |
| Input Impedance | 17 | 5.0 | kΩ typ @ 1 MHz 25°C |
| Differential Voltage Range | ±5.0 | ±5.0 | V typ |
| Common Mode Voltage Range | ±6.0 | ±6.0 | V typ |
| Gain | 3.0 | 4.0 | V/mV typ 25° |
| Fanout | 4.0 | 6.0 | 74 Series TTL Loads |
| Propagation Delay – 50 mV Overdrive | 20 | 22 | ns max 25° |

of the measurement technique. The earlier "standard" of using a 100 mV input step with 5.0 mV overdrive has given way to seemingly endless variations. To be meaningful, speed comparisons must be made with identical conditions. It is for this reason that the speed conditions specified for the National parts are the same as those of the parts replaced.

Probably the most impressive speed characteristic of the six National parts is the fact that propagation delay is essentially independent of input overdrive (Figure 1); a highly desirable characteristic in A to D applications. Their delay typically

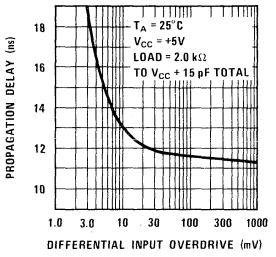



**FIGURE 1. Delay vs Overdrive**

varies only 3 ns for overdrive variations of 5.0 mV to 500 mV, whereas the other parts have a corresponding delay variation of two to one. As can be seen in Tables I and II, the National parts have an improved maximum delay specification. Further, the 20 ns maximum delay is meaningful since it is specified with a representative load: a 2.0 kΩ resistor to +5.0V and 15 pF total load capacitance. Figure 2 shows typical delay variation with temperature.

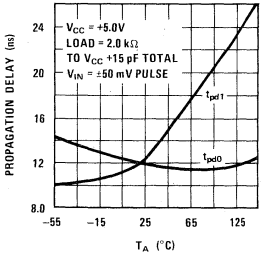



**FIGURE 2. Delay vs Temperature**

## INPUT PARAMETERS

The A to D, level detector, and line receiver applications of these devices require good input accuracy and impedance. In all these cases the differential input voltage is relatively large, resulting in a complete switch of input bias current as the input signal traverses the reference voltage level. This effect can give rise to reduced gain and threshold inaccuracy, dependent on input source impedances and comparator input bias currents. Tables I and II show that the National parts have a substantially lower maximum bias current to ease this problem. This was done without resorting to Darlington input stages whose price is higher offset voltages and longer delay times. The lower bias currents also raise input resistance in the threshold region. Lower input capacitance and higher input resistance result in higher input impedance at high frequencies.

Even with low source impedances, input accuracy is still dependent on offset voltage. Since none of the devices under discussion has internal offset null capability, ultimate accuracy was improved by designing and specifying lower maximum offset voltage. Refer to Figure 3 for typical offset voltage drift with temperature.

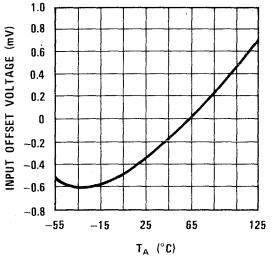



**FIGURE 3. Offset Temperature Coefficient**

## OTHER PERFORMANCE AREAS

In the case of the LM160/LM260/LM360, fanout was doubled over the previous device. For the LM161/LM261/LM361, operating supply voltage range was extended to ±15V op amp supplies

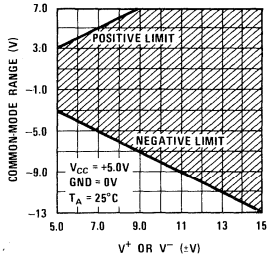



**FIGURE 4. LM161 Common Mode Range**

which are often readily available where such a comparator is used. Figure 4 reveals the common mode range of the latter device.

The performance improvements previously mentioned were a result of circuit design (Figures 5 and 6) and device processing. Schottky clamping, which can give rise to reliability problems, was not used. Gold doping, which results in processing dependent speeds and low transistor beta, was not used. Instead a non-gold-doped process with high breakdown voltage, high beta, and high $f_T$ ($\approx$ 1.5 GHz) was selected which produced remarkably consistent performance independent of normal process variation. The higher breakdown voltage allows the LM161/LM261/LM361 to operate on ±15V supplies and results in lower transistor capacitance; higher beta provides lower input bias currents; and higher $f_T$ helps reduce propagation time.

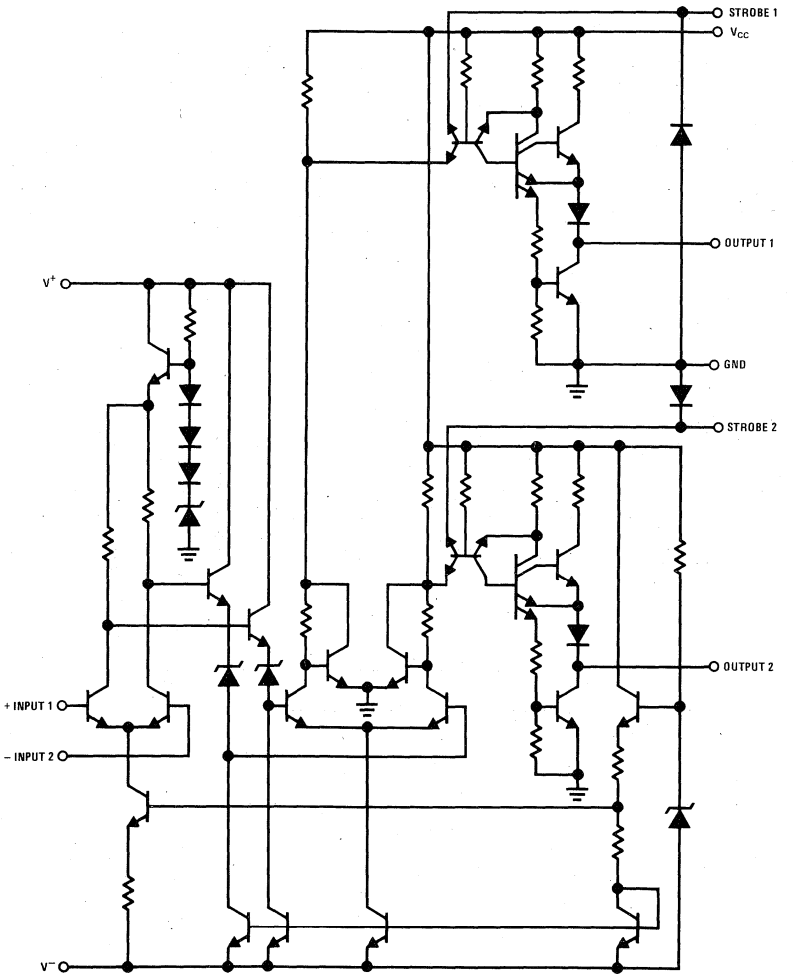



**FIGURE 5. LM161 Schematic Diagram**

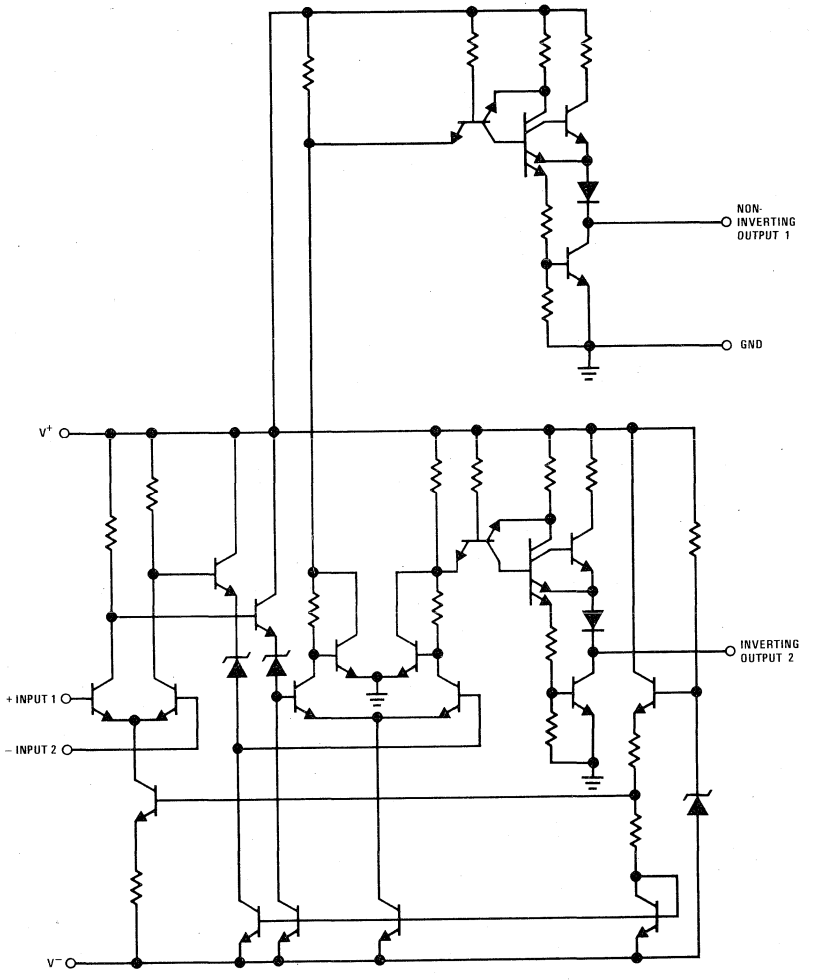



FIGURE 6. LM160 Schematic Diagram

## APPLICATIONS

Typical applications have been mentioned previously. The LM160 and LM161 may be combined as in Figure 7 to create a fast, accurate peak detector for use in tape and disk-file read channels. A 3-bit A to D converter with 21 ns typical conversion time is shown in Figure 8. Although primarily intended for interfacing to TTL logic, direct connection may be made to ECL logic from the LM161 by the technique shown in Figure 9. When used this way the common mode range is shifted from that of the TTL configuration. Finally level detectors or line receivers may be implemented with hysteresis in the transfer characteristic as seen in Figure 10.

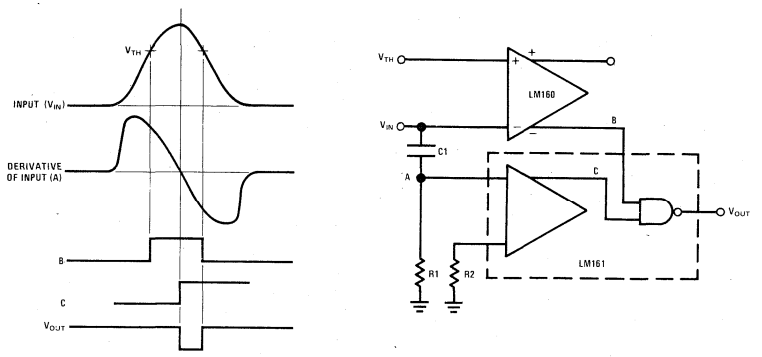



**FIGURE 7. Peak Detector**

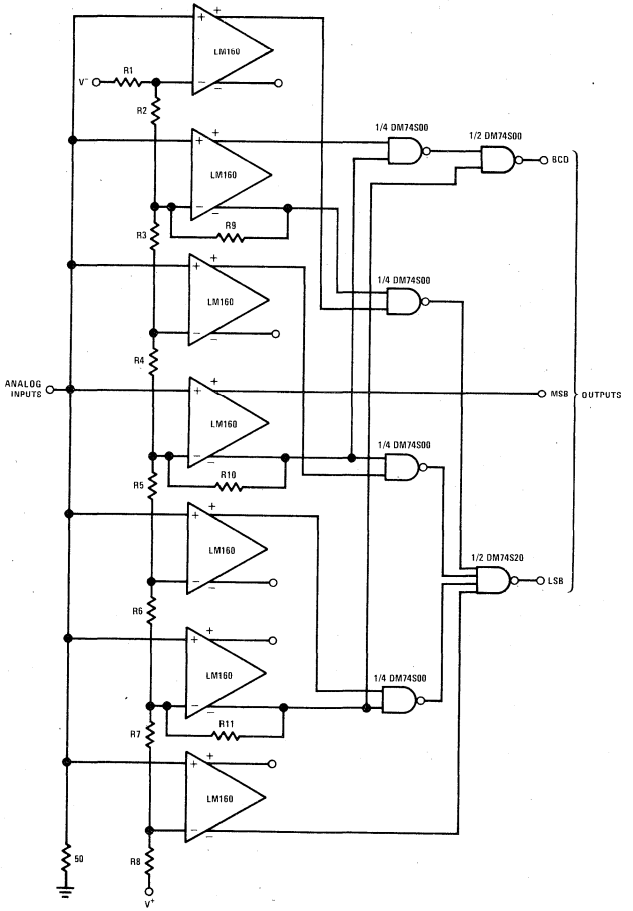



**FIGURE 8. High Speed 3-bit A to D Converter**

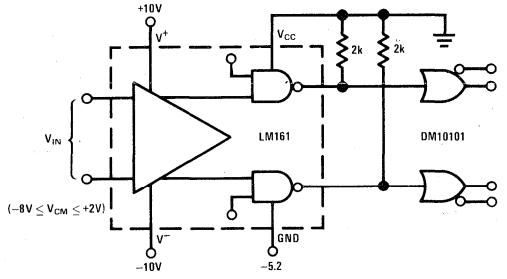
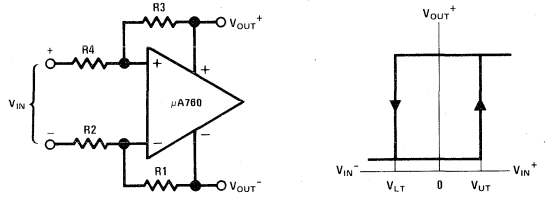



**FIGURE 9. Direct Interfacing to ECL**




$$V_{UT} = V_{OH}\left(\frac{R2}{R1}\right) - V_{OL}\left(\frac{R4}{R3}\right)$$

$$V_{LT} = V_{OL}\left(\frac{R2}{R1}\right) - V_{OH}\left(\frac{R4}{R3}\right)$$

**FIGURE 10. Level Detector with Hysteresis**

Gene Taatjes
JULY 1973

## CMOS LINEAR APPLICATIONS

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. Figure 1 shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristic as shown in Figure 1.

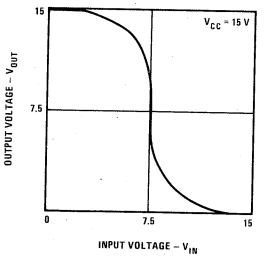



**FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter.**

Under AC conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. Figure 2 shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

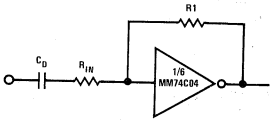



**FIGURE 2. A 74CMOS Invertor Biased for Linear Mode Operation.**

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.

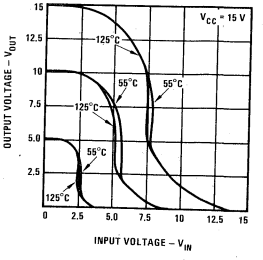



**FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier.**

Figure 3 shows typical voltage characteristics of each inverter at several values of the $V_{CC}$. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self biased inverter with supply voltage is shown in Figure 4. When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

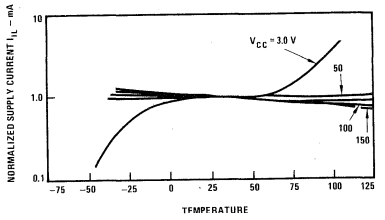



**FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics.**

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or dual supply.

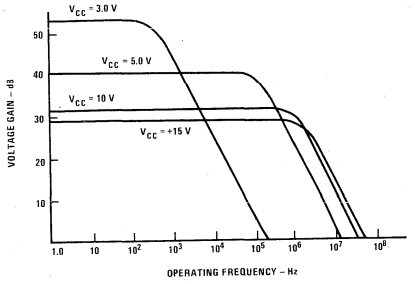



**FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in Figure 2.**

## APPLICATIONS

### Cascading Amplifiers for Higher Gain.

By cascading the basic amplifier block shown in Figure 2 a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in Figure 6) a higher open loop gain is achieved which results in more accurate closed loop gains.

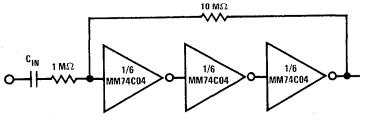



**FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier.**

### Post Amplifier for Op Amps.

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in Figure 7 is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

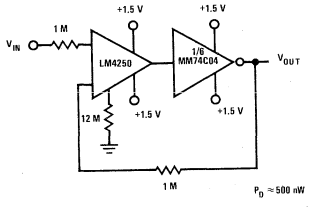



**FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp.**

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in Figure 8, the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.

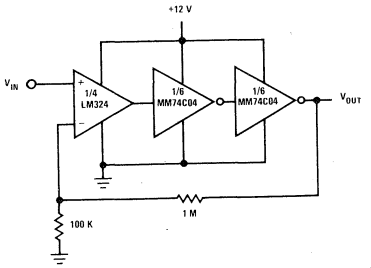



**FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324.**

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA

from the $V_{CC}$ supply while the MM74C02 will supply approximately 10 mA from the negative supply. Shown in Figure 9 is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.

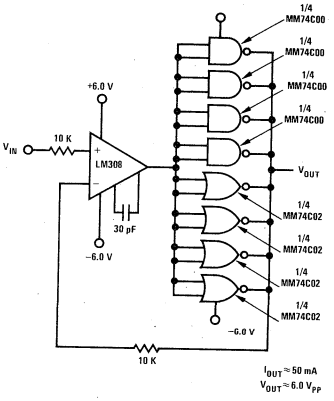



**FIGURE 9. MM74C00 and MM74C02 Used as a Post Amplifier to Provide Increased Current Drive.**

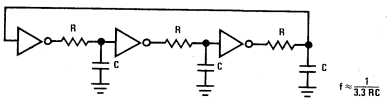
### Other Applications.

Shown in Figure 10 is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

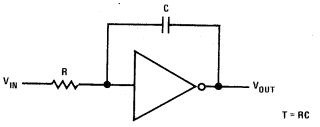
### Conclusion

Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

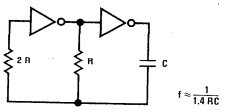
Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.



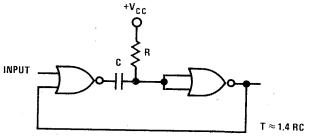

**Phase Shift Oscillator Using MM74C04**



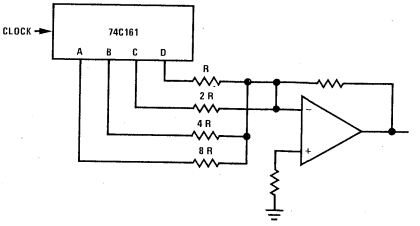

**Integrator Using Any Inverting CMOS Gate**




**Square Wave Oscillator**




**One Shot**




**Staircase Generator**

**FIGURE 10. Variety of Circuit Ideas Using CMOS Devices.**

Carl Nelson
DECEMBER 1973

# VERSATILE TIMER OPERATES FROM MICROSECONDS TO HOURS

## INTRODUCTION

Timing functions, until recently, have been somewhat neglected by integrated circuit manufacturers. The primary reason was the extremely wide range of input and output signals currently incorporated in discrete designs. In addition, power supply voltages varied over a ten to one range and timing periods were as short as microseconds and as long as hours.

The LM122 timer has been designed to operate over a very wide range of input/output signal levels, supply voltages, and timing periods. It will replace most discrete designs with improved performance and reliability. This new timer overcomes many of the problems incurred in discrete or early IC designs.

First, it locks out trigger signals during the timing period to guarantee a precise output regardless of trigger level — while maintaining the ability to be retriggered almost immediately following the end of the timing pulse. (Duty cycles up to 99.9% can be achieved). Secondly, the timing period is free from jitter caused by supply fluctuations because the timing components are driven from an internal regulated source. Supply voltage for the timer can vary from 4.5V to 40V even during the timing period! An additional feature is the ±40V excursion allowed on the trigger input and the 40V/50 mA drive capability of the output transistor. These two specifications allow the LM122 to interface directly to present designs without level shift or power boosting problems. Finally, the LM122 will generate stable timing periods from several microseconds to hours—a useful range of eight decades. Worst case guarantees on comparator bias current and threshold level allow the user to easily select timing components for maximum accuracy.

## CIRCUIT DESCRIPTION

The LM122 circuitry can be divided into five separate sections: output stage, bias network, voltage regulator, comparator, and logic. These sections are grouped on the schematic in Figure 1 to simplify understanding of the timer.

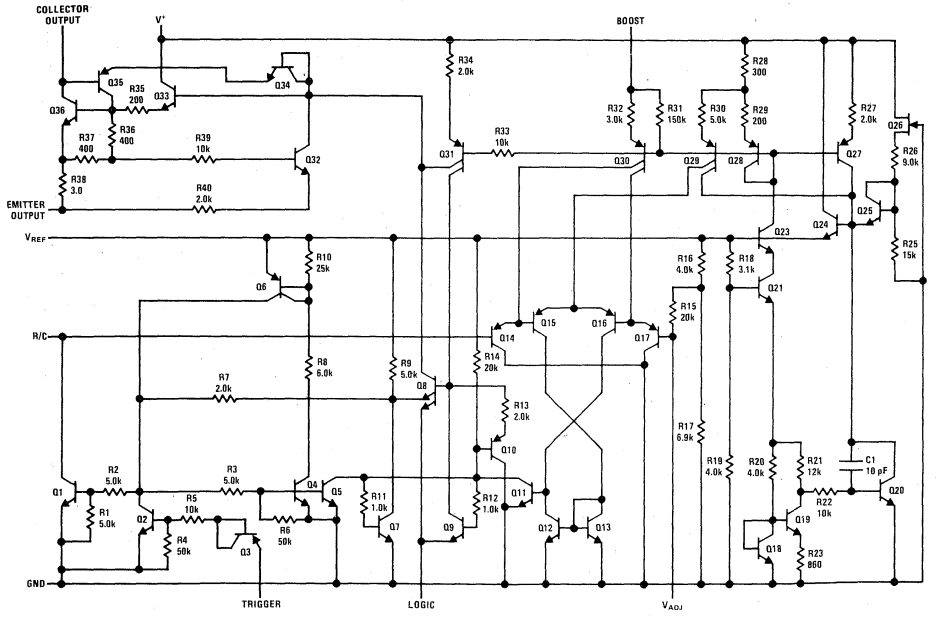



**FIGURE 1. Schematic Diagram**

The floating transistor output stage of the LM122 consists of Q32 through Q36. Q36 is the actual output transistor and is driven by emitter follower, Q33. Q34 and Q35 are antisaturation clamps to reduce stored charge in Q36 and to limit current through Q33. Q32 acts as a current limiter with the limit set at about 120 mA.

The regulator built into the LM122 is a $V_{BE}/\Delta V_{BE}$* type with a typical output voltage of 3.15V at up to 5.0 mA load current. Q18 and Q19 generate a 100$\mu$A current through Q19 which has a positive temperature coefficient of 0.33%/°C. This generates 1.2V and +4 mV/°C TC across R21. When added to the base emitter diode voltages of Q20 and Q21, a 2.4V, zero TC reference is established at the base of Q21. R18 and R19 form a divider to raise the regulated voltage to 3.15V. (This particular voltage was chosen because it can be operated off a single 5.0V supply and because one RC time constant is exactly 2.0V out of 3.15V.) Q23 buffers Q21 from supply fluctuations and sets up the currents for the bias section of the timer. Q20 is a single stage of voltage gain for the regulator. It is buffered by the series pass transistor, Q24. Q25, Q26, R25, and R26 are included for starting purposes and do not affect operation once current is flowing in the regulator section.

The function of the comparator is to cause an output change of state when the timing capacitor has charged to one RC time constant. Q11 through Q17 perform this function. Q14, Q15, Q16, and Q17 are a Darlington differential stage driving an active load formed by Q12 and Q13. Q11 is a second stage operating as a common emitter amplifier with R14 as its load resistor. For long timing intervals, the Darlington is run with no bleed current from Q30. Operating current for Q15 and Q16 is about 5$\mu$A per side. The specially processed lateral PNP's have $h_{FE}$'s of about 200, so operating current for Q14 and Q17 is typically 25 nA. At these current levels, the substrate PNP's have $h_{FE}$'s of 80, giving comparator input currents of 300 pA! One side of the comparator is tied to a divider (R16 and R17) which is set at 63.2% of the reference voltage — one RC time constant. The other side is connected to the external timing resistor and capacitor.

The logic section of the LM122 performs four functions: first, it provides a latching action to make the circuitry immune to retriggering during the timing interval; second, it simulates the action of an exclusive OR gate to generate a logic reverse function; additionally, it translates the low level output from the comparator to the high level swing needed to drive the floating transistor output; and finally, it drives the discharge transistor to reset the timing capacitor. Q2 and Q3 makeup the TTL compatible trigger input to the logic section. Q3 is a lateral PNP with 60V reverse emitter-base breakdown voltage, allowing negative inputs as high as −40V without harm to the chip. R5 is an epitaxial resistor which pinches off at 30V and has a breakdown of 80V. This allows positive input voltages of up to 40V on the trigger terminal even when operating the timer from a supply voltage of only 5.0V. Typical current drawn by the trigger terminal is 40$\mu$A at 2.0V and 600$\mu$A at 40V. Q4 and Q6 form a latch which self-limits at about 400$\mu$A and can be turned off by Q2. Q5 and Q7 interface the latch to the comparator so that the comparator can fire the latch at the end of the timing period. Q8, Q9, and Q10 perform the level shifting required to drive the output transistor and double as an exclusive OR gate, with the emitters of Q8 and Q9 as one input and the collectors of Q5 and Q11 as the second input. Grounding the Q8 and Q9 emitters reverses the effect of a signal appearing at the collector of Q11.

Biasing for the various circuits in the timer is generated by a string of PNP current sources consisting of Q27 through Q31. Current levels are established by the constant current source, Q23, driving diode connected Q28. The current from Q23 is 400$\mu$A, setting the drop across the emitter resistor, R28 plus R29, at 200 mV. Q29 delivers 10$\mu$A to the comparator and Q31 supplies a total of 100$\mu$A to the output transistor and logic circuitry. Part of Q29's collector is returned to Q27 to avoid having to use a large value resistor for R30. Q30 is completely off when using the timer for long timing periods. Shorting the boost terminal to $V^+$ adds about 5$\mu$A bleed current at the emitters of Q14 and Q17. This extra current is needed to slew the emitters of the comparator for timing periods less than 1 ms.

## DESCRIPTION OF PIN FUNCTIONS

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

$V^+$ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing on $V^+$ is not generally needed but may be necessary when driving highly reactive loads. Quiescent current drawn from the $V^+$ terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The $V_{REF}$ pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to $V_{REF}$, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in

*See AN-42, "On Card Regulator for Logic Circuits"

applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature controllers. Typical temperature drift of the reference is less than 0.01%/°C.

The trigger terminal is used to start timing. Threshold is typically 1.6V at +25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the trigger source is typically 20μA at threshold, rising to 600μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region.

If the trigger terminal is held high as the timing period ends, the output pulse will appear normally, but the timing capacitor will not be discharged. This is a necessary circuit action to prevent repetitive cycles when the trigger is held high. After the timing period, the capacitor is discharged when the trigger decreases below the threshold, without affecting the output.

The R/C pin is tied to the uncommitted side of the comparator and to the collector of the capacitor discharge transistor. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). The internal discharge transistor turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the R/C pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Input current to the R/C pin is typically 300 pA when the voltage is negative with respect to the $V_{ADJ}$ terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is 30 nA. Gain of the comparator is very high, 200,000 or more depending on the state of the logic reverse pin and the connection of the output transistor.

The ground pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the $V^+$ terminal. Level shifting may be necessary for the input trigger if the trigger voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the ground terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the ground pin of the LM122 was tied to a negative supply.

The terminal labeled $V_{ADJ}$ is tied to one side of the comparator and to a voltage divider between $V_{REF}$ and ground. The divider voltage is set at 63.2% of $V_{REF}$ with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to $V_{ADJ}$. This resistor is a pinched type with a typical variation in absolute value of ±100% and a TC of 0.7%/°C. For this reason, external signals (typically a pot between $V_{REF}$ and ground) connected to $V_{ADJ}$ should have a source resistance as low as possible. For small changes in $V_{ADJ}$, up to several kΩ is all right, but for large variations 250Ω or less should be maintained. This can be accomplished with a 1.0k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on $V_{ADJ}$ from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The $V_{ADJ}$ pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high when the $V_{ADJ}$ pin is grounded. In this case, the output changes state, but the capacitor does not discharge. If the trigger drops while $V_{ADJ}$ is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when $V_{ADJ}$ is released, the output may or may not change state, depending the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output.

In noisy environments or in comparator-type applications, a bypass capacitor on the $V_{ADJ}$ terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The emitter and the collector outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the emitter is tied to the ground pin and the signal is taken from the collector, or the collector is tied to $V^+$ and the signal is taken from the emitter. Variations on these basic connections are possible. The collector can be tied to any positive voltage up to 40V when the signal is taken from the emitter. However, the emitter will not be pulled higher than the supply voltage on the $V^+$ pin. Connecting the collector to a voltage less than the $V^+$ voltage is allowed. The emitter should not be connected to a hard source other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with collector-emitter voltages up to 40V. The power time product, however, must not exceed 15 watt·seconds

for power levels above the maximum rating of the package. A short to 30V, for instance, can not be held for more than 4 seconds. These levels are based on a 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A boost pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current. For short time intervals where low input current is not needed, comparator operating current can be increased several orders of magnitude for fast operation. Shorting the boost terminal to $V^+$ increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5.0μA.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used.

The "Logic" pin is used to reverse the signal appearing at the output transistor. An open or "high" condition on the logic pin programs the output transistor to be "off" during the timing period and "on" all other times. Grounding the logic pin reverses the sequence to make the transistor "on" during the timing period. Threshold for the logic is typically 150 mV with 150μA flowing out of the terminal. If an active drive to the logic pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum $V_{SAT}$ of 75 mV at 200μA is required. A typical example of active drive to the logic pin is the pulse width discriminator shown in Figure 16.

## CALCULATING WORST CASE TIMING ERROR

Timing errors for the LM122 come from the following sources:

1. Timing ratio error
2. Capacitor saturation voltage
3. Internal switching delays
4. Comparator bias current
5. External resistor and capacitor tolerance
6. Capacitor and board leakage

In general, errors 1 and 5 are the most significant, so they will be treated first.

For most applications, the major contribution to timing error from the LM122 itself is variation in timing ratio, which is the ratio of the comparator threshold voltage (typically 2.0V) to the voltage at the $V_{REF}$ pin. A 1% error in this ratio results in a 1.8% initial timing error. Timing ratio error comes from variations in the internal divider ratio and from offset voltage in the comparator. The LM122 is specified to have a timing ratio from 0.626 to 0.638 at +25°C, giving a ±1.8% worst case contribution to initial timing period error. Over temperature, the worst case figures doubles to ±3.6%. If the initial error is trimmed out externally however, timing error drift due to timing ratio will generally be less than ±0.5% over temperature.

Adding all the contributions to timing error from the LM122 itself will usually give a figure in the 2% to 3% range at +25°C. External timing components ($R_t$ and $C_t$) will normally contribute much more error than this unless selected components are used. ±5% tolerance on $R_t$ and $C_t$ will increase the worst case error to 12% to 13%. By trimming out initial component errors, an exact initial timing period can be obtained, but temperature drift then becomes the limiting factor. For most applications, the contributions to timing period drift due to the LM122 itself will be in the 0.005%/°C to 0.02%/°C range.

If accurate timing over temperature is required, low drift components must be used for $R_t$ and $C_t$. Capacitors are available with temperature coefficients of 100 to 200 ppm/°C. Resistors, at least in the lower ranges, are available with TC's much better than this. Above 1 MΩ, however, care must be used in the selection of a low TC resistor. Units are available up to 100 MΩ with less than 100 ppm/°C drift.

Capacitor saturation voltage is the voltage still remaining on the timing capacitor after it has been reset to as near ground as the internal discharge transistor can drive it. For timing resistors 1 MΩ or greater, this remaining voltage is typically 2.5 mV. For smaller timing resistors, the capacitor saturation voltage can be calculated by the following formula:

$$V_C \approx 2.5\ \text{mV} + \frac{(V_{REF})^* (80\Omega)}{R_t}$$

*$V_{REF}$ = 3.15V

The effect of $V_C$ on timing period is linear at 0.03%/mV. Temperature dependence of $V_C$ is typically +0.2%/°C for $R_t \leq 300k\Omega$, rising to 0.4%/°C for $R_t$ = 10 kΩ. This gives a typical temperature coefficient of timing error *due to* $V_C$ of (0.002) (2.5 mV) (0.03%/mV) = 0.0015%/°C for $R_t \geq 1$ MΩ and (0.004) (24 mV) (0.03%/mV) ≈ 0.003%/°C for $R_t$ = 10 kΩ. Since most applications can use timing resistors in the range of 100 kΩ and up, error *from capacitor saturation voltage* rarely exceeds 0.15% initially, with ±0.05% variation over the full temperature range.

Internal switching delays cause errors which tend to be a fixed time rather than a percentage of the timing period. In the boosted mode this delay is typically 800 ns, and with the boost off; the delay is about 25μs. These times can be added

directly to the calculated timing period for worst case analysis. For timing periods longer than 25 ms, the 25$\mu$s delay gives an error of 0.1% or less. In the range of 1 or 25 ms, error due to delays is 0.1% or less for the boosted mode, rising to a maximum of 4.0% in the unboosted mode. At $\tau$ = 10$\mu$s, delay is the major contribution to timing error ($\approx$ 8%).

Comparator bias current contributes a negligible timing error for all but very long time timing periods. Error can be calculated with a simple formula:

$$\text{Error (\%)} = -50 \cdot R_t \cdot I_b \text{ (Note sign)}$$
$I_b$ = Comparator Bias Current
$R_t$ = Timing Resistor

For $R_t$ = 100 M$\Omega$ and $I_b$ = 0.3 nA (typical) a 1.5% reduction in timing period is incurred. For worst case calculations at +25°C, an $I_b$ of 1 nA maximum is specified in the unboosted mode and 100 nA in the boosted mode. At temperatures below +25°C, these numbers still hold. At +125°C, $I_b$ increases due to leakage to a maximum of ±5 nA unboosted. For worst case calculations below +125°C, the leakage error (5 nA) can be assumed to halve for each 10°C drop below +125°C. At +95°C for instance, the leakage component of $I_b$ would be (5 nA/8) $\approx$ 0.6 nA for a total $I_b$ of 1.6 nA worst case. For the commercial LM322 and LM3905, worst case $I_b$ is 2 nA at +75°C, and for the LM2905 $I_b$ is 2 nA maximum at +85°C. For temperatures between −25°C and +85°C, the TC of $I_b$ is typically 5 pA/°C in the unboosted mode and 100 pA/°C in the boosted mode. For a 100 M$\Omega$ $R_t$, this 5 pA/°C contributes −0.025%/°C to timing period drift.

$$\text{Error (\%/°C)} = (-50)(\Delta I_b/\Delta T)(R_t)$$

For worst case calculations a $\Delta I_b/\Delta T$ ($-25 \leq T_A \leq +85$°C) of 12 pA/°C may be used for the LM122/LM222 and 20 pA/°C for the LM322 and LM2905/LM3905.

External leakage paths may cause timing errors for large values of $R_t$ and high board temperatures. Connections made to the R/C pin should be kept free of dust, moisture, and soldering flux if long time intervals are to be kept accurate. All package types have the R/C pin located between $V_{REF}$ and the ground pin to minimize these leakages.

## DESIGN HINTS

### Eliminating Timing Cycle Upon Initial Application of Power

The LM122 will start a timing cycle automatically (with no trigger input) when $V^+$ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to $V_{REF}$ instead of ground as shown in Figure 2. This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to $V_{REF}$. A 1.0 k$\Omega$ resistor should be included in series with the timing capacitor to limit the surge current load on $V_{REF}$ when the capacitor is discharged.

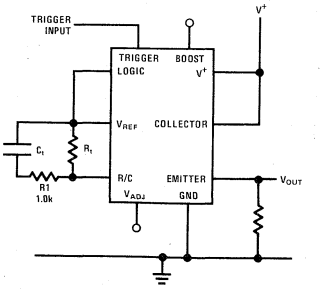



**FIGURE 2. Eliminating Initial Timing Cycle**

### Using Electrolytic Timing Capacitors

Electrolytic capacitors are not usually recommended for timing because of their unstable capacitance and high leakage. For long timing periods (> 10 seconds) at moderate temperatures (0°C to 50°C) however, an electrolytic may be attractive because of its low cost per microfarad Solid tantalum capacitors such as the Kemet* C series T310 (molded epoxy) or T110 (hermetic) are recommended. These units have long term stabilities of 2% to 3% and a temperature coefficient of +0.2%/°C. Selected units are available for timing use with very low leakage.

### Reset Time

The timing capacitor used with the LM122 is reset with an internal transistor which has a collector offset voltage of 2.5 mV @ 1$\mu$A with approximately 80$\Omega$ of collector resistance The time required to reset this capacitor determines the minimum time between timing pulses. An approximate formula for reset time is:

$$\text{Reset Time} = (80\ \Omega)\ (C_t{}^{\dagger})\ (5)$$

$^{\dagger}C_t$ = External timing capacitor.

## NOISY ENVIRONMENTS

The LM122 is relatively insensitive to noise on supply lines and to radiated energy. In *extremely* noisy environments however, it may be necessary to configure the LM122 differently, both to eliminate false triggering and to prevent premature end of a timing period. The circuit "a" shown in Figure 3 has been set up for maximum noise rejection. C1 bypasses the $V_{ADJ}$ pin because of the relatively high impedance ($\approx$ 30 k$\Omega$) of this point. Negative spikes on the $V_{ADJ}$ pin will cause premature end of the timing period. C2 bypasses the supply for rejection of fast transients. R1 sets up the trigger pin to a "normally high" condition. This prevents extremely high electromagnetic fields from triggering the internal flip-flop during a timing period. The input trigger signal is capacitively coupled through C3. Triggering occurs on the *negative* edge of the trigger pulse as shown in the waveform sketch next to Figure 21.

*Manufactured by Union Carbide

If the output voltage from the LM122 can be set up to go "high" during the timing cycle, the alternate connection shown in "b" can be used. Here, the trigger is held high by D2 during the timing period. When the output goes low after the timing period is over, the circuit may be retriggered immediately via D1. R1 and C3 suppress unwanted spikes at the trigger input.

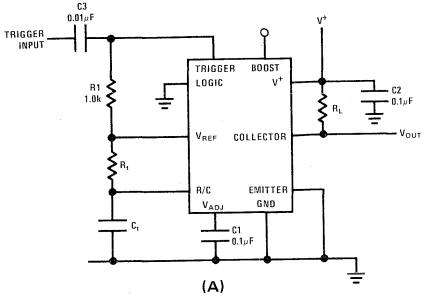



FIGURE 3. Maximum Noise Immunity

## ABORTING A TIMING CYCLE (Figure 4)

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground $V_{ADJ}$
- Raise R/C more positive than $V_{ADJ}$
- Wire "OR" the output

Grounding $V_{ADJ}$ will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving $V_{ADJ}$ to as near ground as possible. Worst case sink current is about 300μA.

A timing cycle may be also ended by a positive pulse to a resistor ($R \leq R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to $V_{ADJ}$ (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.

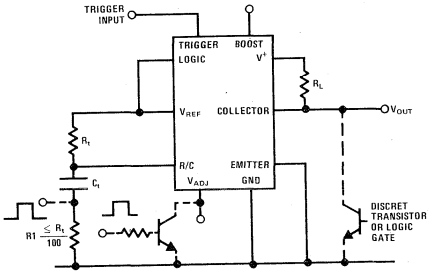



FIGURE 4. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

### Using the LM122 as a Comparator

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the $V_{ADJ}$ terminal with a divider tied to $V_{REF}$. Stability of the reference voltage is typically ±1% over a temperature range of −55°C to +125°C. Offset voltage drift in the comparator is typically 25μV/°C in the boosted mode and 50μV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to ±50V as shown in Figure 5. There is actually no limit on input voltage as long as current is limited to ±1 mA. The resistor shown contributes

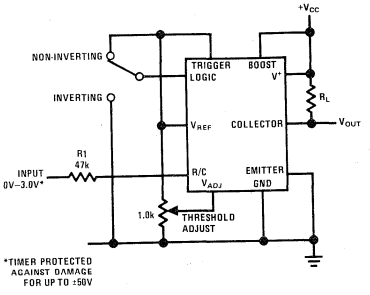



FIGURE 5. Comparator With 0 Volts to 3.0 Volts Threshold

a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply should make this comparator very useful.

### Using Dual Supplies

The LM122 can be operated off dual supplies as shown in Figure 6. The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to $V^-$ or be actually tied to $V^-$ as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "lo" on the trigger pin (with respect to $V^-$) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.

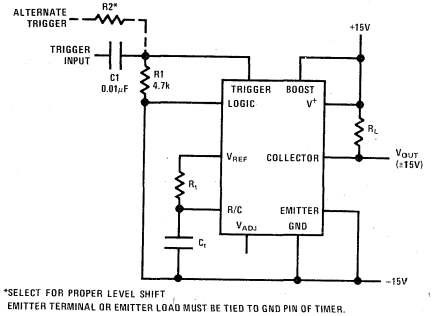
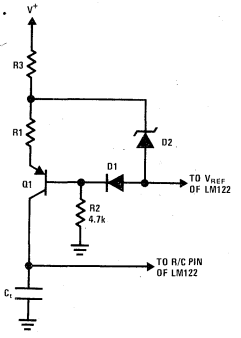



**FIGURE 6. Operating Off Dual Supplies**

## LINEARIZING THE CHARGING SWEEP

In some applications (such as a linear pulse width modulator) it may be desireable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in the accompanying sketch.




Q1 converts the current through R1 to a current source independent of the voltage across $C_t$. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the $V^+$ supply is stable and D1 and R2 can be omitted also if temperature stability if not critical. With D1 and R2 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

## APPLICATIONS

### Basic Timers

Figure 7 is a basic timer using the collector output. $R_t$ and $C_t$ set the time interval with $R_L$ as the load. During the timing interval the output may be

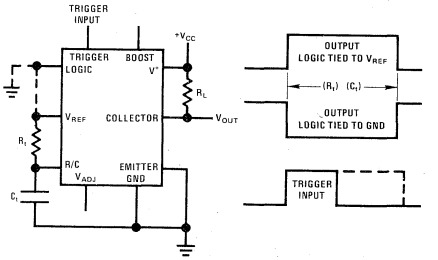



**FIGURE 7. Basic Timer-Collector Output and Timing Chart**

either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch alongside Figure 7.

Figure 8 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.

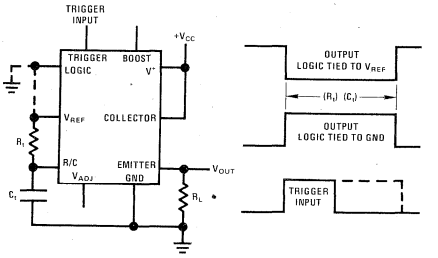



**FIGURE 8. Basic Timer-Emitter Output and Timing Chart**

Figure 9 shows the timer interfacing 5V logic to a high voltage relay. Although the $V^+$ terminal could be tied to the +28V supply, this would be

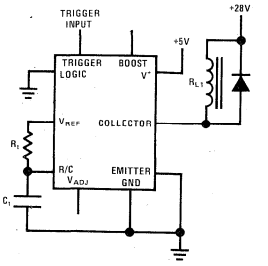



**FIGURE 9. 5 Volt Logic Supply Driving 28 Volt Relay**

an unnecessary waste of power in the IC. In any case, the threshold for the trigger is 1.6V regardless of where $V^+$ is tied.

Figure 10 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. $V_{OUT}$ swings between +5V and ground with a minimum fanout of 5 for medium speed TTL.

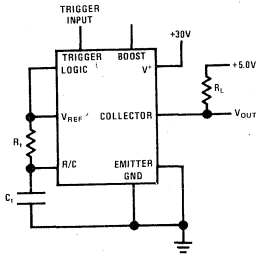



**FIGURE 10. 30 Volt Supply Interfacing to 5 Volt Logic**

Figure 11 is an application where the LM122 is used to simulate a thermal delay relay which

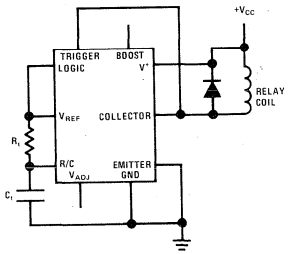



**FIGURE 11. Time Out on Power Up (Relay Energized $R_tC_t$ Seconds After $V_{CC}$ is Applied)**

prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for $R_t$ $C_t$ seconds after $V_{CC}$ is applied, then closes and stays energized until $V_{CC}$ is turned off. Figure 12 is a similar circuit except that the relay is energized

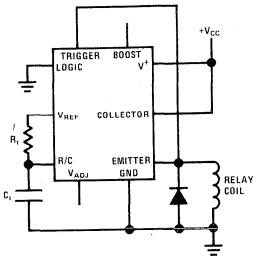



**FIGURE 12. Time Out on Power Up (Relay Energized *Until* $R_tC_t$ Seconds After $V_{CC}$ is Applied)**

as soon as $V_{CC}$ is applied. $R_t$ $C_t$ seconds later, the relay is de-energized and stays off until the $V_{CC}$ supply is recycled.

Figure 13 is a more advanced application of the LM122 as a proportioning temperature controller with optical isolation and synchronized zero crossing features. The timing function is not used. Instead the trigger terminal is held high and the LM122 is used as a high gain comparator with a built in reference. R1 is a thermistor with a −4%/°C temperature coefficient used as the sensor. R2 is used to set the temperature to be controlled by R1. R3 through R8 set up the proportioning action. R3 raises the impedance of the R1/R2 divider so that R5 sees a relatively constant impedance independent of the set point temperature. R6 and R8 reduce the $V_{ADJ}$ impedance so that internal variations in divider impedance do not affect proportioning action. R5 and R7 set

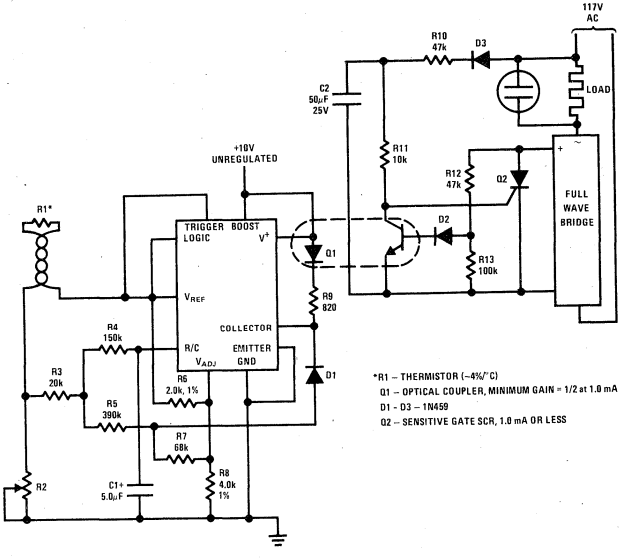



**FIGURE 13. Proportioning Temperature Controller with Synchronized Zero-Crossing**

the actual width of the proportioning band and can be scaled as necessary to alter the width of the band. Larger resistors make the band narrower. The values shown give approximately a 1°C band. R4 and C1 determine the proportioning frequency which is about 1 Hz with the values shown. C1 or R4 can change to alter frequency, but R4 should be between 50k and 500k, and C1 must be a low leakage type to prevent temperature shifts. D1 prevents supply voltage fluctuations from affecting set point or proportioning band. Any unregulated supply between 6V and 15V is satisfactory.

Q1 is an optical isolator with a minimum gain of 0.5. With the values shown for R9, R10, and R11, Q1 is over-driven by at least 3 to 1 to insure deep saturation for reliable turn off of the SCR. Q2 must be a sensitive gate device with a worst case gate firing current of 0.5 mA. R12, R13, and D2 implement the synchronized zero-crossing feature by preventing Q1 from turning off after the voltage across Q2 has climbed above 2.5V. D3, R10, and C2 provide a source of semifiltered dc current for SCR gate drive. D3 and Q2 must have a minimum breakdown of 200V.

Figure 14 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with

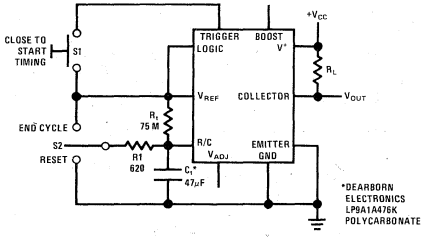



**FIGURE 14. One Hour Timer With Reset and Manual Cycle End**

the appropriate change in output state and discharging of $C_t$, or cause $C_t$ to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released. The average charging current through $R_t$ is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.

Figure 15 is another application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP switch transistor. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω the Thevinin resistance must be connected between $V_{REF}$ and ground with its tap point tied to $V_{ADJ}$.

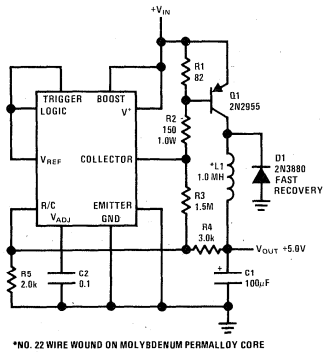



**FIGURE 15. 5 Volt Switching Regulator With 1.0 Amp Output and 5.5 Volt Minimum Input**

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made (Figure 16).

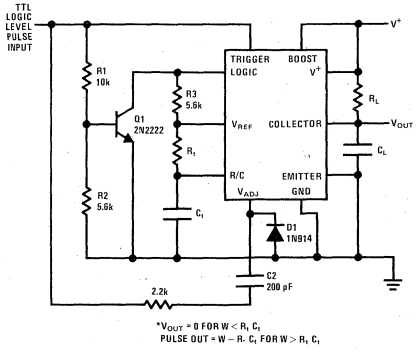



**FIGURE 16. Pulse Width Detector**

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by $R_t$ and $C_t$. The output pulse width is equal to the input trigger width minus $R_t \cdot C_t$. C2 insures no output pulse for short (< RC) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops.

$C_L$ filters the narrow spikes which would occur at the output due to interval delays during switching.

The LM122 can be used as a two terminal time delay switch if an "on" voltage drop of 2V to 3V can be tolerated. In Figure 17, the timer is used to drive a relay "on" $R_t$ $C_t$ seconds after application of power. "off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

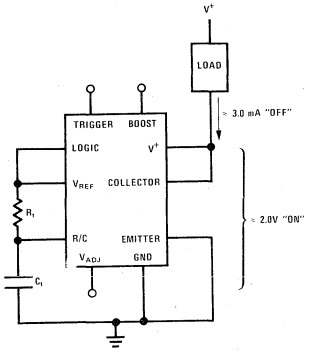



**FIGURE 17. Two-Terminal Time Delay Switch**

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in Figure 18. Pulse width is adjusted with R2 to

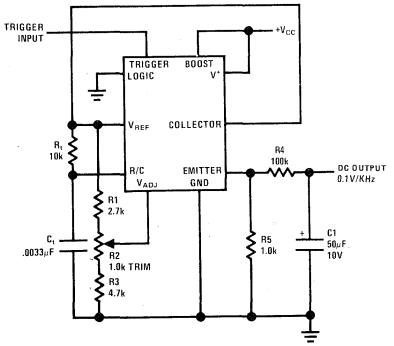



**FIGURE 18. Frequency to Voltage Converter (Tachometer) Output Independent of Supply Voltage**

provide initial calibration at 10 kHz. The collector of the output transistor is tied to $V_{REF}$, giving constant amplitude pulses equal to $V_{REF}$ at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, $(R_t)(C_t)(V_{REF})(f)$. Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

In some applications it is desirable to reduce supply drain to zero between timing cycles. In Figure 19 this is accomplished by using an external PNP as a latch to drive the $V^+$ pin of the timer.

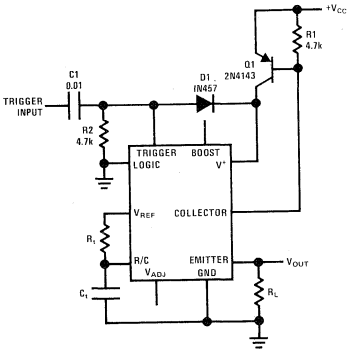
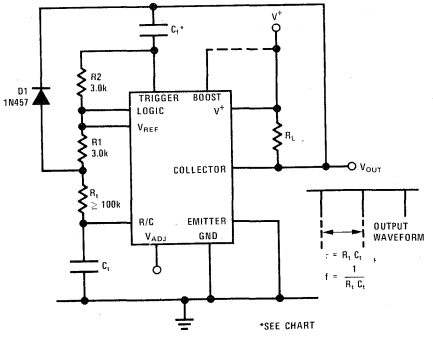



**FIGURE 19. Zero Power Dissipation Between Timing Intervals**

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents coupling back into the trigger signal from the dc load created by the trigger input. If the trigger input is a short pulse, C1 and R2 may be eliminated. $R_L$ must have a minimum value of $(V_{CC})/(2.5\ mA)$.

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capacitor as shown in Figure 20. Operating frequency is $1/(R_t\ C_t)$. The



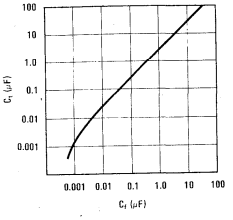




**FIGURE 20. Oscillator**

output is a narrow negative pulse whose width is approximately $2R_2\ C_f$. For optimum frequency

stability, $C_f$ should be as small as possible. The minimum value is determined by the time required to discharge $C_t$ through the internal discharge transistor. A conservative value for $C_f$ can be chosen from the graph included with Figure 20. For frequencies below 1 kHz, the frequency error introduced by $C_f$ is a few tenths of one percent or less for $R_t \gtrsim 500k$.

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally "high" trigger will result in negative edge triggering. In Figure 21, R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with Figure 21 shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual starts of timing is approximately 0.5 to 1.5 R1 C1 depending on the trigger amplitude, or about 2.5 to 7.5μs with the values shown. This time will have to be increased for $C_t$ larger than 0.01μF because $C_t$ is charged to $V_{REF}$ whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

$$C1 \geq \frac{C_t}{10}$$

The LM122 can be connected as a chain of timers quite easily with no interface required. In Figure 22A and 22B, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.

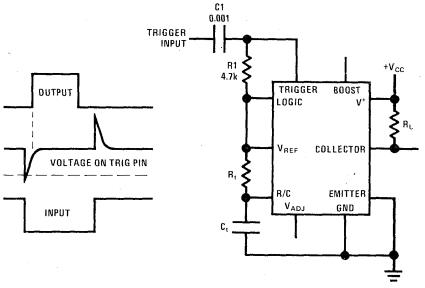



**FIGURE 21. Timer Triggered by Negative Edge of Input Pulse**

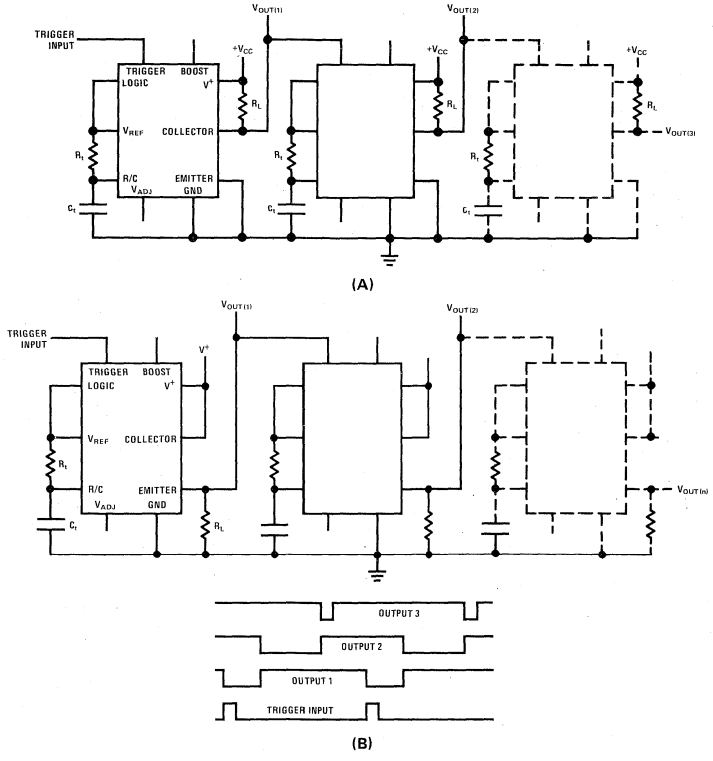
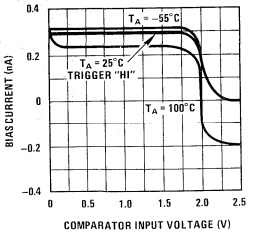


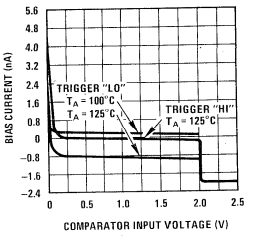

**FIGURE 22. Chain of Timers**

# typical performance characteristics

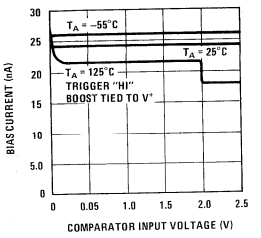
### Comparator Bias Current



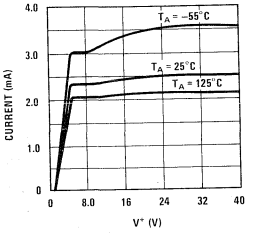

### Comparator Bias Current



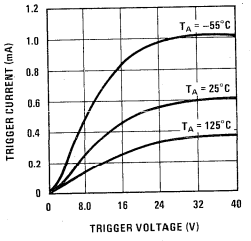

### Comparator Bias Current



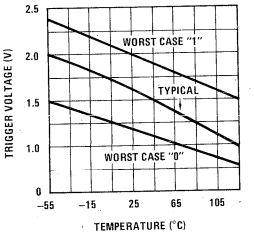

### Supply Current



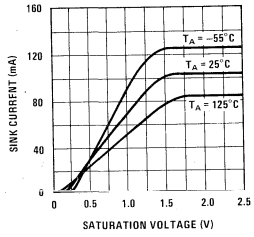

### Trigger Input Characteristics



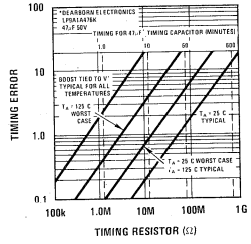

### Trigger Threshold



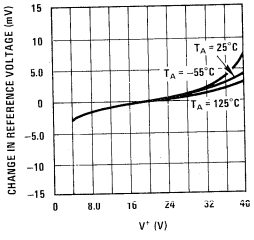

### Collector Output Saturation Characteristics at High Current



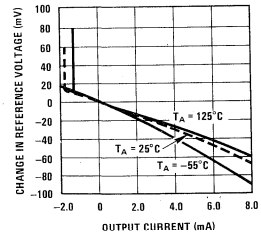

### Timing Error Due to Comparator Bias Current



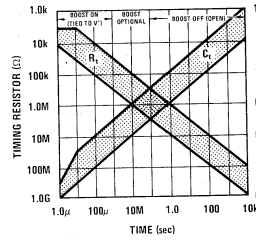

### Reference Regulation



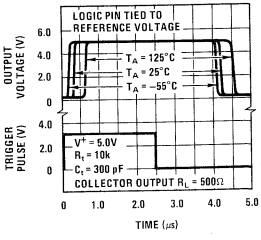

### Reference Regulation




### Suggested Timing Components




### Short Output Pulse



Nello Sevastopoulos
George Cleveland
Jim Sherwin
MARCH 1974

# LM340 SERIES THREE TERMINAL POSITIVE REGULATORS

## INTRODUCTION

The LM340-XX are three terminal 1.0A positive voltage regulators with preset output voltages of 5.0V, 6.0V, 8.0V, 12V, 15V, 18V or 24V. The LM340 regulators are complete 3-terminal regulators requiring no external components for normal operation. However, by adding a few parts, one may improve the transient response, provide for a variable output voltage, or increase the output current. Included on the chip are all of the functional blocks required of a high stability voltage regulator; these appear in Figure 1. The

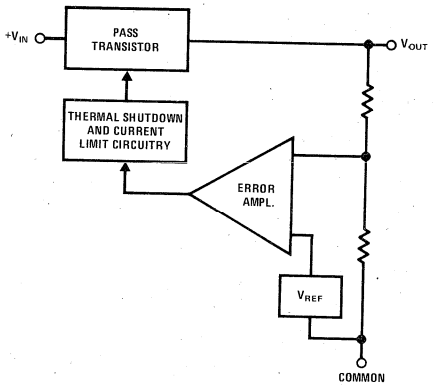



**FIGURE 1. Functional Block of the LM340**

error amplifier is internally compensated; the voltage reference is especially designed for low noise and high predictability; and, as the pass element is included, the regulator contains fixed current limiting and thermal protection. The LM340 is available in either metal can TO-3 or plastic TO-220 package.

## 1. CIRCUIT DESIGN

### Voltage Reference

Usually IC voltage regulators use temperature-compensated zeners as references. Such zeners exhibit BV > 6.0V which sets the minimum supply voltage somewhat above 6.0V. Additionally they tend to be noisy, thus a large bypass capacitor is required.

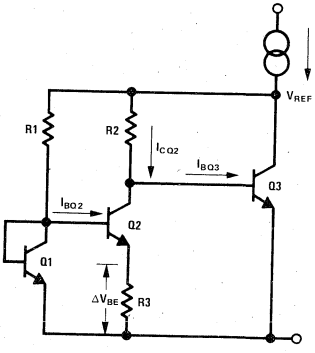



**FIGURE 2. Simplified Volt Reference**

Figure 2 illustrates a simplified reference using the predictable temperature, voltage, and current relationship of emitter-base junctions.

Assuming $J_{Q1} > J_{Q2}$, $I_{CQ2} >> I_{BQ2} = I_{BQ3}$, Area (emitter Q1) = Area (emitter Q2),

and $V_{BEQ1} = V_{BEQ3}$, then (1-1)

$$V_{REF} \simeq \left(\frac{kT}{q} \ln \frac{R2}{R1}\right) \frac{R2}{R3} + V_{BEQ3} \quad (1\text{-}2)$$

### Simplified LM340

In Figure 3 the voltage reference includes R1 – R3 and Q1 – Q5. Q3 also acts as an error amplifier and Q6 as a buffer between Q3 and the current source. If the output drops, this drop is fed back, through R4, R5, Q4, Q5, to the base of Q3. Q7 then conducts more current re-establishing the output given by:

$$V_{OUT} = V_{REF} \frac{R4 + R5}{R4}$$

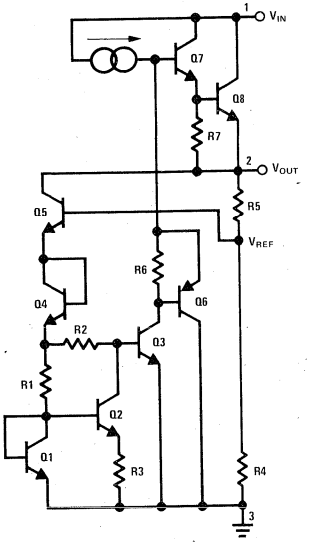



FIGURE 3. LM340 Simplified

## Complete Circuit of the LM340 (Figure 4)

Here $(J_{Q2}, J_{Q3}) > (J_{Q4}, J_{Q5})$ and a positive TC $\Delta V_{BE}$ appears across R6. This is amplified by 17, (R6/R6 = 17) and is temperature compensated by the $V_{BE}$ of Q6, Q7, Q8 to develop the reference voltage. R17 is changed to get the various fixed output voltages.

## Short Circuit Protection

A) $V_{IN} - V_{OUT} < 6.0V$: There is no current through D2 and the maximum output current will be given by:

$$I_{OUT\,MAX} = \frac{V_{BEQ14}}{R16} \simeq 2.2A\ (T_j = 25^\circ C) \quad (1\text{-}4)$$

B) $V_{IN} - V_{OUT} > 6.0V$: To keep Q16 operating within its maximum power rating the output current limit must decrease as $V_{IN} - V_{OUT}$ increases. Here D2 conducts and the drop across R16 is less than $V_{BE}$ to turn on Q14. In this case $I_{OUT}$ maximum is:

$$I_{OUT\,MAX} = \frac{1}{R16}\left(V_{BEQ14} - \frac{[(V_{IN}-V_{OUT})-V_{ZD2}-V_{BEQ14}]}{R13}R14\right) \quad (1\text{-}5)$$

$$= 0.077\,[37.2-(V_{IN}-V_{OUT})]\ (A)$$

at $T_j = 25^\circ C$

## Thermal Shut Down

In Figure 4 the $V_{BE}$ of Q13 is clamped to 0.4V. When the die temperature reaches approximately +175°C the $V_{BE}$ to turn on Q13 is 0.4V. When Q13 turns on it removes all base drive from Q15

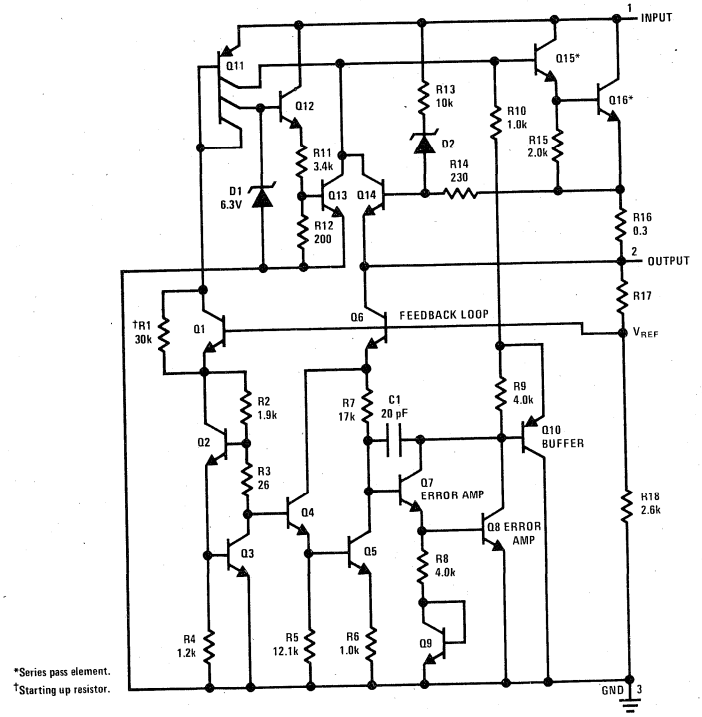



FIGURE 4. Complete Circuit of the LM340

which turns off the regulator thus preventing a further increase in die temperature.

**Power Dissipation**

The maximum power dissipation of the LM340 is given by:

$$P_{DMAX} = (V_{INMAX} - V_{OUT})\, I_{OUTMAX} + V_{INMAX}\, I_Q \text{ (W)} \quad (1\text{-}6)$$

The maximum junction temperature (assuming that there is no thermal protection) is given by:

$$T_{jM} = \frac{36 - 13\, I_{OUTMAX} - (V_{IN} - V_{OUT})}{0.0855} + 25^\circ C \quad (1\text{-}7)$$

Example:

$V_{INMAX}$ = 23V, $I_{OUTMAX}$ = 1.0A, LM340T-15.

Equation (1-7) yields: $T_{jM} = 200^\circ C$. So the $T_j$ max of 150°C specified in the data sheet should be the limiting temperature.

From (1-6) $P_D \cong 8.1W$. The thermal resistance of the heat sink can be estimated from:

$$\theta_{s\text{-}a} = \frac{T_{jMAX} - T_A}{P_D} - (\theta_{j\text{-}c} + \theta_{c\text{-}s})(^\circ C/W) \quad (1\text{-}8)$$

The thermal resistance $\theta_{j\text{-}c}$ (junction to case) of the TO-220 package is 6°C/W, and assuming a $\theta_{c\text{-}s}$ (case to heat sink) of 0.4, equation (1-8) yields:

$\theta_{s\text{-}a} = 8.4^\circ C/W$

## 2. CURRENT SOURCE

The circuit shown on Figure 5 provides a constant output current (equal to $V_{OUT}/R1$ or 200 mA)

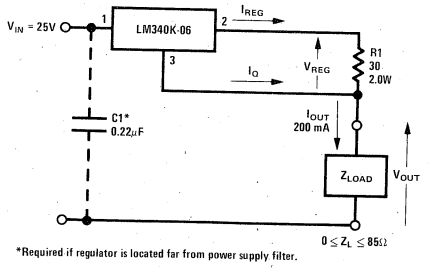



**FIGURE 5. Current Source**

for a variable load impedance of 0 to 85Ω. Using the following definitions and the notation shown on Figure 5, $Z_{OUT}$ and $I_{OUT}$ are:

$Q_{CC}/V$ = Quiescent current change per volt of input/output (pin 1 to pin 2) voltage change of the LM340

$L_r/V$ = Line regulation per volt: the change in the LM340 output voltage per volt of input/output voltage change at a given $I_{OUT}$.

$$\Delta I_{OUT} = (Q_{CC}/V)\, \Delta V_{OUT} + \frac{L_r/V}{R1}\, \Delta V_{OUT} \quad (2\text{-}1)$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \quad (2\text{-}2)$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{(Q_{CC}/V)\, \Delta V_{OUT} + \frac{(L_r/V)}{R1}\, \Delta V_{OUT}} \quad (2\text{-}3)$$

$$Z_{OUT} = \frac{1}{(Q_{CC}/V) + \frac{(L_r/V)}{R1}} \quad (2\text{-}4)$$

The LM340-06 data sheet lists maximum quiescent current change of 1.3 mA for an 8.0V to 25V change in input voltage; and a line regulation (interpolated for $I_{OUT}$ = 200 mA) of 75 mV maximum for an 8.0V to 25V change in input voltage:

$$Q_{CC}/V = \frac{1.3\text{ mA}}{17V} = 76\mu A/V \quad (2\text{-}5)$$

$$L_r/V = \frac{75\text{ mV}}{17V} = 4.4\text{ mV/V} \quad (2\text{-}6)$$

The worst case change in the 200 mA output current for a 1.0V change in output or input voltage using equation 2-1 is:

$$\frac{\Delta I_{OUT}}{1.0V} = 76\mu A + \frac{4.4\text{ mV}}{30\Omega} = 223\mu A \quad (2\text{-}7)$$

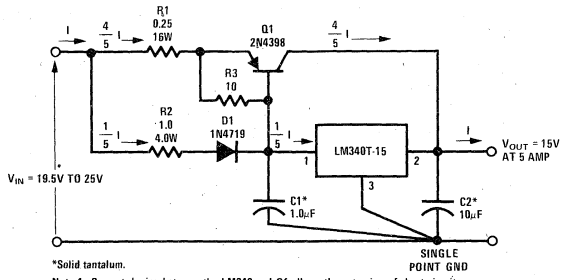
and the output impedance for a 0 to 85Ω change in $Z_L$ using equation 2-4 is:

$$Z_{OUT} = \frac{1}{76\mu A + \frac{4.4\text{ mV}}{30\Omega}} = 4.5\text{ k}\Omega \quad (2\text{-}8)$$

Typical measured values of $Z_{OUT}$ varied from 10 – 12.3 kΩ, or 81 – 100μA/V change input or output (approximately 0.05%/V).

## 3. HIGH CURRENT REGULATOR WITH SHORT CIRCUIT CURRENT LIMIT

The 15V regulator circuit of Figure 6 includes an external boost transistor to increase output current capability to 5.0A. Unlike the normal boosting methods, it maintains the LM340's ability to provide short circuit current limiting and thermal shut-down without use of additional active components. The extension of these safety features to the external pass transistor Q1 is based on a current sharing scheme using R1, R2, and D1. Assuming




*Solid tantalum.

Note 1: Current sharing between the LM340 and Q1 allows the extension of short circuit current limit, safe operating area protection, and (assuming Q1's heat sink has four or more times the capacity of the LM340 head sink) thermal shutdown protection.

Note 2: $I_{SHORT\ CIRCUIT}$ is approximately 5.5 amp.

Note 3: $I_{OUT\ MAX}$ at $V_{OUT}$ = 15V is approximately 9.5 amp.

**FIGURE 6. 15V 5.0A Regulator with Short Circuit Current Limit**

the base-to-emitter voltage of Q1 and the voltage drop across D1 are equal, the voltage drops across R1 and R2 are equal. The currents through R1 and R2 will then be inversely proportional to their resistances. For the example shown on Figure 6, resistor R1 will have four times the current flow of R2. For reasonable values of Q1 beta, the current through R1 is approximately equal to the collector current of Q1; and the current through R2 is equal to the current flowing through the LM340. Therefore, under overload or short circuit conditions the protection circuitry of the LM340 will limit its own output current and, because of the R1/R2 current sharing scheme, the output current of Q1 as well. Thermal overload protection also extends Q1 when its heat sink has four or more times the capacity of the LM340 heat sink. This follows from the fact that both devices have approximately the same input/output voltage and share the load current in a ratio of four to one.

The circuit shown on Figure 6 normally operates at up to 5.0A of output current. This means up to 1.0A of current flows through the LM340 and up to 4.0A flows through Q1. For short term overload conditions the curve of Figure 7 shows the maximum instantaneous output current versus temperature for the boosted regulator. This curve reflects the approximately 2.0A current limit of the LM340 causing an 8.0A current limit in the pass

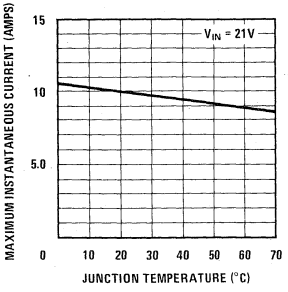



**FIGURE 7. Maximum Instantaneous Current vs Junction Temperature**

transistor, or 10A, total. Under continuous short circuit conditions the LM340 will heat up and limit to a steady total state short circuit current of 4.0A to 6.0A as shown in Figure 8. This curve was taken using a Wakefield 680-75 heat sink (approximately 7.5°C/W) at a 25°C ambient temperature.

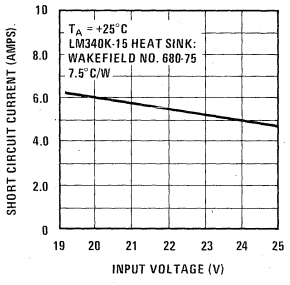



**FIGURE 8. Continuous Short Circuit Current vs Input Voltage**

For optimum current sharing over temperature between the LM340 and Q1, the diode D1 should be physically located close to the pass transistor on the heat sink in such a manner as to keep it at the same temperature as that of Q1. If the LM340 and Q1 are mounted on the same heat sink the LM340 should be electrically isolated from the heat sink since its case (pin 3) is at ground potential and the case of Q1 (its collector) is at the output potential of the regulator. Capacitors C1 and C2 are required to prevent oscillations and improve the output impedance respectively. Resistor R3 provides a path to unload excessive base charge from the base of Q1 when the regulator goes suddenly from full load to no load. The single point ground system shown on Figure 6 allows the sense pins (2 and 3) of the LM340 to monitor the voltage directly at the load rather than at some point along a (possibly) resistive ground return line carrying up to 5.0A of load current. Figure 9 shows the typical variation of load regulation versus load current for the boosted regulator. The insertion of the external pass transistor increases the input/output differential voltage from 2.0V to approximately 4.5V. For an

output current less than 5.0A, the R2/R1 ratio can be set lower than 4:1. Therefore, a less expensive PNP transistor may be used.

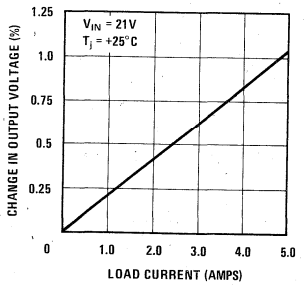



**FIGURE 9. Load Regulation**

## 4. 5.0V, 5.0A VOLTAGE REGULATOR FOR TTL

The high current 5.0V regulator for TTL shown in Figure 10 uses a relatively inexpensive NPN pass transistor with a lower power PNP device to replace the single, higher cost, power PNP shown in Figure 6. This circuit provides a 5.0V output at up to 5.0A of load current with a typical load regulation of 1.8% from no load to full load. The peak instantaneous output current observed was 10.4A at a 25°C junction temperature (pulsed load with a 1.0 ms ON and a 200 ms OFF period) and 8.4A for a continuous short circuit. The typical line regulation is 0.02% of input voltage change ($I_{OUT}$ = 0).

One can easily add an overload indicator using the National's new NSL5027 LED. This is shown with dotted lines in Figure 10. With this configuration R2 is not only a current sharing resistor but also an overload sensor. R5 will determine the current through the LED; the diode D2 has been added to match the drop across D1. Once the load current exceeds 5.0A (1.0A through the LM340 assuming perfect current sharing and $V_{D1}$ = $V_{D2}$) Q3 turns ON and the overload indicator lights up.

Example:

$I_{OVERLOAD}$ = 5.0A

$I_{LED}$ = 40 mA (light intensity of 16 mcd)

$$V_{LED} = 1.75,\ R5 \simeq \frac{V_{IN} - 2.65}{I_{LED}} \qquad (4\text{-}1)$$

## 5. ADJUSTABLE OUTPUT VOLTAGE REGULATOR FOR INTERMEDIATE OUTPUT VOLTAGES

The addition of two resistors to an LM340 circuit allows a non-standard output voltage while maintaining the limiting features built into IC. The example shown in Figure 11 provides a 10V output using an LM340K-08 by raising the reference (pin number 3) of the regulator by 2.0V.

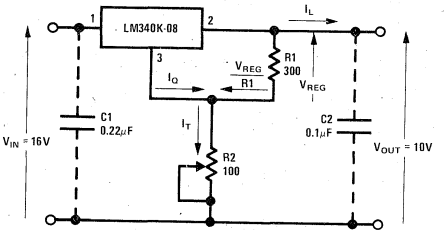
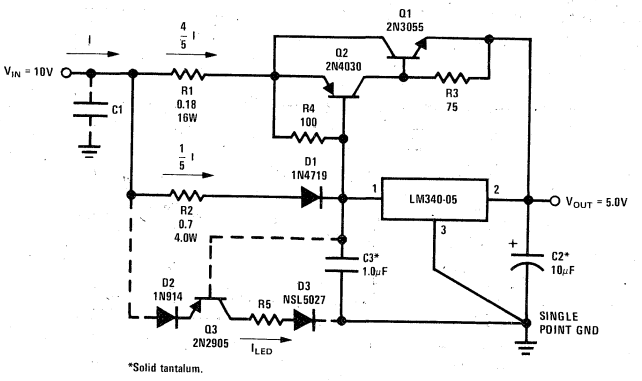



**FIGURE 11. 10V Regulator**

The 2.0V pedestal results from the sum of regulator quiescent current $I_Q$ and a current equal to $V_{REG}$/R1, flowing through potenteniometer R2 to ground. R2 is made adjustable to compensate for differences in $I_Q$ and $V_{REG}$ output. The circuit is practical because the change in $I_Q$ due to line voltage and load current changes is quite small.

The line regulation for the boosted regulator is the sum of the LM340 line regulation, its effects on the current through R2, and the effects of




*Solid tantalum.

**FIGURE 10. 5.0V, 5.0A Regulator for TTL (with short circuit, thermal shutdown protection, and overload indicator)**

$\Delta I_Q$ in response to input voltage changes. The change in output voltage is:

$$\Delta V_{OUT} = (L_r/V)\,\Delta V_{IN} + \frac{(L_r/V)\,\Delta V_{IN}\,R2}{R1} + (Q_{CC}/V)\,\Delta V_{IN}\,R2 \quad (5\text{-}1)$$

giving a total line regulation of:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = (L_r/V)\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/V)\,R2 \quad (5\text{-}2)$$

The LM340-08 data sheet lists $\Delta V_{OUT} < 160$ mV and $\Delta I_Q < 1.0$ mA for $\Delta V_{IN} = 14.5$V at $I_{OUT} = 500$ mA. This is:

$$L_r/V = \frac{160\text{ mV}}{14.5\text{V}} = 11\text{ mV/V} \quad (5\text{-}3)$$

$$Q_{CC}/V = \frac{1.0\text{ mA}}{14.5\text{V}} = 60\mu\text{A/V} \quad (5\text{-}4)$$

The worst case at line regulation for the circuit of Figure 12 calculated by equation 5-2, $I_{OUT} = 500$ mA and R2 = 61Ω is:

$$\frac{\Delta V_{OUT}}{1.0\text{V}} = 11\text{ mV/V}\left(1 + \frac{61\Omega}{300\Omega}\right) + (69\mu\text{A/V})\,61\Omega \quad (5\text{-}5)$$

$$\frac{\Delta V_{OUT}}{1.0\text{V}} = 13.2\text{ mV/V} + 4.2\text{ mV/V} = 17.4\text{ mV/V} \quad (5\text{-}6)$$

This represents a worst case line regulation value of 0.17%/V.

The load regulation is the sum of the LM340 voltage regulation, its effect on the current through R2, and the effect of $\Delta I_Q$ in response to changes in load current. Using the following definitions and the notation shown on Figure 11 $\Delta V_{OUT}$ is:

$Z_{OUT}$ = Regulator output impedance: the change in output voltage per amp of load current change.

$Z_{340}$ = LM340 output impedance

$Q_{CC}/A$ = Quiescent current change per amp of load current change

$$\Delta V_{OUT} = (Z_{340})\,\Delta I_L + \frac{(Z_{340})}{R1}\,\Delta I_L\,R2 + (Q_{CC}/A)\,\Delta I_L\,R2 \quad (5\text{-}7)$$

and the total output impedance is:

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_L} = Z_{340}\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/A)\,R2 \quad (5\text{-}8)$$

The LM340-08 data sheet gives a maximum load regulation $L_r = 160$ mV and $\Delta I_Q = 0.5$ mA for a 1.5A load change.

$$Z_{340} = \frac{160\text{ mV}}{1.5\text{A}} = 0.107\Omega \quad (5\text{-}9)$$

$$Q_{CC}/A = \frac{0.5\text{ mA}}{1.5\text{A}} = 333\mu\text{A/A} \quad (5\text{-}10)$$

This gives a worst case dc output impedance (ac output impedance being a function of C2) for the 10V regulator using equation 5-8 of:

$$Z_{OUT} = 0.107\Omega\left(1 + \frac{61\Omega}{300\Omega}\right) + (333\mu\text{A/A})\,61\Omega \quad (5\text{-}11)$$

$$Z_{OUT} = 0.12\Omega + 0.020\Omega = 0.14\Omega$$

or a worst case change of approximately 1.5% for a 1.0A load change. Typical measured values are about 0.56% or one-third of the worst case value.

## 6. VARIABLE OUTPUT REGULATOR

In Figure 12 the ground terminal of the regulator is "lifted" by an amount equal to the voltage applied to the non-inverting input of the operational amplifier LM101A. The output voltage of the

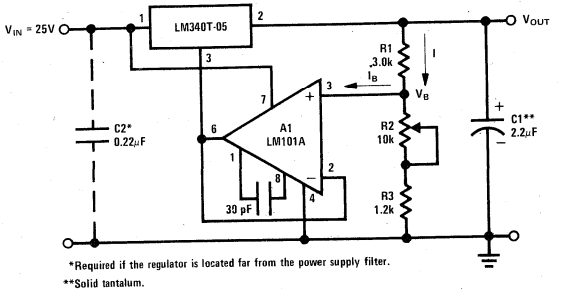



**FIGURE 12. Variable Output Regulator**

regulator is therefore raised to a level set by the value of the resistive divider R1, R2, R3 and limited by the input voltage. With the resistor values shown in Figure 12, the output voltage is variable from 7.0V to 23V and the maximum output current (pulsed load) varies from 1.2A to 2.0A ($T_j = 25°C$) as shown in Figure 13.

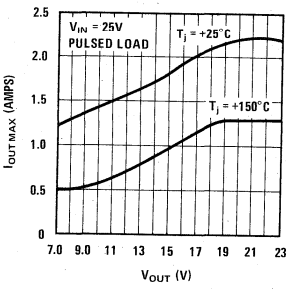



**FIGURE 13. Maximum Output Current**

Since the LM101A is operated with a single supply (the negative supply pin is grounded). The common mode voltage $V_B$ must be at least at a 2.0 $V_{BE}$ + $V_{SAT}$ above ground. R3 has been added to insure this when R2 = 0. Furthermore the bias current $I_B$ of the operational amplifier should be negligible compared to the current flowing through the resistive divider.

Example:

$V_{IN}$ = 25V

$V_{OUT\,MIN} = 5 + V_B$, (R2 = 0),
$V_B = R3\,(I - I_B) = 2.0V$
R1 = 2.5 R3

$V_{OUT\,MAX} = V_{IN}$ − dropout volt.
$(R2 = R2_{MAX})$
$R2_{MAX} = 3.3\,R1$

So setting R3, the values of R1 and R2 can be determined.

If the LM324 is used instead of the LM101A, R3 can be omitted since its common mode voltage range includes the ground, and then the output will be adjustable from 5 to a certain upper value defined by the parameters of the system.

The circuit exhibits the short-circuit protection and thermal shutdown properties of the LM340 over the full output range.

The load regulation can be predicted as:

$$\Delta V_{OUT} = \frac{R1 + R2 + R3}{R1}\,\Delta V_{340} \qquad (6\text{-}1)$$

where $\Delta V_{340}$ is the load regulation of the device given in the data sheet. To insure that the regulator will start up under full load a reverse biased small signal germanium diode, 1N91, can be added between pins 2 and 3.

## 7. VARIABLE OUTPUT REGULATOR 0.5V – 29V

When a negative supply is available an approach equivalent to that outlined in section 6 may be used to lower the minimum output voltage of the regulator below the nominal voltage that of the LM340 regulator device. In Figure 14 the voltage $V_G$ at the ground pin of the regulator is determined by the drop across R1 and the gain of the amplifier. The current I may be determined by the following relation:

$$I = \frac{V_{340}}{R1}\,\frac{R2\,R5 - R3\,R4}{R4\,(R2 + R3)} + \frac{V_{IN}^-}{R1} \qquad (7\text{-}1)$$

or if R2 + R3 = R4 + R5 = R

$$I = \frac{V_{340}\,R2}{R1\,R4} + \frac{1}{R1}\,(V_{IN}^- - V_{340}) \qquad (7\text{-}2)$$

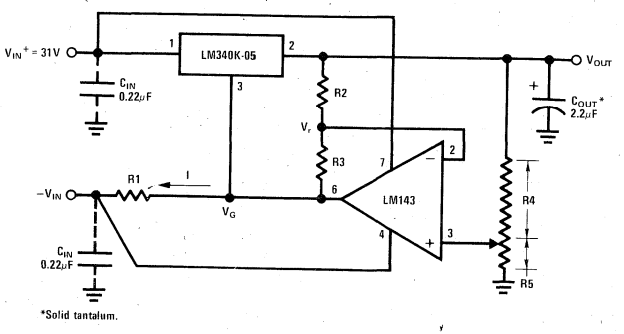



**FIGURE 14. Variable Output Voltage 0.5V – 30V**

considering that the output is given by:

$$V_{OUT} = V_G + V_{340} \quad (7\text{-}3)$$

and

$$V_G = R1\ I - V_{IN}^- \quad (7\text{-}4)$$

combining 7-2, 7-3, 7-4 an expression for the output voltage is:

$$V_{OUT} = V_{340}\ \frac{R2}{R4} \quad (7\text{-}5)$$

Notice that the output voltage is inversely proportional to R4 so the output voltage may be adjusted very accurately for low values. A minimum output of 0.5V has been set. This implies that

$$\frac{R2}{R4} = 0.1\ \frac{R3}{R4} = 0.9\ \frac{R3}{R2} = 9 \quad (7\text{-}6)$$

An absolute zero output voltage will require R4 = ∞ or R2 = 0, neither being practical in this circuit. The maximum output voltage as shown in Figure 14 is 30V if the high voltage operational amplifier LM143 is used. If only low values of $V_{OUT}$ are sought, then an LM101 may be used. R1 can be computed from:

$$R1 = \frac{V_{IN}^-}{I_{Q\,340}} \quad (7\text{-}7)$$

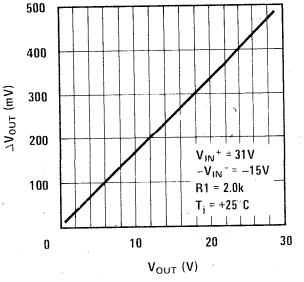



**FIGURE 15. Typical Load Regulation for a 0.5V – 30V Regulator ($\Delta I_{OUT}$ = 1.0A)**

Figure 15 illustrates the load regulation as a function of the output voltage.

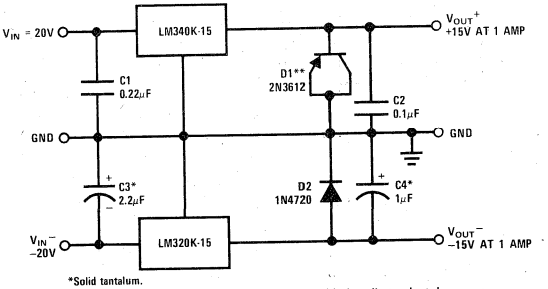
## 8. DUAL POWER SUPPLY

The plus and minus regulators shown in Figure 16 will exhibit line and load regulations consistant with their specifications as individual regulators. If fact, operation will be entirely normal until the problem of common loads occurs. A 30Ω load from the +15V output to the −15V output (representing a 0.5A starting load for the LM340K-15 if the LM320K-15 is already started) would allow start up of the LM340 in most cases. To insure LM340 startup over the full temperature range into a worst case 1.0A current sink load the germanium power "diode" D1 has been added to the circuit. Since the forward voltage drop of the germanium diode D1 is less than that of the silicon substrate diode of the LM340 the external diode will take any fault current and allow the LM340 to start up even into a negative voltage load. D1 and silicon diode D2 also protect the regulator outputs from inadvertant shorts between outputs and to ground. For shorts between outputs the voltage difference between either input and the opposite regulator output should not exceed the maximum rating of the device.

The example shown in Figure 16 is a symmetrical ±15V supply for linear circuits. The same principle applies to non-symmetrical supplies such as a +5.0V and −12V regulator for applications such as registers.

## 9. TRACKING DUAL REGULATORS

In Figure 17, a fraction of the negative output voltage "lifts" the ground pins of the negative LM320K-15 voltage regulator and the LM340K-15 through a voltage follower and an inverter respectively. The dual operational amplifier LM1558 is used for this application and since its supply voltage may go as high as ±22V the regulator outputs may be set between 5.0V and 20V. Because of the tighter output tolerance and the better drift of the LM320, the positive regulator




*Solid tantalum.
**Germanium diode (using a PNP germanium transistor with the collector shorted to the emitter).
Note: C1 and C2 required if regulators are located far from power supply filter.

**FIGURE 16. Dual Power Supply**

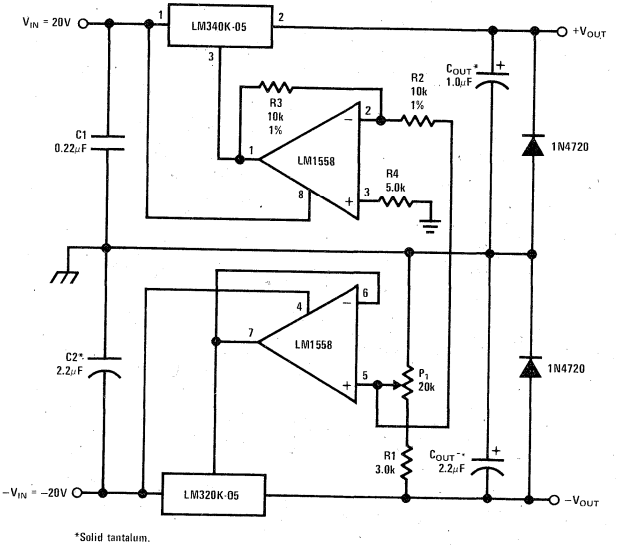



**FIGURE 17. Tracking Dual Supply ±5.0V — ±18V**

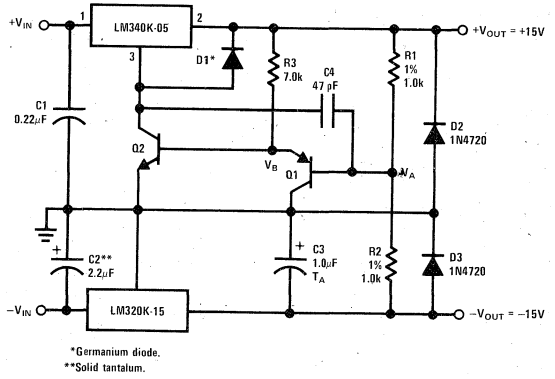



**FIGURE 18. Tracking Dual Supply ±15V**

is made to track the negative. The best tracking action is achieved by matching the gain of both operational amplifiers, that is, the resistors R2 and R3 must be matched as closely as possible.

Indeed, with R2 and R3 matched to better than 1%, the LM340 tracks the LM320 within 40 — 50 mV over the entire output range. The typical load regulation at $V_{OUT}$ = ±15V for the positive regulator is 40 mV from a 0 to 1.0A pulsed load and 80 mV for the negative.

Figure 18 illustrates ±15V tracking regulator, where again the positive regulator tracks the negative. Under steady state conditions $V_A$ is at a virtual ground and $V_B$ at a $V_{BE}$ above ground. Q2 then conducts the quiescent current of the LM340. If $-V_{OUT}$ becomes more negative the collector base junction of Q1 is forward biased thus lowering $V_B$ and raising the collector voltage of Q2. As a result $+V_{OUT}$ rises and the voltage $V_A$ again reaches ground potential.

Assuming Q1 and Q2 to be perfectly matched, the tracking action remains unchanged over the full operating temperature range.

With R1 and R2 matched to 1%, the positive regulator tracks the negative within 100 mV (less than 1%). The capacitor C4 has been added to improve stability. Typical load regulations for the positive and negative sides from a 0 to 1.0A pulsed load ($t_{ON}$ = 1.0 ms, $t_{OFF}$ = 200 ms) are 10 mV and 45 mV respectively.

## 10. HIGH INPUT VOLTAGE

The input voltage of the LM340 must be kept within the limits specified in the data sheet. If

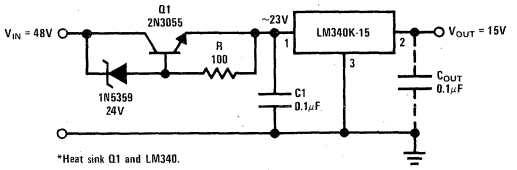



**FIGURE 19. High Input Voltage**

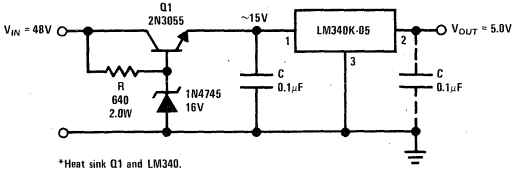



**FIGURE 20. High Input Voltage**

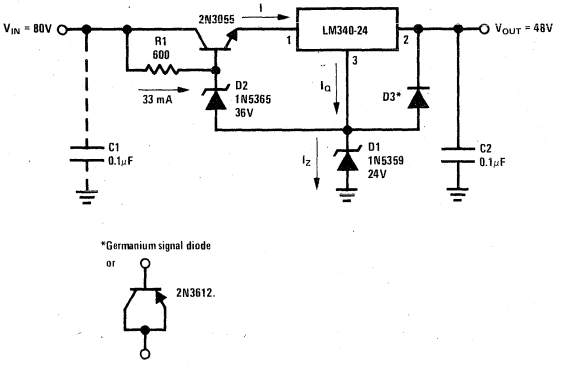



**FIGURE 21. High Voltage Regulator**

the device is operated above the absolute maximum input voltage rating, two failure modes may occur. With the output shorted to ground, the series pass transistor Q16 (see Figure 4) will go to avalanche breakdown; or, even with the output not grounded, the transistor Q1 may fail since it is operated with a collector-emitter voltage approximately 4.0V below the input.

If the only available supply runs at a voltage higher than the maximum specified, one of the simplest ways to protect the regulator is to connect a zener diode in series with the input of the device to level shift the input voltage. The drawback to this approach is obvious. The zener must dissipate ($V_{SUPPLY}$ − $V_{INMAX}$ LM340). ($I_{OUTMAX}$) which may be several watts. Another way to overcome the over voltage problem is illustrated in Figure 19 where an inexpensive, NPN-zener-resistor, combination may be considered as an equivalent to the power zener. The typical load regulation of this circuit is 40 mV from 0 to 1.0A pulsed load ($T_j$ = 25°C) and the line regulation is 2.0 mV for 1.0V variation in the input voltage ($I_{OUT}$ = 0). A similar alternate approach is shown in Figure 20.

With an optional output capacitor the measured noise of the circuit was 700μVp-p.

## 11. HIGH VOLTAGE REGULATOR

In previous sections the principle of "lifting the ground terminal" of the LM340, using a resistor divider or an operational amplifier, has been illustrated. One can also raise the output voltage by using a zener diode connected to the ground pin as illustrated in the Figure 21 to obtain an output level increased by the breakdown voltage of the zener. Since the input voltage of the regulator has been allowed to go as high as 80V a level shifting transistor-zener (D2)—resistor combination has been added to keep the voltage across the LM340 under permissible values. The disadvantage of the system is the increased output noise and output voltage drift due to the added diodes.

Indeed it can be seen that, from no load to full load conditions, the $\Delta I_Z$ will be approximately the current through R1 (≃ 35 mA) and therefore the degraded regulation caused by D1 will be $V_Z$ (at 35 mA + $I_Q$) − $V_Z$ (at $I_Q$).

The measured load regulation was 60 mV for $\Delta I_{OUT}$ of 5.0 mA to 1.0A (pulsed load), and the line regulation is 0.01%/V of input voltage change ($I_{OUT}$ = 500 mA) and the typical output noise 2.0 mVp-p (C2 = 0.1$\mu$F). The value of R1 is calculated as:

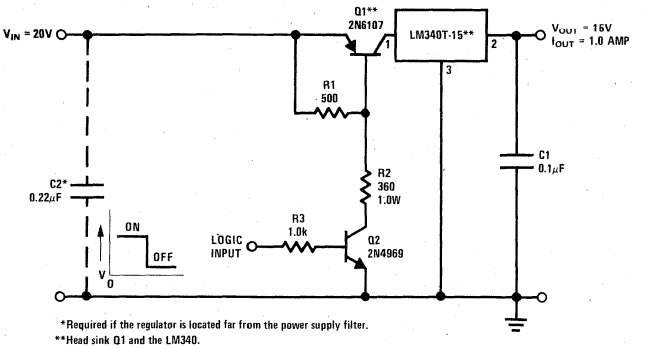
$$R1 \simeq \beta\left[\frac{V_{IN} - (V_{Z1} + V_{Z2})}{I \text{ full load}}\right] \qquad (11\text{-}1)$$

## 12. ELECTRONIC SHUTDOWN

Figure 22 shows a practical method of shutting down the LM340 under the control of a TTL or DTL logic gate. The pass transistor Q1 operates either as a saturated transistor or as an open switch. With the logic input high (2.4V specified minimum for TTL logic) transistor Q2 turns on and pulls 50 mA down through R2. This provides sufficient base drive to maintain Q1 in saturation during the ON condition of the switch. When the logic input is low (0.4V specified maximum for TTL logic) Q2 is held off, as is Q1; and the switch is in the OFF condition. The observed turn-on time was 7.0$\mu$s for resistive loads from 15$\Omega$ to infinity and the turn-off time varied from approximately 3.0$\mu$s for a 15$\Omega$ load to 3.0 ms for a no-load condition. Turn-off time is controlled primarily by the time constant of $R_{LOAD}$ and C1.

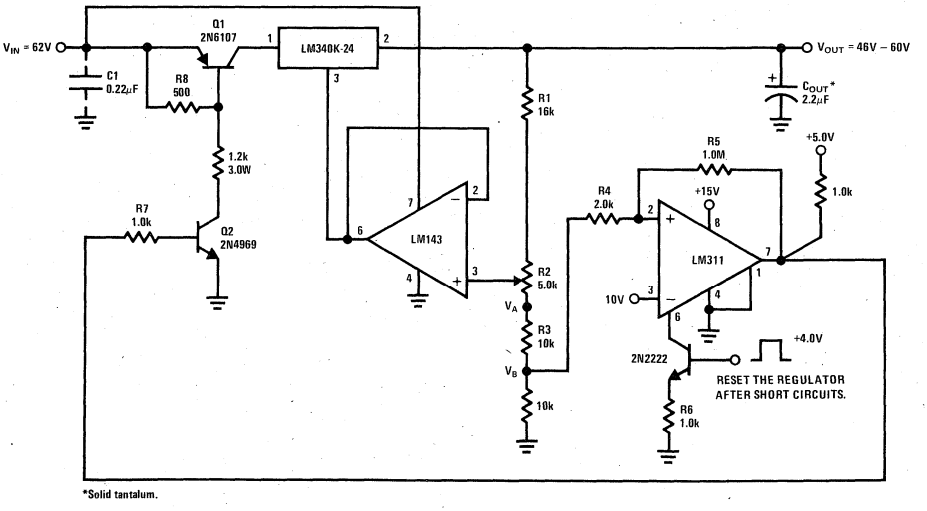
## 13. VARIABLE HIGH VOLTAGE REGULATOR WITH OVERVOLTAGE SHUTDOWN

A high voltage variable-output regulator may be constructed using the LM340 after the idea illustrated in section 7 and drawn in Figure 23. The principal inconvenience is that the voltage across the regulator must be limited to maximum rating of the device, the higher the applied input voltage the higher must be lifted the ground pin of the LM340. Therefore the range of the variable




*Required if the regulator is located far from the power supply filter.
**Head sink Q1 and the LM340.

**FIGURE 22. Electronic Shutdown Circuit**




*Solid tantalum.

**FIGURE 23. Variable High Voltage Regulator with Shortcircuit and Overvoltage Protection**

output is limited by the supply voltage limit of the operational amplifier and the maximum voltage allowed across the regulator. An estimation of this range is given by:

$$V_{OUTMAX} - V_{OUTMIN} = V_{SUPPLY\,MAX\,340} - V_{NOMINAL\,340} - 2.0V \quad (13\text{-}1)$$

Examples:

LM340-24: $V_{OUTMAX} - V_{OUTMIN} = 40 - 24 - 2 = 14V$

Figure 23 illustrates the above considerations. Even though the LM340 is by itself short circuit protected, when the output drops, also $V_A$ drops and the voltage difference across the device increases. If it exceeds 40V the pass transistor internal to the regulator will breakdown, as explained in section 11. To remedy this, an overvoltage shutdown is included in the circuit. When the output drops the comparator switches low, pulls down the base of Q2 thus opening the switch Q1, and shutting down the LM340. Once the short circuit has been removed the LM311 must be activated through the strobe to switch high and close Q1, which will start the regulator again. The additional voltages required to operate the comparator may be taken from the 62V since the LM311 has a certain ripple rejection and the reference voltage (pin 3) may have a superimposed small ac signal. The typical load regulation can be be computed from equation 6-1.

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Jim Sherwin
MAY 1974

## NOISE SPECS CONFUSING ?

It's really all very simple—once you understand it. Then, here's the inside story on noise for those of us who haven't been designing low noise amplifiers for ten years.

You hear all sorts of terms like signal-to-noise ratio, noise figure, noise factor, noise voltage, noise current, noise power, noise spectral density, noise per root Hertz, broadband noise, spot noise, shot noise, flicker noise, excess noise, 1/f noise, fluctuation noise, thermal noise, white noise, pink noise, popcorn noise, bipolar spike noise, low noise, no noise, and loud noise. No wonder not everyone understands noise specifications.

In a case like noise, it is probably best to sort it all out from the beginning. So, in the beginning, there was noise; and then there was signal. The whole idea is to have the noise very small compared to the signal; or, conversely, we desire a high signal-to-noise ratio S/N. Now it happens that S/N is related to noise figure NF, noise factor F, noise power, noise voltage $\bar{e}_n$, and noise current $\bar{i}_n$. To simplify matters, it also happens that any noisy channel or amplifier can be completely specified for noise in terms of two noise generators $\bar{e}_n$ and $\bar{i}_n$ as shown in Figure 1.

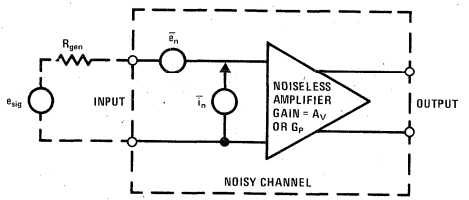



**FIGURE 1. Noise Characterization of Amplifier**

All we really need to understand are NF, $\bar{e}_n$, and $\bar{i}_n$. So here is a rundown on these three.

NOISE VOLTAGE, $\bar{e}_n$, or more properly, EQUIVALENT SHORT-CIRCUIT INPUT RMS NOISE VOLTAGE is simply that noise voltage which would appear to originate at the input of the noiseless amplifier if the input terminals were shorted. It is expressed in nanovolts per root Hertz $nV/\sqrt{Hz}$ at a specified frequency, or in microvolts in a given frequency band. It is determined or measured by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristic is used in measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$ if data is to be expressed per unit bandwidth or per root Hertz. The level of $\bar{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in Figure 2. This increase is 1/f NOISE.

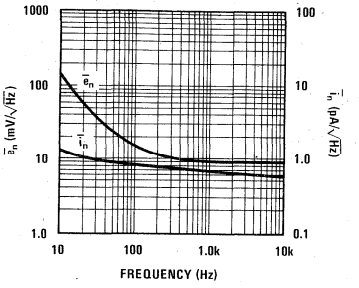



**FIGURE 2. Noise Voltage and Current for an Op Amp**

NOISE CURRENT, $\bar{i}_n$, or more properly, EQUIVALENT OPEN-CIRCUIT RMS NOISE CURRENT is that noise which occurs apparently at the input of the noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz $pA/\sqrt{Hz}$ at a specified frequency or in nanoamps in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional noise voltage which is $\bar{i}_n \times R_{in}$ (or $X_{cin}$). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\bar{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the input, there is only $\bar{e}_n$ and $\bar{i}_n$ $X_{cin}$. The $\bar{i}_n$ is measured with a bandpass filter and converted to $pA/\sqrt{Hz}$ if appropriate; typically it increases at lower frequencies for op amps and bipolar transistors, but increases at higher frequencies for field-effect transistors.

NOISE FIGURE, NF is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \log \frac{(S/N)_{in}}{(S/N)_{out}} \qquad (1)$$

where: S and N are power or $(\text{voltage})^2$ levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of $R_{gen}$ and any $X_{gen}$ as well as frequency must be known to properly express NF in meaningful terms. This is because the amplifier $\bar{i}_n \times Z_{gen}$ as well as $R_{gen}$ itself produces input noise. The signal source in Figure 1 contains some noise. However $e_{sig}$ is generally considered to be noise free and input noise is present as the THERMAL NOISE of the resistive component of the signal generator impedance $R_{gen}$. This thermal noise is WHITE in nature as it contains constant NOISE POWER DENSITY per unit bandwidth. It is easily seen from Equation 2 that the $\overline{e_n^2}$ has the units $V^2/Hz$ and that $(\bar{e}_n)$ has the units $V/\sqrt{Hz}$

$$\overline{e_R^2} = 4kTRB \qquad (2)$$

where: T is temperature in °K
R is resistor value in ohms
B is bandwidth in Hz
k is Boltzman's constant

### Relation Between $\bar{e}_n$, $\bar{i}_n$, $\mu F$

Now we can examine the relationship between $\bar{e}_n$ and $\bar{i}_n$ at the amplifier input. When the signal source is connected, the $\bar{e}_n$ appears in series with the $e_{sig}$ and $\bar{e}_R$. The $\bar{i}_n$ flows through $R_{gen}$ thus producing another noise voltage of value $\bar{i}_n \times R_{gen}$. This noise voltage is clearly dependent upon the value of $R_{gen}$. All of these noise voltages add at the input in rms fashion; that is, as the square root of the sum of the squares. Thus, neglecting possible correlation between $\bar{e}_n$ and $\bar{i}_n$, the total input noise is

$$\overline{e_N^2} = \overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2 \qquad (3)$$

Further examination of the NF equation shows the relationship of $\bar{e}_N$, $\bar{i}_n$, and NF.

$$NF = 10 \log \frac{S_{in} \times N_{out}}{S_{out} \times N_{in}}$$

$$= 10 \log \frac{S_{in}\, G_p\, \overline{e_N^2}}{S_{in}\, G_p\, \overline{e_R^2}}$$

where: $G_p$ = power gain

$$= 10 \log \frac{\overline{e_N^2}}{\overline{e_R^2}}$$

$$= 10 \log \frac{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2}{\overline{e_R^2}}$$

$$NF = 10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2}\, R_{gen}^2}{\overline{e_R^2}}\right) \qquad (4)$$

Thus, for small $R_{gen}$, noise voltage dominates; and for large $R_{gen}$, noise current becomes important. A clear advantage accrues to FET input amplifiers, especially at high values of $R_{gen}$, as the FET has essentially zero $\bar{i}_n$. Note, that for an NF value to have meaning, it must be accompanied by a value for $R_{gen}$ as well as frequency.

### Calculating Total Noise, $\bar{e}_N$

We can generate a plot of $\bar{e}_N$ for various values of $R_{gen}$ if noise voltage and current are known vs frequency. Such a graph is shown in Figure 3 drawn from Figure 2. To make this plot, the thermal noise $\bar{e}_R$ of the input resistance must be calculated from Equation 2 or taken from the graph of Figure 4. Remember that each term in Equation 3 must be squared prior to addition, so the data from Figure 4 and from Figure 2 is squared. A sample of this calculation follows.

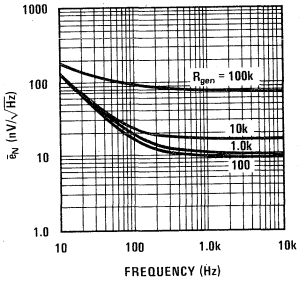



**FIGURE 3. Total Noise for the Op Amp of Figure 2.**

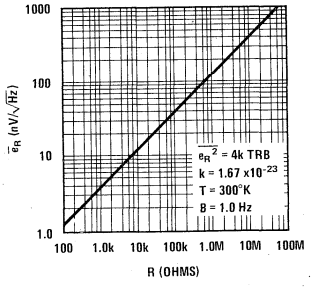



**FIGURE 4. Thermal Noise of Resistor**

Example 1: Determine total equivalent input noise per unit bandwidth for an amplifier operating at 1 kHz from a source resistance of 10 kohms. Use the data from Figures 2 and 4.

1. Read $\bar{e}_R$ from Figure 4 at 10 kohm; the value is 12 nV/$\sqrt{Hz}$.
2. Read $\bar{e}_n$ from Figure 2 at 1 kHz; the value is 9.5 nV/$\sqrt{Hz}$.
3. Read $\bar{i}_n$ from Figure 2 at 1 kHz; the value is 0.68 pA/$\sqrt{Hz}$. Multiply by 10 kohm to obtain 6.8 nV/$\sqrt{Hz}$.

4. Square each term individually, and enter into Equation 3.

$$\bar{e}_N = \sqrt{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2}$$

$$= \sqrt{9.5^2 + 12^2 + 6.8^2} \qquad = \sqrt{279}$$

$$\bar{e}_N = 16.7 \text{ nV}/\sqrt{\text{Hz}}$$

This is total rms noise at the input in one Hertz bandwidth at 1 kHz. If total noise in a given bandwidth is desired, one must integrate the noise over a bandwidth as specified. This is most easily done in a noise measurement set-up, but may be approximated as follows.

1. If the frequency range of interest is in the flat band; i.e., between 1 kHz and 10 kHz in Figure 2, it is simply a matter of multiplying $\bar{e}_N$ by the square root of the bandwidth. Then, in the 1 kHz-10 kHz band, total noise is

$$\bar{e}_N = 16.7\sqrt{9000}$$

$$= 1.59\mu V$$

2. If the frequency band of interest is not in the flat band of Figure 2, one must break the band into sections, calculating average noise in each section, squaring, multiplying by section bandwidth, summing all sections, and finally taking square root of the sum as follows:

$$\bar{e}_N = \sqrt{\overline{e_R^2} B + \sum_1^i (\overline{e_n^2} + \overline{i_n^2} R_{gen}^2)_i \, B_i} \qquad (5)$$

where: i is the total number of sub-blocks.

For most purposes a sub-block may be one or two octaves. Example 2 details such a calculation.

Example 2: Determine the rms noise level in the frequency band 50 Hz to 10 kHz for the amplifier of Figure 2 operating from $R_{gen}$ = 2k.

1. Read $\bar{e}_R$ from Figure 4 at 2k, square the value, and multiply by the entire bandwidth. Easiest way is to construct a table as shown below.
2. Read the median value of $\bar{e}_n$ in a relatively small frequency band, say 50 Hz-100 Hz, from Figure 2, square it and enter into the table.
3. Read the median value of $\bar{i}_n$ in the 50 Hz-100 Hz band from Figure 2, multiply by $R_{gen}$ = 2k, square the result and enter in the table.
4. Sum the squared results from steps 2 and 3, multiply the sum by $\Delta f$ = 100–50 = 50 Hz, and enter in the table.
5. Repeat steps 2-4 for band sections of 100 Hz-300 Hz, 300 Hz-1000 Hz and 1 kHz-10 kHz. Enter results in the table.
6. Sum all entires in the last column, and finally take the square root of this sum for the total rms noise in the 50 Hz-10,000 Hz band.
7. Total $\bar{e}_n$ is 1.62$\mu$V in the 50 Hz-10,000 Hz band.

**Calculating S/N and NF**

Signal-to-noise ratio can be easily calculated from known signal levels once total rms noise in the band is determined. Example 3 shows this rather simple calculation from Equation 6 for the data of Example 2.

$$S/N = 20 \log \frac{e_{sig}}{\bar{e}_N} \qquad (6)$$

Example 3: Determine S/N for an rms $e_{sig}$ = 4 mV at the input to the amplifier operated in Example 2.

1. RMS signal is $e_{sig}$ = 4 mV
2. RMS noise from Example 2 is 1.62$\mu$V
3. Calculate S/N from Equation 6

$$S/N = 20 \log \frac{4 \text{ mV}}{1.62\mu V}$$

$$= 20 \log (2.47 \times 10^3)$$

$$= 20 (\log 10^3 + \log 2.47)$$

$$= 20 (3 + 0.393)$$

$$S/N = 68 \text{ dB}$$

**TABLE I. Noise Calculations for Example 2**

| B (Hz) | $\Delta$f (Hz) | $\bar{e}_n^2$ (nV/Hz) | + $\bar{i}_n^2 R_{gen}^2$ | | | SUM x $\Delta$f | = | ($nV^2$) |
|---|---|---|---|---|---|---|---|---|
| 50-100 | 50 | $(20)^2 = 400$ | $(8.7 \times 2.0k)^2$ | = | 302 | 702* x 50 | | 35,000 |
| 100-300 | 200 | $(13)^2 = 169$ | $(8 \times 2.0k)^2$ | = | 256 | 425 x 200 | | 85,000 |
| 300-1000 | 700 | $(10)^2 = 100$ | $(7 \times 2.0k)^2$ | = | 196 | 296 x 700 | | 207,000 |
| 1.0k-10k | 9000 | $(9)^2 = 81$ | $(6 \times 2.0k)^2$ | = | 144 | 225 x 9000 | | 2,020,000 |
| 50-10,000 | 9950 | $\bar{e}_R^2 = (5.3)^2 = 28$ | | | | 28 x 9950 | | 279,000 |
| Total $\bar{e}_N = \sqrt{2{,}626{,}000} = 1620$ nV = 1.62$\mu$V | | | | | | | | |

*The units are as follows: $(20 \text{ nV}/\sqrt{\text{Hz}})^2 = 400 \text{ (nV)}^2/\text{Hz}$

$(8.7 \text{ pA}/\sqrt{\text{Hz}} \times 2.0\text{kohms})^2 = (17.4 \text{ nA}/\sqrt{\text{Hz}})^2 = 302 \text{ (nV)}^2/\text{Hz}$

Sum = 702 $(\text{nV})^2/\text{Hz}$ x 50 Hz = 35,000 $(\text{nV})^2$

It is also possible to plot NF vs frequency at various $R_{gen}$ for any given plot of $\bar{e}_n$ and $\bar{i}_n$. However there is no specific all-purpose conversion plot relating NF, $\bar{e}_n$, $\bar{i}_n$, $R_{gen}$ and f. If either $\bar{e}_n$ or $\bar{i}_n$ is neglected, a reference chart can be constructed. Figure 5 is such a plot when only $\bar{e}_n$ is considered. It is useful for most op amps when $R_{gen}$ is less than about 200 ohms and for FETs at any $R_{gen}$ (because there is no significant $\bar{i}_n$ for FETs), however actual NF for op amps with $R_{gen} > 200$ ohms is higher than indicated on the chart.

The graph of Figure 5 can be used to find spot NF if $\bar{e}_n$ and $R_{gen}$ are known, or to find $\bar{e}_n$ if NF and $R_{gen}$ are known. It can also be used to find max $R_{gen}$ allowed for a given max NF when $\bar{e}_n$ is known. In any case, values are only valid if $\bar{i}_n$ is negligible and at the specific frequency of interest for NF and $\bar{e}_n$, and for 1 Hz bandwidth. If bandwidth increases, the plot is valid so long as $\bar{e}_n$ is multiplied by $\sqrt{B}$.

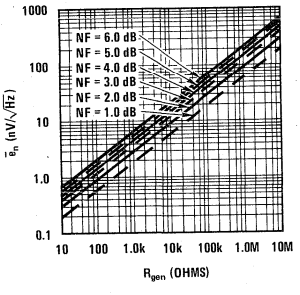



**FIGURE 5. Spot NF vs $R_{gen}$ when Considering *Only* $\bar{e}_n$ and $\bar{e}_R$ (not valid when $\bar{i}_n$ $R_{gen}$ is significant)**

### The Noise Figure Myth

Noise figure is easy to calculate because the signal level need not be specified (note that $e_{sig}$ drops out of Equation 4). Because NF is so easy to handle in calculations, many designers tend to lose sight of the fact that signal-to-noise ratio $(S/N)_{out}$ is what is important in the final analysis, be it an audio, video, or digital data system. One can, in fact, choose a high $R_{gen}$ to reduce NF to near zero if $\bar{i}_n$ is very small. In this case $\bar{e}_R$ is the major source of noise, overshadowing $\bar{e}_n$ completely. The result is very low NF, but very low S/N as well because of very high noise. Don't be fooled into believing that low NF means low noise *per se!*

Another term is worth considering, that is optimum source resistance $R_{OPT}$. This is a value of $R_{gen}$ which produces the lowest NF in a given system. It is calculated as

$$R_{OPT} = \frac{\bar{e}_n}{\bar{i}_n} \qquad (7)$$

This has been arrived at by differentiating Equation 4 with respect to $R_{gen}$ and equating it to zero (see Appendix). *Note that this does not mean lowest noise.*

For example, using Figure 2 to calculate $R_{OPT}$ at say 600 Hz,

$$R_{OPT} = \frac{10 \text{ nV}}{0.7 \text{ pA}} = 14 \text{ kohms}$$

Then note in Figure 3, that $\bar{e}_N$ is in the neighborhood of 20 nV/$\sqrt{\text{Hz}}$ for $R_{gen}$ of 14k. While $\bar{e}_N$ = 10 nV/$\sqrt{\text{Hz}}$ for $R_{gen}$ = 0-100 ohms. STOP! Do not pass GO. Do not be fooled. Using $R_{gen} = R_{OPT}$ does not guarantee lowest noise UNLESS $e_{sig}^2 = kR_{gen}$ as in the case of transformer coupling. When $e_{sig}^2 > kR_{gen}$, as is the case where signal level is proportional to $R_{gen}$ ($e_{sig} = kR_{gen}$), it makes sense to use the highest practical value of $R_{gen}$. When $e_{sig}^2 < kR_{gen}$, it makes sense to use a value of $R_{gen} < R_{OPT}$. These conclusions are verified in the Appendix.

This all means that it does not make sense to tamper with the $R_{gen}$ of existing signal sources in an attempt to make $R_{gen} = R_{OPT}$. Especially, do not add series resistance to a source for this purpose. It does make sense to adjust $R_{gen}$ in transformer coupled circuits by manipulating turns ratio or to design $R_{gen}$ of a magnetic pick-up to operate with pre-amps where $R_{OPT}$ is known. It does make sense to increase the design resistance of signal sources to match or exceed $R_{OPT}$ so long as the signal voltage increases with $R_{gen}$ in at least the ratio $e_{sig}^2 \propto R_{gen}$. It does not necessarily make sense to select an amplifier with $R_{OPT}$ to match $R_{gen}$ because one amplifier operating at $R_{gen} = R_{OPT}$ may produce lower S/N than another (quieter) amplifier operating with $R_{gen} \neq R_{OPT}$.

With some amplifiers it is possible to adjust $R_{OPT}$ over a limited range by adjusting the first stage operating current (the National LM121 and LM381 for example). With these, one might increase operating current, varying $R_{OPT}$, to find a condition of minimum S/N. Increasing input stage current decreases $R_{OPT}$ as $\bar{e}_n$ is decreased and $\bar{i}_n$ is simultaneously increased.

Let us consider one additional case of a fairly complex nature just as a practical example which will point up some factors often overlooked.

Example 4: Determine the S/N *apparent to the ear* of the amplifier of Figure 2 operating over 50-12, 800 Hz when driven by a phonograph cartridge exhibiting $R_{gen}$ = 1350Ω, $L_{gen}$ = 0.5H, and average $e_{sig}$ = 4.0 mVrms. The cartridge is to be loaded by 47k as in Figure 6. This is equivalent to using a Shure V15, Type 3 for average level recorded music.

1. Choose sectional bandwidths of 1 octave each, these are listed in the following table.
2. Read $\bar{e}_n$ from Figure 2 as average for each octave and enter in the table.
3. Read $\bar{i}_n$ from Figure 2 as average for each octave and enter in the table.
4. Read $\bar{e}_R$ for the $R_{gen}$ = 1350Ω from Figure 4 and enter in the table.

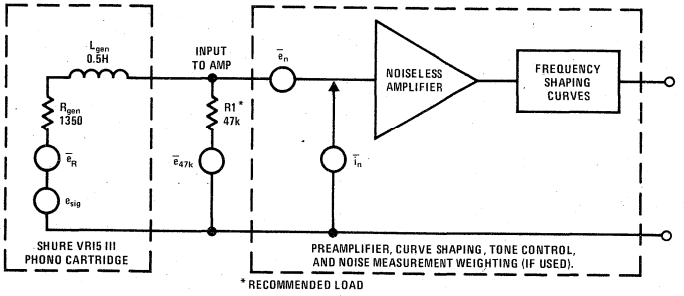



**FIGURE 6. Phono Preamp Noise Sources**

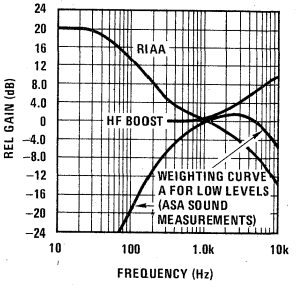



**FIGURE 7. Relative Gain for RIAA, ASA Weighting A, and H-F Boost Curves**

5. Determine the values of $Z_{gen}$ at the midpoint of each octave and enter in the table.
6. Determine the amount of $\bar{e}_R$ which reaches the amplifier input; this is

$$\bar{e}_R \frac{R1}{R1 + Z_{gen}}$$

7. Read the noise contribution $\bar{e}_{47k}$ of R1 = 47k from Figure 4.
8. Determine the amount of $\bar{e}_{47K}$ which reaches the amplifier input; this is

$$\bar{e}_{47k} \frac{Z_{gen}}{R1 + Z_{gen}}$$

9. Determine the effective noise contributed by $\bar{i}_n$ flowing through the parallel combination of R1 and $Z_{gen}$. This is

$$\bar{i}_n \frac{Z_{gen} R1}{Z_{gen} + R1}$$

10. Square all noise voltage values resulting from steps 2, 6, 8 and 9; and sum the squares.
11. Determine the relative gain at the midpoint of each octave from the RIAA playback response curve of Figure 7.
12. Determine the relative gain at these same midpoints from the A weighted response curve of Figure 7 for sound level meters (this roughly accounts for variations in human hearing).
13. Assume a tone control high frequency boost of 10 dB at 10 kHz from Figure 7. Again determine relative response of octave midpoints.
14. Multiply all relative gain values of steps 11-13 and square the result.
15. Multiply the sum of the squared values from step 10 by the resultant relative gain of step 14 and by the bandwidth in each octave.
16. Sum all the values resultant from step 15, and find the square root of the sum. This is the total audible rms noise apparent in the band.
17. Divide $e_{sig}$ = 4 mV by the total noise to find S/N = 69.5 dB.

**Steps for Example**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Frequency Band (Hz) | 50-100 | 100-200 | 200-400 | 400-800 | 800-1600 | 1.6-3.2k | 3.2-6.4k | 6.4-12.8k |
| | Bandwidth, B (Hz) | 50 | 100 | 200 | 400 | 800 | 1600 | 3200 | 6400 |
| | Bandcenter, f (Hz) | 75 | 150 | 300 | 600 | 1200 | 2400 | 4800 | 9600 |
| 5 | $Z_{gen}$ at f (ohms) | 1355 | 1425 | 1665 | 2400 | 4220 | 8100 | 16k | 32k |
| | $Z_{gen}$ R1 (ohms) | 1300 | 1360 | 1600 | 2270 | 3900 | 6900 | 11.9k | 19k |
| | $Z_{gen}/(R1 + Z_{gen})$ | 0.028 | 0.030 | 0.034 | 0.485 | 0.082 | 0.145 | 0.255 | 0.400 |
| | $R1/(R1 + Z_{gen})$ | 0.97 | 0.97 | 0.97 | 0.95 | 0.92 | 0.86 | 0.74 | 0.60 |
| 11 | RIAA Gain, $A_{RIAA}$ | 5.6 | 3.1 | 2.0 | 1.4 | 1 | 0.7 | 0.45 | 0.316 |
| 12 | Corr for Hearing, $A_A$ | 0.08 | 0.18 | 0.45 | 0.80 | 1 | 1.26 | 1 | 0.5 |
| 13 | H-F Boost, $A_{boost}$ | 1 | 1 | 1 | 1 | 1.12 | 1.46 | 2.3 | 3.1 |
| 14 | Product of Gains, A | 0.45 | 0.55 | 0.9 | 1.12 | 1.12 | 1.28 | 1.03 | 0.49 |
| | $A^2$ | 0.204 | 0.304 | 0.81 | 1.26 | 1.26 | 1.65 | 1.06 | 0.241 |
| 4 | $\bar{e}_R$ ($nV/\sqrt{Hz}$) | 4.5 | 4.5 | 4.5 | 4.5 | 4.5 | 4.5 | 4.5 | 4.5 |
| 7 | $\bar{e}_{47k}$ ($nV/\sqrt{Hz}$) | 29 | 29 | 29 | 29 | 29 | 29 | 29 | 29 |
| 3 | $\bar{i}_n$ ($pA/\sqrt{Hz}$) | 0.85 | 0.80 | 0.77 | 0.72 | 0.65 | 0.62 | 0.60 | 0.60 |
| 2 | $\bar{e}_n$ ($nV/\sqrt{Hz}$) | 19 | 14 | 11 | 10 | 9.5 | 9 | 9 | 9 |
| 9 | $\bar{e}_1 = \bar{i}_n (Z_{gen}\ R1)$ | 1.1 | 1.09 | 1.23 | 1.63 | 2.55 | 4.3 | 7.1 | 11.4 |
| 6 | $\bar{e}_2 = \bar{e}_R\ R1/(R1 + Z_{gen})$ | 4.35 | 4.35 | 4.35 | 4.25 | 4.15 | 3.86 | 3.33 | 2.7 |
| 8 | $\bar{e}_3 = \bar{e}_{47k}\ Z_{gen}/(R1 + Z_{gen})$ | 0.81 | 0.87 | 0.98 | 1.4 | 2.4 | 4.2 | 7.4 | 11.6 |
| 10 | $\overline{e_n^2}$ | 360 | 195 | 121 | 100 | 90 | 81 | 81 | 81 |
| | $\overline{e_1^2}$ (from $\bar{i}_n$) | 1.21 | 1.2 | 1.5 | 2.65 | 6.5 | 18.5 | 50 | 150 |
| | $\overline{e_2^2}$ (from $\bar{e}_R$) | 19 | 19 | 19 | 18 | 17 | 15 | 11 | 7.2 |
| | $\overline{e_3^2}$ (from $\bar{e}_{47k}$) | 0.65 | 0.76 | 0.96 | 2 | 5.8 | 18 | 55 | 135 |
| | $\Sigma\ \overline{e_n^2}$ ($nV^2/Hz$) | 381 | 216 | 142 | 122 | 120 | 133 | 147 | 373 |
| 15 | $BA^2$ (Hz) | 10.2 | 30.4 | 162 | 504 | 1010 | 2640 | 3400 | 1550 |
| | $BA^2 \Sigma \overline{e^2}$ ($nV^2$) | 3880 | 6550 | 23000 | 61500 | 121000 | 350000 | 670000 | 580000 |
| 16 | $\Sigma (\overline{e_{n_i}^2} + \overline{e_{1_i}^2} + \overline{e_{2_i}^2} + \overline{e_{3_i}^2})\ B_i A_i^2 = 1{,}815{,}930\ nV^2$ | | | | | | | | |
| | $\bar{e}_N = \sqrt{\Sigma} = 1.35\mu V$ | | | | | | | | |
| 17 | $S/N = 20 \log (4.0\ mV/1.35\mu V) = 69.5\ dB$ | | | | | | | | |

Note the significant contributions of $\bar{i}_n$ and the 47k resistor, especially at high frequencies. Note also that there will be a difference between calculated noise and that noise measured on broadband meters because of the A curve employed in the example. If it were not for the A curve attenuation at low frequencies, the $\bar{e}_n$ would add a very important contribution below 200 Hz. This would be due to the RIAA boost at low frequency. As it stands, 97% of the 1.35$\mu$V would occur in the 800-12.8 kHz band alone, principally because of the high frequency boost and the A measurement curve. If the measurement were made without either the high frequency boost or the A curve, the $\bar{e}_n$ would be 1.25$\mu$V. In this case, 76% of the total noise would arise in the 50 Hz-400 Hz band alone. If the A curve were used, but the high frequency boost were deleted, $\bar{e}_n$ would be 0.91$\mu$V; and 94% would arise in the 800-12, 800 Hz band alone.

The three different methods of measuring would only produce a difference of +3.5 dB in overall S/N, however the prime sources of the largest part of the noise and the frequency character of the noise can vary greatly with the test or measurement conditions. It is, then, quite important to know the method of measurement in order to know which individual noise sources in Figure 6 must be reduced in order to significantly improve S/N.

## CONCLUSIONS

The main points in selecting low noise preamplifiers are:

1. Don't pad the signal source; live with the existing $R_{gen}$.
2. Select on the basis of low values of $\bar{e}_n$ and especially $\bar{i}_n$ if $R_{gen}$ is over about a thousand ohms.
3. Don't select on the basis of NF or $R_{OPT}$ in most cases. NF specs are all right so long as you know precisely how to use them and so long as they are valid over the frequency band for the $R_{gen}$ or $Z_{gen}$ with which you must work.
4. Be sure to (root) sum all the noise sources $\bar{e}_n$, $\bar{i}_n$ and $\bar{e}_R$ in your system over appropriate bandwidth.
5. The higher frequencies are often the most important unless there is low frequency boost or high frequency attenuation in the system.
6. Don't forget the filtering effect of the human ear in audio systems. Know the eventual frequency emphasis or filtering to be employed.

**APPENDIX I**

Derivation of $R_{OPT}$:

$$NF = 10 \log \frac{\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}$$

$$10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2} R_{gen}^2}{\overline{e_R^2}}\right)$$

$$\frac{\partial NF}{\partial R} = \frac{0.435}{(4kTRB)^2} \frac{4\,kTRB\,(2R\,\overline{i_n^2}) - (\overline{e_n^2} + \overline{i_n^2} R^2)4kTB}{1 + (\overline{e_n^2} + \overline{i_n^2} R^2)/4kTRB}$$

where: $R = R_{gen}$

Set this = 0, and

$$4kTRB(2R\overline{i_n^2}) = 4kTB(\overline{e_n^2} + \overline{i_n^2} R^2)$$

$$2\overline{i_n^2} R^2 = \overline{e_n^2} + \overline{i_n^2} R^2$$

$$\overline{i_n^2} R^2 = \overline{e_n^2}$$

$$R^2 = \overline{e_n^2} / \overline{i_n^2}$$

$$R_{OPT} = \frac{\bar{e}_n}{\bar{i}_n}$$

**APPENDIX II**

Selecting $R_{gen}$ for highest S/N.

$$S/N = \frac{e_{sig}^2}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2)}$$

For S/N to increase with R,

$$\frac{\partial S/N}{\partial R} > 0$$

$$\frac{\partial S/N}{\partial R} = \frac{2e_{sig}(\partial e_{sig}/\partial R)(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2) - e_{sig}^2 (4kT + 2\overline{i_n^2} R)}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2} R^2)^2}$$

**APPENDIX II (Con't)**

if we set $> 0$, then

$$2\,(\partial\, e_{sig}/\partial\, R)\,(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\,R^2) > e_{sig}\,(4kT + 2\overline{i_n^2}\,R)$$

For $e_{sig} = k_1\sqrt{R}$, $\quad \partial e_{sig}/\partial R = \dfrac{k_1}{2\sqrt{R}}$

$$(2k_1/2\sqrt{R})\,(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\,R^2) > k_1\sqrt{R}\,(4kT + 2\overline{i_n^2}\,R)$$

$$\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\,R^2 > 4kTR + 2\overline{i_n^2}\,R^2$$

$$\overline{e_n^2} > \overline{i_n^2}\,R^2$$

$$R < \bar{e}_n/\bar{i}_n$$

Therefore S/N increases with $R_{gen}$ so long as $R_{gen} \leq R_{OPT}$

For $e_{sig} = k_1 R$, $\partial e_{sig}/\partial R = k_1$

$$2k_1\,(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\,R^2) > k_1 R\,(4kT + 2\overline{i_n^2}R)$$

$$2\overline{e_R^2} + 2\overline{e_n^2} + 2\overline{i_n^2}\,R^2 > 4kTR + 2\overline{i_n^2}\,R^2$$

$$\overline{e_R^2} + 2\overline{e_n^2} > 0$$

Then S/N increases with $R_{gen}$ for any amplifier.

For any $e_{sig} < k_1\sqrt{R}$, an optimum $R_{gen}$ may be determined. Take, for example, $e_{sig} = k_1 R^{0.4}$, $\partial e_{sig}/\partial R = 0.4k_1 R^{-0.6}$

$$(0.8k_1/R^{0.6})(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\,R^2) > k_1 R^{0.4}\,(4kT + 2\overline{i_n^2}R)$$

$$0.8\,\overline{e_R^2} + 0.8\,\overline{e_n^2} + 0.8\,\overline{i_n^2}\,R^2 > 4kTR + 2\,\overline{i_n^2}\,R^2$$

$$0.8\,\overline{e_n^2} > 0.2\,\overline{e_R^2} + 1.2\,\overline{i_n^2}\,R^2$$

Then S/N increases with $R_{gen}$ until

$$0.25\,\overline{e_R^2} + 1.5\,\overline{i_n^2}\,R^2 = \overline{e_n^2}$$

Robert Dobkin
MAY 1974

# FAST IC POWER TRANSISTOR WITH THERMAL PROTECTION

## INTRODUCTION

Overload protection is perhaps most necessary in power circuitry. This is shown by recent trends in power transistor technology. Safe-area, voltage and current handling capability have been increased to limits far in excess of package power dissipation. In RF transistors, devices are now available and able to withstand badly mismatched loads without destruction. However, for anyone working with power transistors, they are still easily destroyed.

Since power circuitry, in many cases, drives other low level circuitry—such as a voltage regulator—protection is doubly important. Overloads that cause power transistor failure can result in the destruction of the entire circuit. This is because the common failure mode for power transistors is a short from collector to emitter—applying full voltage to the load. In the case of a voltage regulator, the raw supply voltage would be applied to the low level circuitry.

A new monolithic power transistor provides virtually absolute protection against any type of overload. Included on the chip are current limiting, safe area protection and thermal limiting. Current limiting controls the peak current through the chip to a safe level below the fuzing current of the aluminum metalization. At high collector to emitter voltage the safe area limiting reduces the peak current to further protect the power transistor. If, under prolonged overload, power dissipation causes chip temperature to rise toward destructive levels, thermal limiting turns off the device keeping the devices at a safe temperature. The inclusion of thermal limiting, a feature not easily available in discrete circuitry makes this device especially attractive in applications where normal protective schemes are ineffective.

The device's high gain and fast response further reduce requirements of surrounding circuitry. As well as being used in linear applications, the IC can interface transistor-transistor logic or complementary-MOS logic to power loads without external devices. In fact, the input-current requirement of 3 microamperes is small enough for one CMOS gate to drive over 400 LM195's.

Besides high dc current gain, the IC has low input capacitance so it can be easily driven from high impedance sources—even at high frequencies. In a standard TO-3 power package, the monolithic structure ties the emitter, rather than the collector, to the case effectively bootstrapping the base-to-package capacitance. Additionally, connecting the emitter to the package is especially convenient for grounded emitter circuits.

The device is fully protected against any overload condition when it is used below the maximum voltage rating. The current-limiting circuitry restricts the power dissipation to 35 watts, 1.8 amperes are available at collector-to-emitter voltage of 17V decreasing to about 0.8 amperes at 40V. In reality, however, like standard transistors, power dissipation in actual use is limited by the size of the external heat sink.

Switching time is fast also. At 40V 25 Ohm load can be switched on or off in a relatively fast 500 ns. The internal planar double diffused monolithic transistors have an $f_t$ of 200 MHz to 400 MHz. The limiting factor on overall speed is the protective and biasing circuitry around the output transistors. An important performance point is that no more than the normal 3μA base current is needed for fast switching.

To the designer, the LM195 acts like an ordinary power transistor, and its operation is almost identical to that of a standard power device. However, it provides almost absolute protection against any type of overload. And, since it is manufactured with standard seven-mask IC technology, the device is produceable in large quantities at reasonable cost.

## CIRCUIT DESIGN

Besides the protective features, the monolithic power transistor should function as closely to a discrete transistor as possible. Of course, due to the circuitry on the chip, there will be some differences.

*Figure 1* shows a simplified schematic of the power transistor. A power NPN Darlington is driven by an input PNP. The PNP and output NPN's are biased by internal current source $I_1$. The composite three transistors yield a total current gain in excess of $10^6$ making it easy to drive the power transistors from high impedance sources. Unlike normal power transistors, the base current is negative, flowing out of the PNP. However, in most cases this is not a problem.

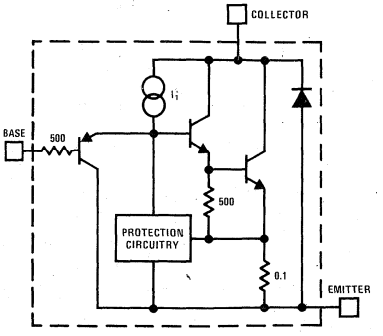



**FIGURE 1. Simplified Circuit of the LM195**

The input PNP transistor is made with standard IC processing and has a reverse base-emitter breakdown voltage in excess of 40V. This allows the power transistor to be driven from a stiff voltage source without damage due to excessive base current. At input voltages in excess of about 1V the input PNP becomes reverse biased and no current is drawn from the base lead. In fact it is possible for the base of the monolithic transistor to be driven with up to 40V even though the collector to emitter voltage is low. Further, the input PNP isolates the base drive from the protective circuitry insuring that even with high base drive the device will be protected. When the device is turned off current $I_1$ is shunted from the base of the NPN transistor by the PNP and appears at the emitter terminal. This sets the minimum load current to about 2 mA, not a severe restriction for a power transistor. Because of the PNP and $I_1$, the power transistor turns "on" rather than "off" if the base is opened; however, most power circuits already include a base-emitter resistor to absorb leakage currents in present power transistors.

A schematic of the LM195 is shown in *Figure 2*. The circuitry is biased by four current sources comprised of Q4, Q7, Q8 and Q9. The operating current is set by Q5 and Q6 and is relatively independent of supply voltage. FET Q1 and R2 insure reliable starting of the bias circuitry while D1 clamps the output of the FET limiting the starting current at high supply voltage.

The output transistors Q19 and Q20 are driven from input PNP Q14. Current limiting independent of temperature changes is provided by Q21, Q16, and Q15. At high collector to emitter voltages the current limit decreases due to the voltage across R21 from D3, D4 and R20. The double emitter structure used on Q21 allows the power limiting to more closely approximate constant power curve rather than a straight line decrease in output current as input voltage increases.

Transistor Q13 thermally limits the device by removing the base drive at high temperature. The actual temperature sensing is done by Q11 and Q12 with Q10 regulating the voltage across the sensors so thermal limit temperature remains independent of supply. As temperature increases, the collector current of Q11 increases while the $V_{BE}$ of Q12 decreases. At about 170°C the Q12 turns on Q13 removing the base drive from the output transistors. Finally, C1, Q2 and Q3 boost operating currents during switching to obtain faster response time and Q17 and Q18 compensate for $h_{fe}$ variations in the power devices.

## PERFORMANCE

The new power transistor is packaged in a standard TO-3 transistor package making it compatible with standard power transistors. An added advantage of the monolithic structure is that the emitter is tied to the case rather than the collector. This allows the device to be connected directly to ground in collector output applications.

A photomicrograph of the LM195 is shown in *Figure 3*. More than half of the die area is needed for the output power transistor (Q20). Actually, the power transistor is many individual small transistors connected in parallel with a common collector. Partitioning the power device into small discrete areas improves power handling over a single large device. Firstly, the power device has ten base sections spread across the chip. Between the base diffusion are N+ collector contacts. Each section has its own emitter ballasting resistor to insure current sharing between sections. One of these resistors is used to sense the output current for current limiting.

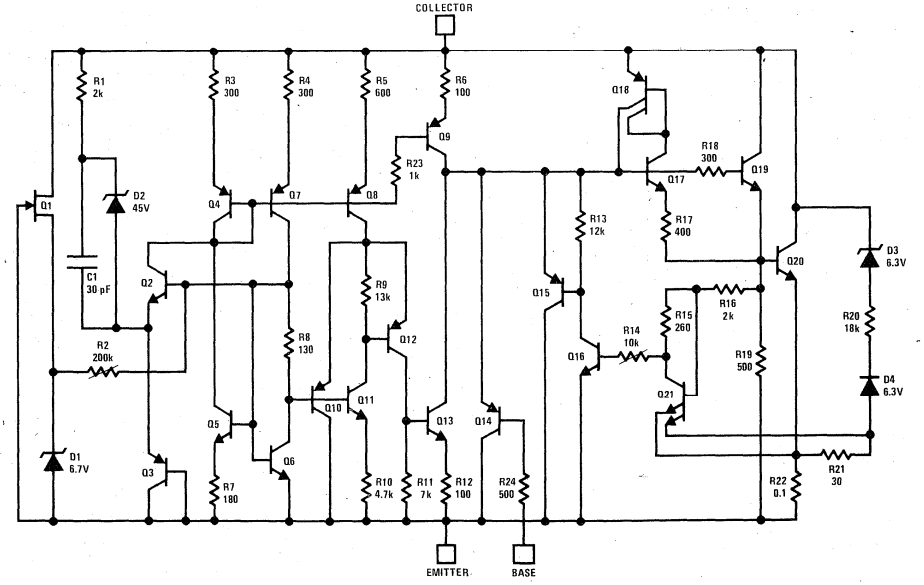



**FIGURE 2. Schematic Diagram of the LM195**

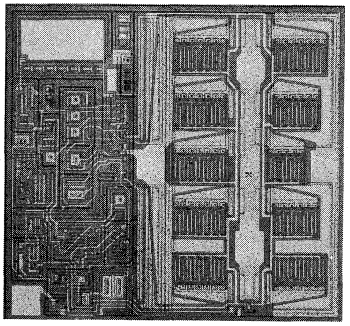


**FIGURE 3. LM195 Chip**

**TABLE I. Typical Performance**

| | |
|---|---|
| Collector to Emitter Voltage | 42V |
| Base to Emitter Voltage (max.) | 42V |
| Peak Collector Current (internally limited) | 1.8 amps |
| Reverse Base Emitter Voltage | 20V |
| Base to Emitter Voltage ($I_C$ = 1.0 amp) | 0.9V |
| Base Current | 3μA |
| Saturation Voltage | 2V |
| Switching Time (turn on or turn off) | 500 ns |
| Power Dissipation (internally limited) | 35 watts |
| Thermal Limit Temperature | 165°C |
| Maximum Operating Temperature | 150°C |
| Thermal Resistance (Junction to Case) | 2.3°C/W |

A detail of one of the base sections is shown in *Figure 4.* An interdigitated structure is used with alternating base contacts and emitter stripes. Integrated into each emitter is an individual emitter ballasting resistor to insure equal current sharing between emitters in each section. Aluminum metalization runs the length of the emitter stripe to prevent lateral voltage drop from debiasing a section of the stripe at high operating currents. All current in the stripe flows out through the small ballasting resistor where it is summed with the currents from the other stripes in the section. The partitioning in conjunction with the emitter resistor gives a power transistor with large safe-area and good power handling capability.

## APPLICATIONS

With the full protection and high gain offered by this monolithic power transistor, circuit design is considerably simplified. The inclusion of thermal limiting, not normally available in discrete design allows the use of smaller heat sinks than with conventional protection circuitry. Further, circuits where protection of the power device is difficult—if not impossible—now cause no problems.

For example, with only current limiting, the power transistor heat sink must be designed to dissipate worst case overload power dissipation at maximum ambient temperature. When the power transistor is thermally limited, only normal power need be dissipated by the heat sink. During overload, the device is allowed to heat up and thermally limit, drastically reducing the size of the heat sink needed.

Switching circuits such as lamp drivers, solenoid drivers or switching regulators do not dissipate much power during normal operation and usually no heat sink is necessary. However, during overload, the full supply voltage times the maximum output current must be dissipated. Without a large heat sink standard power transistors are quickly destroyed.

Using this new device is easier than standard power transistors but a few precautions should be observed. About the only way the device can be destroyed is excessive collector to emitter voltage or improper power supply polarity. Sometimes when used as an emitter follower, low level high frequency oscillations can occur. These are easily cured inserting a 5k-10k resistor in series with the base lead. The resistor will eliminate the oscillation without effecting speed or performance. Good power supply bypassing should also be used since this is a high frequency device.

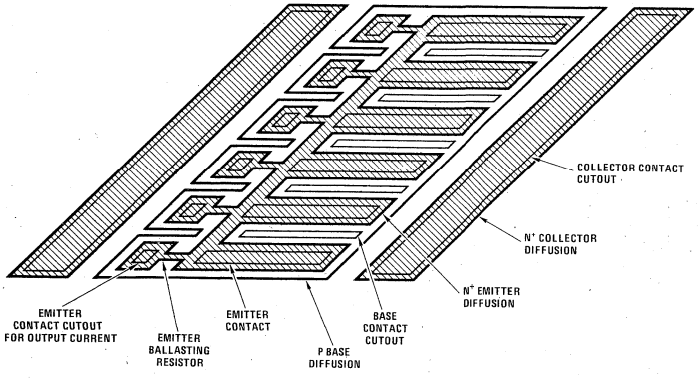



**FIGURE 4. Detailed Structure of one Section of the Power Transistor**

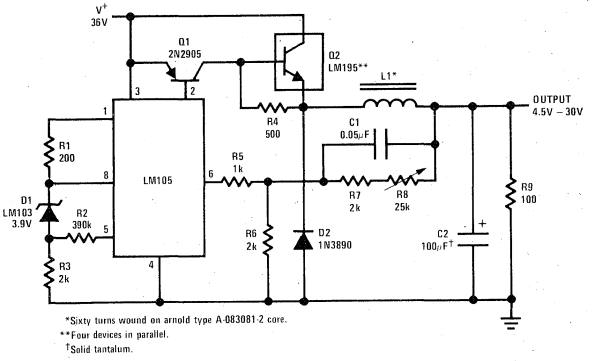



**FIGURE 5. 6 Amp Variable Output Switching Regulator**

*Figure 5* shows a 6 amp, variable output switching regulator for general purpose applications. An LM105 positive regulator is used as the amplifier-reference for the switching regulator. Positive feedback to induce switching is obtained from the LM105 at pin 1 through an LM103 diode. The positive feedback is applied to the internal amplifier at pin 5 and is independent of supply voltage. This forces the LM105 to drive the pass devices either "on" or "off," rather than linearly controlling their conduction. Negative feedback, delayed by L1 and the output capacitor, C2, causes the regulator to switch with the duty cycle automatically adjusting to provide a constant output. Four LM195's are used in parallel to obtain a 6 amp output since each device can only supply about 2 amps. Note that no ballasting resistors are needed for current sharing. When Q1 turns "on" all bases are pulled up to $V^+$ and no base current flows in the LM195 transistors since the input PNP's are reverse biased.

A two terminal current/power limiter is shown in *Figure 6*. The base and collector are shorted—turning the power transistor on. If the load current exceeds 2 amps, the device current limits protecting the load. If the overload remains on, the device will thermal limit, further protecting itself and the load. In normal operation, only 2V appear across the device so high efficiency is realized and no heat sink is needed. Another method of protection would be to place the monolithic power transistor on a common heat sink with the devices to be protected. Overheating will then cause the LM195 to thermal limit protecting the rest of the circuitry.

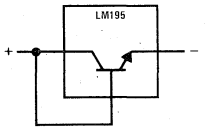



**FIGURE 6. Two Terminal Current Limiter**

The low base current make this power device suitable for many unique applications. *Figure 7* shows a time delay circuit. Upon application of power or S1 closing, the load is energized. Capacitor C1 slowly charges toward $V^-$ through R1. When the voltage across R1 decreases below about 0.8 volts the load is de-energized. Long delays can be obtained with small capacitor values since a high resistance can be used.

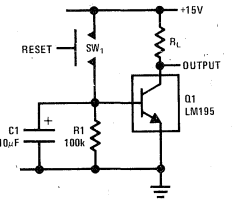



**FIGURE 7. Time Delay Circuit**

*Figure 8 and 9* show how the LM195 can be used with standard IC's to make positive or negative voltage regulators. Since the current gain of the LM195 is so high, both regulators have better than 2 mV load regulation. They are both fully overload protected and will operate with only 2V input-to-output voltage differential.

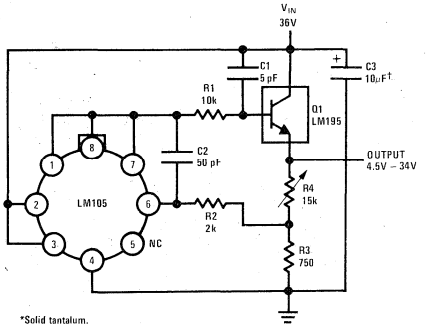



**FIGURE 8. 1 Amp Positive Voltage Regulator**

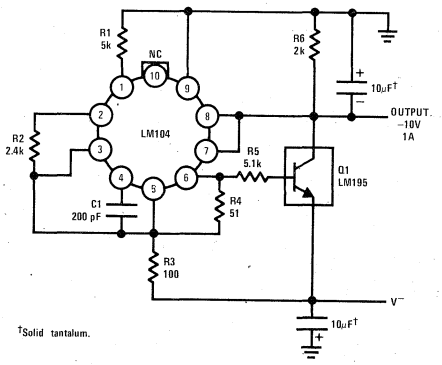



**FIGURE 9. 1 Amp Negative Regulator**

An optically isolated power transistor is shown in *Figure 10.* D1 and D2 are almost any standard optical isolator. With no drive, R1 absorbs the base current of Q1 holding it off. When power is applied to the LED, D2 allows current to flow from the collector to base. Less than 20μA from the diode is needed to turn the LM195 fully on.

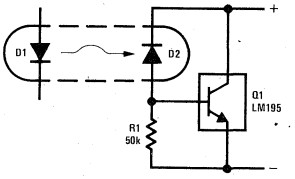



**FIGURE 10. Optically Isolated Power Transistor**

An alternate connection for better ac response is to return the cathode of D2 to separate positive supply rather than the collector of Q1, as shown in *Figure 11,* eliminating the added collector to base capacitance of the diode. With this circuit a 40V 1 amp load can be switched in 500 ns. Of course, any photosensitive diode can be used instead of the opto-isolator to make a light activated switch.

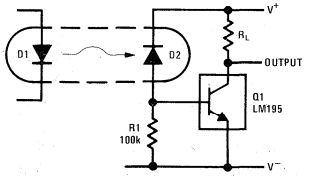



**FIGURE 11. Fast Optically Isolated Switch**

A power lamp flasher is shown in *Figure 12.* It is designed to flash a 12V bulb at about a once-per-second rate. The reverse base current of Q2 provides biasing for Q1 eliminating the need for a resistor. Typically, a cold bulb can draw 8 times its normal operating current. Since the LM195 is current limited, high peak currents to the bulb are not experienced during turn-on. This prolongs bulb life as well as easing the load on the power supply.

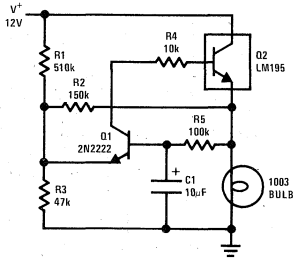



**FIGURE 12. 1 Amp Lamp Flasher**

Since no PNP equivalent of this device is available, it is advantageous to use the LM195 in a quasi-complementary configuration to simulate a power PNP. *Figure 13* shows a quasi PNP made with an LM195. A low current PNP is used to drive the LM195 as the power output device. Resistor R1 protects against overdrive destroying the PNP and, in conjunction with C1, frequency compensates the loop against oscillations. Resistor R2 sets the operating current for the PNP and limits the collector current.

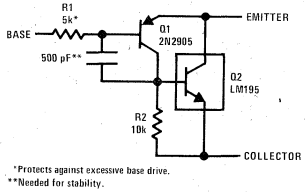



**FIGURE 13. PNP Configuration for LM195**

*Figure 14* shows a power op amp with a quasi-complementary power output stage. Q1 and Q2 form the equivalent of a power PNP. The circuit is simply an op amp with a power output stage. As shown, the circuit is stable for almost any load. Better bandwidth can be obtained by decreasing C1 to 15 pF (to obtain 150 kHz full output response), but capacitive loads can cause oscillation. If due to layout, the quasi-complimentary loop oscillates, collector to base capacitance on Q1 will stabilize it. A simpler power op amp for up to 300 Hz operation is shown in *Figure 15.*

One of the more difficult circuit types to protect is a current regulator. Since the current is already fixed, normal protection doesn't work. Circuits to limit the voltage across the current regulator may allow excessive current to flow through the load. About the only protection method that protects both the regulator and the driven circuit is thermal limiting.

A 100 mA, two terminal regulator is shown in *Figure 16.* The circuit has low temperature coefficient and operates

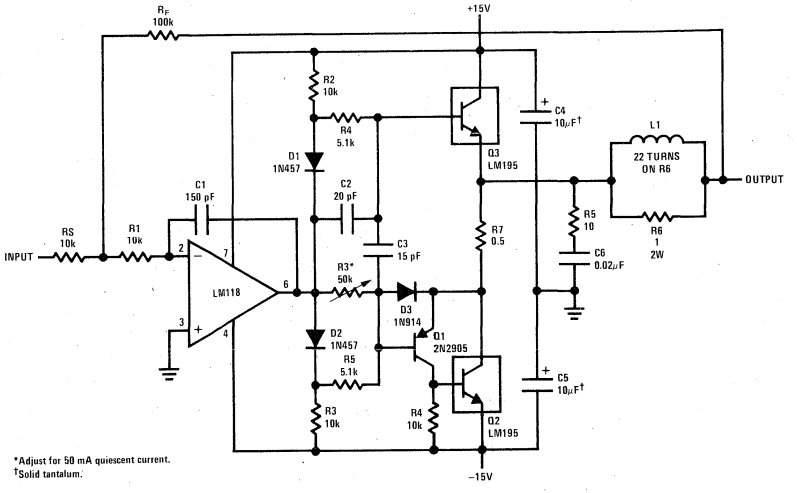



**FIGURE 14. Power Op Amp**

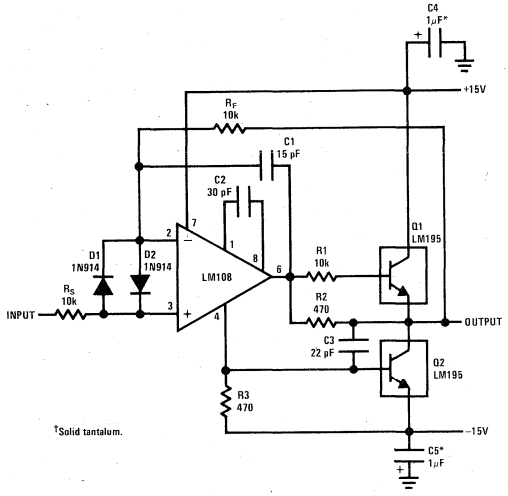



**FIGURE 15. 1 Amp Voltage Follower**

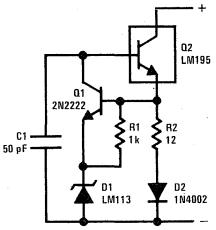



**FIGURE 16. Two Terminal 100 mA Current Regulator**

down to 3V. Once again, the reverse base current of the LM195 to bias the operating circuitry.

A 2N2222 is used to control the voltage across a current sensing resistor, R2 and diode D1, and therefore the current through it. The voltage across the sense network is the $V_{BE}$ of the 2N2222 plus 1.2V from the LM113. In the sense network R2 sets the current while D1 compensates for the $V_{BE}$ of the transistor. Resistor R1 sets the current through the LM113 to 0.6 mA.

## CONCLUSIONS

A new IC power transistor has been developed that significantly improves power circuitry reliability. The device is virtually impossible to destroy through abuse. Further it has high gain and fast response. It is manufactured with standard seven mask IC technology making it produceable in large quantities at reasonable prices. Finally, in addition to the protection features, it has high gain simplifying surrounding circuitry.

Robert C. Dobkin
JULY 1974

## WIDE RANGE FUNCTION GENERATOR

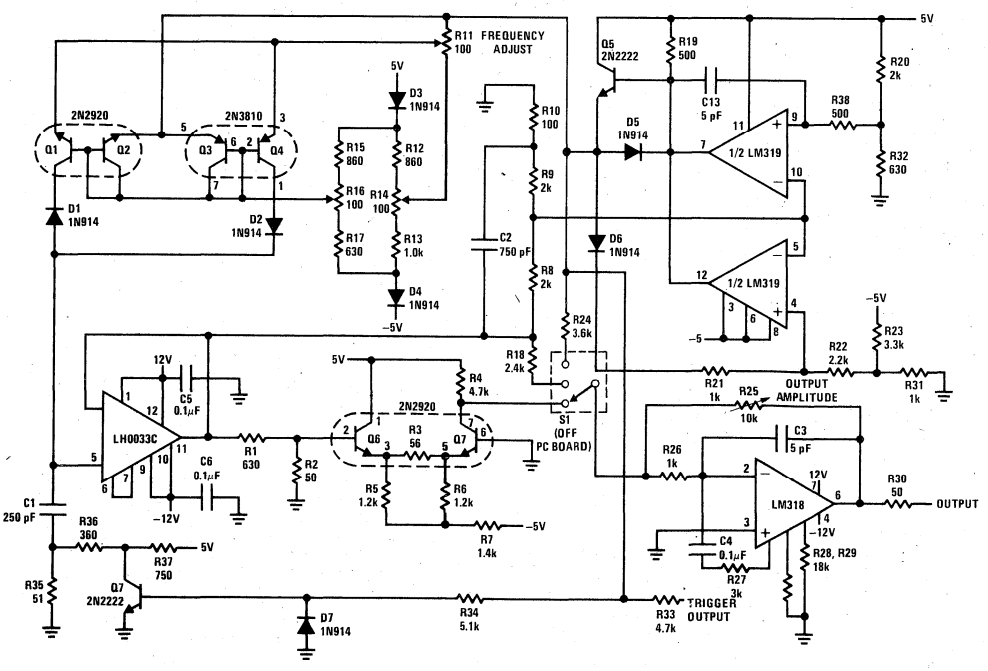
The sine, square, triangle function generator has proven to be exceptionally useful. Various IC circuits have been published for generating square and triangle waveforms in an attempt to duplicate the general purpose function generator. However, these simple circuits are usually limited to about 10 kHz and have no sine wave output. The function generator shown here provides all three waveforms and operates from below 10 Hz to 1 MHz with usable output to about 2 MHz.

### DESIGN

As with most function generators, an integrator-comparator generates the square and triangle waveforms with a shaping circuit forming the triangle wave into a sine wave.

Obtaining six decades of operating with a single control plus 2 MHz operation requires some unusual circuit design techniques as well as good high frequency IC's. The triangle wave is generated by switching current-source transistors to alternately charge and discharge the timing capacitor. This generates a linear tri-wave without the use of an op amp integrator. A FET voltage follower buffers the tri-wave and drives the comparator, output amplifier and sine converter.

A precision dual comparator is used to set the peak-to-peak amplitude of the tri-wave. It is necessary to accurately control the tri-wave since the sine converter requires close amplitude control to produce a low distortion output. An accurate divider across the 5V supply regulators sets the threshold at the inputs of the LM319 comparator. The tri-wave is applied to the other comparator inputs through another divider—R8, R9, R10 and C2. The comparator switches when the amplitude of the tri-wave is ±2.5V. Capacitor C2 compensates for delays in the comparator at high frequencies.




**Function Generator Schematic**

## PARTS LIST

| | | | | | |
|---|---|---|---|---|---|
| R1 | 630Ω | 1% | C1 | 250 pF | |
| R2 | 50Ω | 1% | C2 | 750 pF | |
| R3 | 56Ω | 5% | C3 | 5 pF | |
| R4 | 4.7k | 5% | C4 | 0.1μF | |
| R5 | 1.2k | 1% | C5 | 0.1μF | |
| R6 | 1.2k | 1% | C6 | 0.1μF | |
| R7 | 1.4k | 1% | C7 | 500μF | 25V |
| R8 | 2k | 5% | C8 | 500μF | 25V |
| R9 | 2k | 5% | C9 | 4.7μF | Solid Tantalum |
| R10 | 100Ω | 5% | C10 | 4.7μF | Solid Tantalum |
| R11 | 100Ω potentiometer | | C11 | 4.7μF | Solid Tantalum |
| R12 | 860Ω | 5% | C12 | 4.7μF | Solid Tantalum |
| R13 | 1k | 5% | C13 | 5 pF | |
| R14 | 100Ω PC mount trimpot | | | | |
| R15 | 860Ω | 5% | | | |
| R16 | 100Ω PC mount trimpot | | Q1–Q2 | 2N2920 | Dual NPN |
| R17 | 630Ω | 5% | Q3–Q4 | 2N3810 | Dual PNP |
| R18 | 2.4k | 5% | Q5 | 2N2222 | |
| R19 | 500Ω | 5% | Q6–Q7 | 2N2920 | Dual NPN |
| R20 | 2k | 5% | Q8 | 2N2222 | |
| R21 | 1k | 5% | | | |
| R22 | 2.2k | 5% | D1–D7 | 1N914 | |
| R23 | 3.3k | 5% | 1–Varo VE27 Full Wave Bridge | | |
| R24 | 3.6k | 5% | | | |
| R25 | 10k potentiometer | | 1–LM318H Operational Amplifier | | |
| R26 | 1k | 5% | 1–LM319N Dual Comparator | | |
| R27 | 3k | 5% | 1–LH0033C Fast Buffer | | |
| R28 | 18k | 5% | 1–LM340K | 12V | Positive Voltage Regulator |
| R29 | 18k | 5% | 1–LM320K | −12V | Negative Voltage Regulator |
| R30 | 50Ω | 5% | 1–LM309H | 5V | Positive Voltage Regulator |
| R31 | 1k | 5% | 1–LM320H | −5V | Negative Voltage Regulator |
| R32 | 630Ω | 5% | | | |
| R33 | 4.7k | 5% | TI = Triad F90X | | |
| R34 | 5.1k | 5% | | | |
| R35 | 51Ω | 5% | $S_1$–3 Position ST Switch | | |
| R36 | 360Ω | 5% | $S_2$–SPST Switch | | |
| R37 | 750Ω | 5% | | | |
| R38 | 500Ω | 5% | 1/4 Amp Fuse and Holder–PC Board, Mounting Hardware, etc. | | |

A square wave output from the comparator is obtained at the emitter of Q5 and is used to drive both the current switches and output amplifier. The current switches–Q1, Q2, Q3, Q4–provide a 5 nA to 5 mA current to timing capacitor, C1. The exponential relationship between emitter-base voltage and collector current allows a six decade current range to be obtained with a single potentiometer. The maximum output current is set by the current through R15 or R17 (depending on polarity) and appears when the arm of the frequency control, R11, ties all four emitters together. As R11 is rotated, a voltage is developed between the emitters of Q1–Q4 and Q2–Q3. This voltage decreases the emitter base voltage of Q1 and Q4 decreasing their operating current. About 380 mV is developed across R11 and corresponds to over a $10^6$ reduction in charging current.

Converting the tri-wave to a sine wave also uses the non-linear relationship between emitter-base voltage and collector current of a transistor pair.

Transistors Q6 and Q7 form a differential amplifier with emitter degeneration. The tri-wave is attenuated by R1 and R2 to about 450 mV and applied to one half of the pair–Q6. This drives the transistors non-linearly producing a sine wave output current at the collector of Q7 to drive the output amplifier.

The output amp, an LM318, uses feedforward compensation to maximize bandwidth and slew rate. It is used for adjustable scaling of all three waveforms to ±10V. Even with the feedforward, there is not quite enough bandwidth for good reproduction of the triangle or

square wave at frequencies over 1 MHz. Therefore, if the higher frequencies are of major interest, a faster output amplifier is necessary.

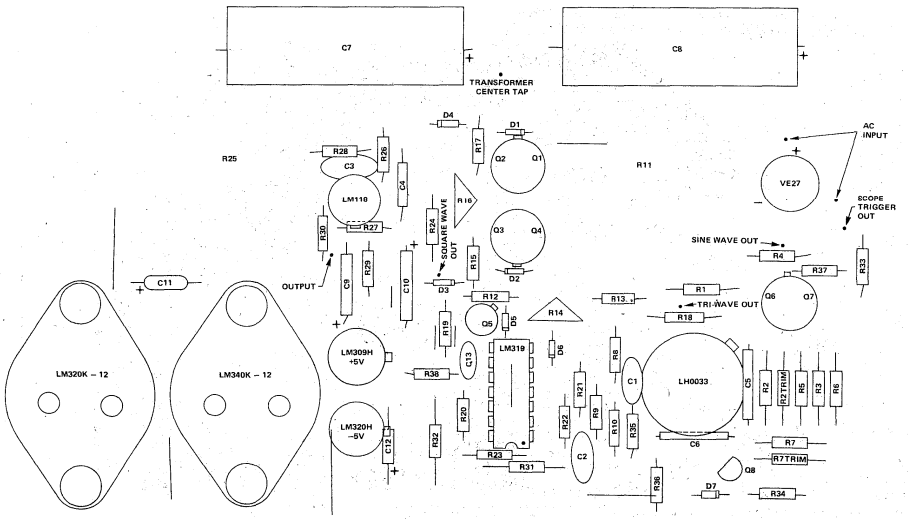
## CONSTRUCTION AND SET UP

It is important to observe good construction practices for proper operation. All four power supplies should be bypassed with 4.7$\mu$F solid tantalum capacitors on the circuit board. Since the circuit operates at relatively high frequencies, short leads and a compact layout is a good idea. The wiring to the function selector switch should be made with shielded wire to minimize spikes from the fast square wave. At low frequencies, charging currents to the timing capacitor are quite low, so 60 Hz pickup can modulate the operating frequency. Shielding the current sources and C1 from the power transformer is in order.

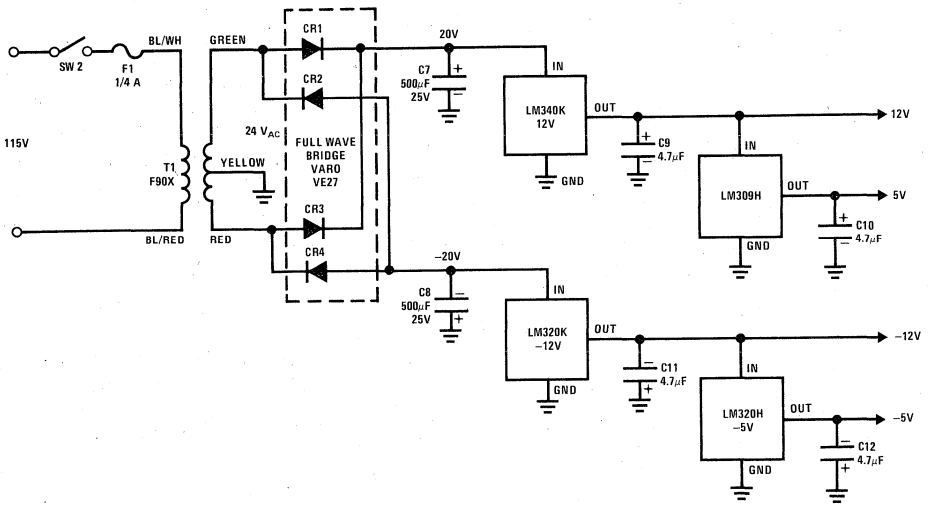
All transistors used to set the timing currents must track with temperature changes. Of course, the individual pairs will track but the NPN pair must also track the PNP pair as well. There are many small heat sinks for transistors which can be used to thermally couple Q1, Q2, to Q3, Q4. Temperature differences between the pair will cause the symmetry to change.

Set up is not difficult either. Firstly, R11 is set for a 1 MHz output. Then R16 is used to adjust the output symmetry. Secondly, R11 is set to provide a 10 Hz output and the symmetry is again adjusted by R14.

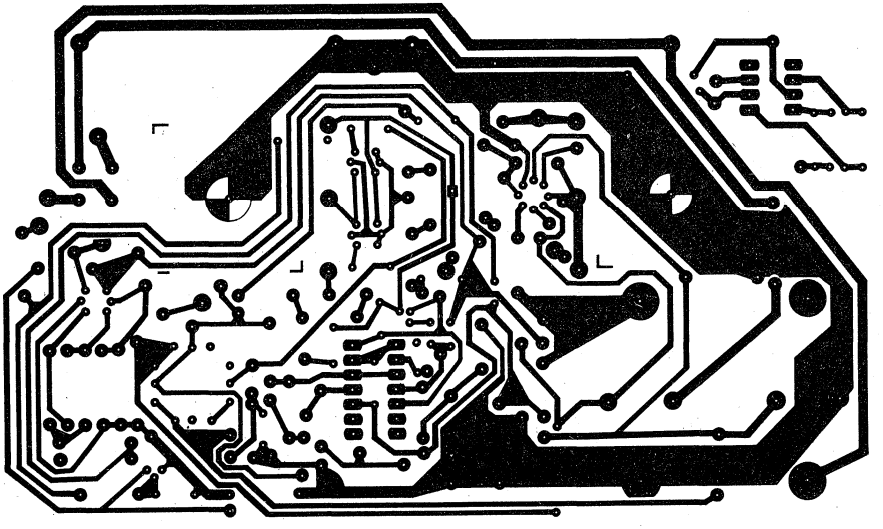
Other possible adjustments that may be necessary are in the sine converter. R7 can be trimmed if the sine output (from the LM318) has a dc offset. Also, it may be necessary to adjust R2 to minimize distortion. (It should be mentioned that there can be considerable distortion if the symmetry of the tri-wave is not 50%.)




**Component Location, Top View**




Power Supply Section Schematic



Circuit Board Layout
(This PC layout must be enlarged approximately 120% in order to be usable.)

Jim Sherwin
MAY 1974

# USE THE LM158/LM258/LM358 DUAL, SINGLE SUPPLY OP AMP

## INTRODUCTION

Use the LM158/LM258/LM358 dual op amp with a single supply in place of the MC1458/MC1558/MC1558C with split supply and reap the profits in terms of:

a. Input and output voltage range down to the negative (ground) rail
b. Single supply operation
c. Lower standby power dissipation
d. Higher output voltage swing
e. Lower input offset current
f. Generally similar performance otherwise.

The main advantage, of course, is that you can eliminate the negative supply in many applications and still retain equivalent op amp performance. Additionally, and in some cases more importantly, the input and output levels are permitted to swing down to ground (negative rail) potential. Table I shows the relative performance of the two in terms of guaranteed and/or typical specifications.

In many applications the LM158/LM258/LM358 can also be used directly in place of LM1558 for split supply operation.

## SINGLE SUPPLY OPERATION

The MC1458/MC1558 or similar op amps exhibit several important limitations when operated from a single positive (or negative) supply. Chief among these is that input and output signal swing is severely limited for a given supply as shown in *Figure 1*. For linear operation, the input voltage must not reach within 3 volts of ground or of the supply, and output range is similarly limited to within 3–5 volts of ground or supply. This means that operation with a +12V supply could be limited as low as 2 Vp-p output swing. The LM358 however, allows a 10.5 Vp-p output swing for the same 12V supply. Admittedly these are worst case specification limits, but they serve to illustrate the problem.

**TABLE I. Comparison of Dual Op Amps, MC1458 and LM358**

| CHARACTERISTIC | MC1458 | LM358 |
|---|---|---|
| $V_{IO}$ | 6 mV Max | 7 mV Max |
| CM $V_I$ | 24 Vp-p* | 0 – 28.5V* |
| $I_{IO}$ | 200 nA | 50 nA |
| $I_{OB}$ | 500 nA | –500 nA |
| CMRR | 60 dB Min @ 100 Hz<br>90 dB Typ | 85 dB Typ @ DC |
| $\overline{e}_n$ @ 1 kHz, $R_{GEN}$ 10 kΩ | 45 nV/$\sqrt{Hz}$ Typ | 40 nV/$\sqrt{Hz}$ Typ** |
| $Z_{IN}$ | 200 MΩ Typ | Typ 100 MΩ |
| $A_{VOL}$ | 20k Min<br>100k Typ | 100k Typ |
| $f_c$ | 1.1 MHz Typ | 1 MHz Typ** |
| $P_{BW}$ | 14 kHz Typ | 11 kHz Typ** |
| $dV_o/dt$ | 0.8V/μs Typ | 0.5V/μs Typ** |
| $V_o$ @ $R_L$ = 10k/2k | 24/20 Vp-p* | 28.5 Vp-p |
| $I_{SC}$ | 20 mA Typ | Source 20 mA Min (40 Typ)<br>Sink 10 mA Min (20 Typ) |
| PSRR @ DC | 37 dB Min<br>90 dB Typ | 100 dB Typ |
| $I_D$ ($R_L$ = ∞) | 8 mA Max | 2 mA Max |

‡From laboratory measurement
*Based on $V_S$ = 30V on LM358 only, or $V_S$ = ±15V
**From data sheet typical curves

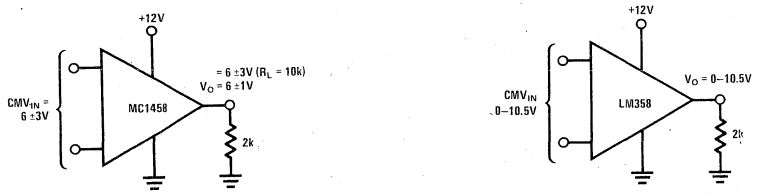



FIGURE 1. Worst Case Signal Levels with +12V Supply

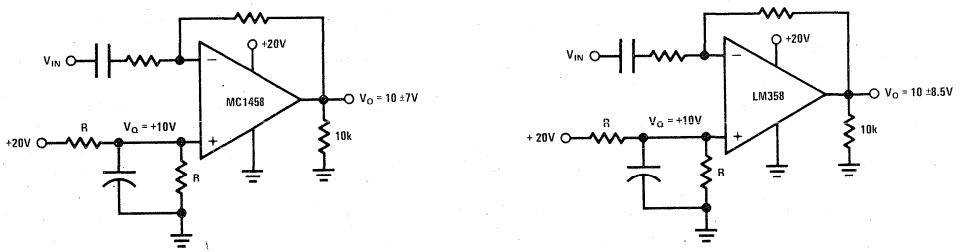



FIGURE 2. Operating with AC Signals

## AC GAIN

For ac signals the input can be capacitor coupled. The input common mode and quiescent output voltages are fixed at one-half the supply voltage by a resistive divider at the non-inverting input as shown in *Figure 2*. This quiescent output could be set at a lower voltage to minimize power dissipation in the LM358, if desired, so long as $V_Q \geq V_{IN}$ pk. For the MC1458 the quiescent output must be higher, $V_Q \geq 3V + V_{IN}$ pk thus, for small signals, power dissipation is much greater with the MC1458. Example: Required $V_O = V_Q \pm 1V$ pk into 2k, $V_{SUPPLY}$ = as required. Find quiescent dissipation in load and amplifier for MC1458 and LM358.

| LM358 | MC1458 |
|---|---|
| $V_Q = +1V$ | $V_Q = 4V$ |
| $V_{SUPPLY} = +3.5V$ | $V_{SUPPLY} = 8V$ |
| $P_{LOAD} = \frac{E_L^2}{R_L} = \frac{1}{2k} = 0.5$ mW | $P_{LOAD} = \frac{4^2}{2k} = 8$ mW |
| $P_D = V_S I_S^* + (V_S - V_Q) I_L$ | $P_D = P_D^* + (V_S - V_Q) I_L$ |
| $= 3.5V \times 0.7$ mA $+ (3.5 - 1) \frac{1V}{2k}$ | $= 22$ mW $+ (8 - 4) \frac{4V}{2k}$ |
| $P_D = 2.45 + 1.25 = 3.7$ mW | $P_D = 22 + 8 = 30$ mW |
| $P_{TOTAL} = 3.7 + 0.5 = 4.2$ mW | $P_{TOTAL} = 30 + 8 = 38$ mW |
| *From typical characteristics | *From typical characteristics |

The MC1458 requires over twice the supply voltage and nearly 10 times the supply power of the LM358 in this application.

## INVERTING DC GAIN

Connections and biasing for dc inverting gain are essentially the same as for the ac coupled case. Note, of course, that the output cannot swing negative when operated from a single positive supply. *Figure 3* shows the connections and signal limitations.

## NON-INVERTING DC GAIN

The non-inverting gain connection does not require the $V_Q$ biasing as before; the inverting input can be returned to ground in the usual manner for gains greater than unity, (see *Figure 4*). A tremendous advantage of the LM358 in this connection is that input signals and output may extend all the way to ground; therefore dc signals in the low-millivolt range can be handled. The MC1458 still requires that $V_{IN}$ = 3–17V. Therefore maximum gain is limited to $A_V = (V_O - 3)/3$, or $A_V$ max = 5.4 for a 20V supply.

There is no similar limitation for the LM358.

## ZERO T.C. INPUT BIAS CURRENT

An interesting and unusual characteristic is that $I_{IN}$ has a zero temperature coefficient. This means that matched resistance is not required at the input, allowing omission of one resistor per op amp from the circuit in most cases.

## BALANCED SUPPLY OPERATION

The LM358 will operate satisfactorily in balanced supply operation so long as a load is maintained from output to the negative supply.

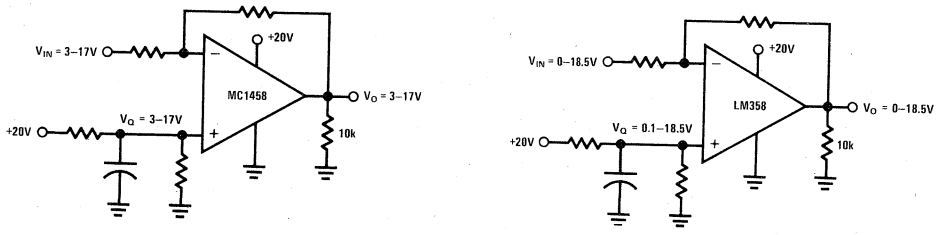



**FIGURE 3. Typical DC Coupled Inverting Gain**

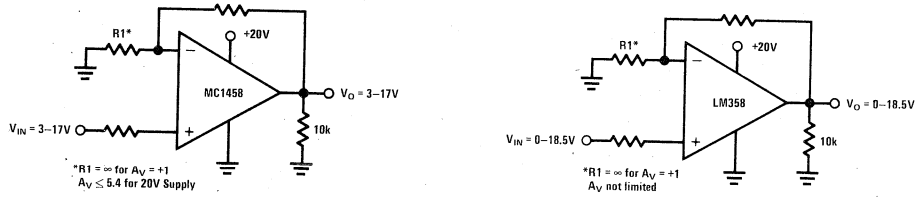



**FIGURE 4. Typical DC Coupled Non-Inverting Gain**

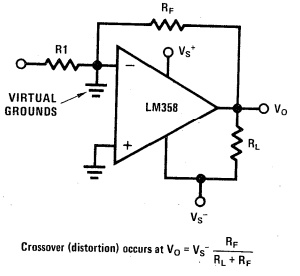



**FIGURE 5. Split Supply Operation of LM358**

The output load to negative supply forces the amplifier to source some minimum current at all times, thus eliminating crossover distortion. Crossover distortion without this load would be more severe than that expected with the normal op amp. Since the single supply design took notice of this normal load connection to ground, a class AB output stage was not included. Where ground referenced feedback resistors are used as in *Figure 5*, the required load to the negative supply depends upon the peak negative output signal level desired without exhibiting crossover distortion. $R_L$ to the negative rail should be chosen small enough that the voltage divider formed by $R_F$ and $R_L$ will permit $V_o$ to swing negative to the desired point according to the equation

$$R_L = R_F \frac{V_S^- - V_o}{V_o}$$

$R_L$ could also be returned to the positive supply with the advantage that $V_o$ max would never exceed ($V_S^+$ − 1.5V). Then with ±15V supplies $R_{L\ MIN}$ would be 0.12 $R_F$. The disadvantage would be that the LM358 can source twice as much current as it can sink, therefore $R_L$ to negative supply can be one-half the value of $R_L$ to positive supply.

The need for single or split supply is based on system requirements which may be other than op amp oriented. However if the only need for balanced supplies is to simplify the biasing of op amps, there are many systems which can find a cost effective benefit in operating LM358's from single supplies rather than standard op amps from balanced supplies. Of the usual op amp circuits, Table II shows those few which have limited function with single supply operation. Most are based on the premise that to operate from a single supply, a reference $V_Q$ at about one-half the supply be available for bias or (zero) signal reference. The basic circuits are those listed in AN-20.

**TABLE II. Conventional Op Amp Circuits Suitable for Single Supply Operation**

| APPLICATION | LIMITATIONS |
|---|---|
| AC Coupled amp‡ | $V_Q$* |
| Inverting amp | $V_Q$ |
| Non-inverting amp | OK* |
| Unity gain buffer | OK |
| Summing amp | $V_Q$ |
| Difference amp | $V_Q$ |
| Differentiator | $V_Q$ |
| Integrator | $V_Q$ |
| LP Filter | $V_Q$ |
| I-V Connector | $V_Q$ |
| PE Cell Amp | OK |
| I Source | $I_{O\ MIN} = \frac{1.5}{R1}$ |
| I sink | OK |
| Volt Ref | OK |
| FW Rectifier | $V_Q$ or modified circuit |
| Sine wave osc | $V_Q$ |
| Triangle generator | $V_Q$ |
| Threshold detector | OK |
| Tracking, regulator PS | Not practical |
| Programmable PS | OK |
| Peak Detector | OK to $V_{IN} = 0$ |

‡See AN20 for conventional circuits
*$V_Q$ denotes need for a reference voltage, usually at about $\frac{V_S}{2}$
OK means no reference voltage required

Jim Sherwin
JANUARY 1975

# LM377, LM378, AND LM379 DUAL TWO, FOUR, AND SIX WATT POWER AMPLIFIERS

## INTRODUCTION

The LM377, LM378 and LM379 are two-channel power amplifiers capable of delivering 2, 4, and 6 watts respectively into 8 or 16Ω loads. They feature on-chip frequency compensation, output current limiting, thermal shut-down protection, fast turn-on and turn-off without "pops" or pulses of active gain, an output which is self-entering at $V_{CC}/2$, and a 5 to 20 MHz gain-bandwidth product. Applications include stereo or multi-channel audio power output for phono, tape or radio use over a supply range of 10 to 35V, as well as servo amplifier, power oscillator and various instrument system circuits. Normal supply is single-ended, however, split supplies may be used without difficulty or degradation in power supply rejection.

## CIRCUIT DESCRIPTION

The simplified schematic of *Figure 1* shows the important design features of the amplifier. The differential input stage made up of Q1—Q4 uses a double (split) collector PNP Darlington pair having several advantages. The high base-emitter breakdown of the lateral PNP transistor is about 60V which affords significant input over-voltage protection. The double collector allows operation at high emitter current to achieve good first stage $f_t$ and minimum phase shift while simultaneously operating at low transconductance to allow internal compensation with a physically small capacitor C1. (Unity gain bandwidth of an amplifier with pole-splitting compensation occurs where the first stage transconductance equals $\omega$ C1.)

Further decrease of transconductance is provided by degeneration caused by resistors at Q2 and Q3 emitters which also allow better large signal slew rate. The second collector provides bias current to the input emitter follower for increased frequency response and slew rate. Full differential input stage gain is provided by the "turnaround" differential to single-ended current source loads Q5 and Q6. The input common-mode voltage does not extend below about 0.5V above ground as might otherwise be expected from initial examination of the input circuit. This is because Q7 is actually preceeded by an emitter follower transistor not shown in the simplified circuit.

The second stage Q7 operates common-emitter with a current source load for high gain. Pole splitting compensation is provided by C1 to achieve unity gain bandwidth of about 10 MHz. Internal compensation is sufficient with closed-loop gain down to about $A_V$ = 25.

The output stage is a complementary common-collector class AB composite. The upper, or current sourcing section, is a Darlington emitter follower Q12 and Q13. The lower, or current sinking, section is a composite PNP made up of Q14, Q15, and Q9. Normally, this type of PNP composite has low $f_t$ and excessive delay caused by the lateral PNP transistor Q9. The usual result is poor unity gain bandwidth and probable oscillation on the negative half of the output waveform. The traditional fix has been to add an external series

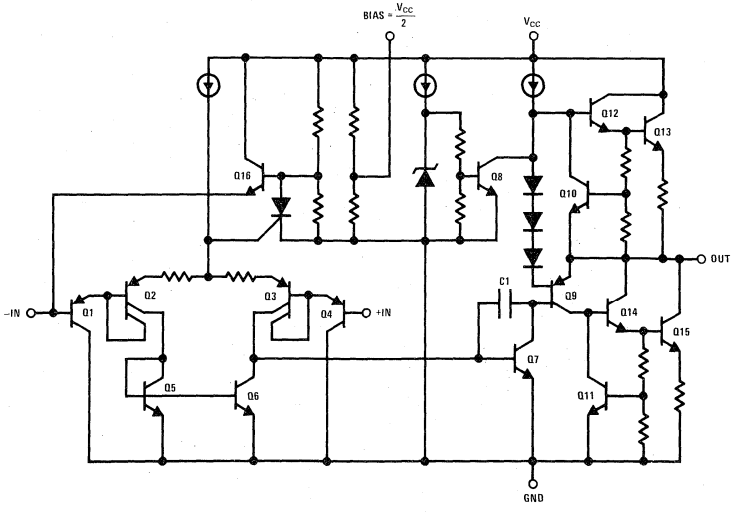



**FIGURE 1. Simplified Schematic Diagram**

RC network from output to ground to reduce loop gain of the composite PNP and so prevent the oscillation. In the LM377 series amplifiers, Q9 is made a field-aided lateral PNP to overcome these performance limitations and so reduce external parts count. There is no need for the external RC network, no oscillation is present on the negative half cycle, and bandwidth is better with this output stage. Q10 and Q11 provide output current limiting at about 1.3A, and there is internal thermal limiting protection at 150°C junction temperature. The output may be ac shorted without problem; and, although not guaranteed performance, dc shorts to ground are acceptable. A dc short to supply is destructive due to the thermal protection circuit which pulls the output to ground.

To achieve a stable dc operating point, it is desirable to close the feedback loop with unity dc gain. To achieve this simultaneously with a high ac gain normally requires a fairly large bypass capacitor, C1, in *Figure 2*.

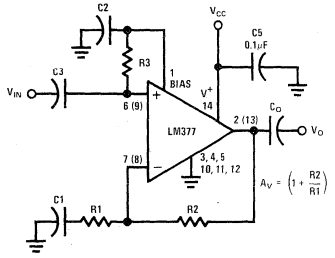



**FIGURE 2. Non-Inverting Amplifier Connection**

Establishing the initial charge on this capacitor results in a turn-on delay. An additional capacitor, C2, is normally required to supply a ripple-free reference to set the dc operating point. To achieve good supply rejection $X_{C2}$ is normally made much smaller than a series resistor from the bias divider circuit ($R_S$ in *Figure 3*). Where a supply rejection of 40 dB is required with 40 dB closed-loop gain, 80 dB ripple attenuation is required of $R_S$ C2. The turn-on time can be calculated as follows:

$$PSRR = \frac{R_S - jX_{C2}}{X_{C2}} \approx \frac{R_S}{X_{C2}} = \omega RC = \omega T$$

$$T = \frac{PSRR}{\omega} = \frac{80\ dB}{2\pi\ 120\ Hz} = \frac{10^4}{754} = 13.3\ sec$$

$$t_{ON} \approx \frac{T}{3} = 4.5 \text{ seconds to small signal operation}$$

$$t_{ON} \approx 3T = 40 \text{ seconds to full output voltage swing}$$

The 3T delay might normally be considered excessive! The LM377 series amplifiers incorporate active turn-on circuitry to eliminate the long turn-on time. This circuitry appeared in *Figure 1* as Q16 and an accompanying SCR; it is repeated and elaborated in *Figure 3*. In operation, the turn-on circuitry charges the external capacitors, bringing output and input levels to $V_{CC}/2$, and then disconnects itself leaving only the $V_{CC}/2$ divider $R_B/R_B$ in the circuit.

The turn-on circuit operation is as follows. When power is applied, approximately $V_{CC}/2$ appears at the base of Q16, rapidly charging C1 and C2 via a low emitter-follower output impedance and series resistors of 3k and 1k. This causes the emitters of the differential input pair to rise to $V_{CC}/2$, bringing the differential amp Q3 and Q4 into balance. This, in turn, drives Q3 into conduction. Transistors Q2 and Q3 form an SCR latch which then triggers and clamps the base of Q16 to

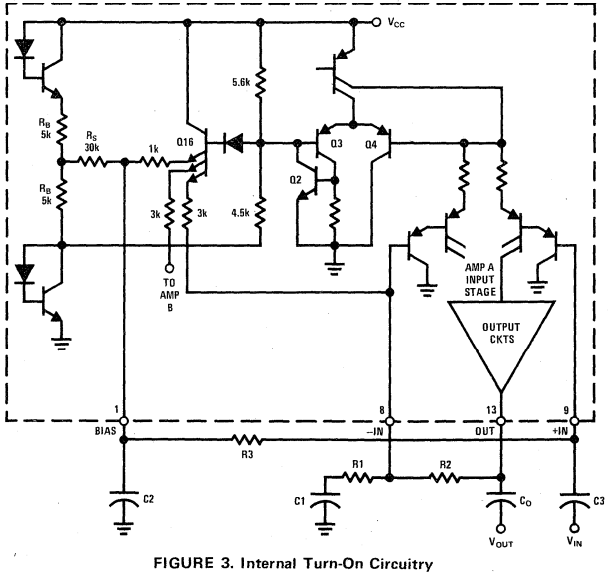



**FIGURE 3. Internal Turn-On Circuitry**

ground, thus disabling the charging circuit. Once the capacitors are charged, the internal voltage divider $R_B/R_B$ maintains the operating point at $V_{CC}/2$. Using C2 = 250μF, the $t_{ON}$ = 3T ≈ 0.3 seconds and PSRR ≈ 75 dB at 120 Hz due to the 30k resistor $R_S$. Using C2 = 1000μF, PSRR would be 86 dB. The internal turn-on circuit prevents the usual "pop" from the speaker at turn-on. The turn-off period is also pop-free as there is no series of pulses of active gain often seen in other similar amplifiers.

Note that the base of Q4 is tied to the emitters of only one of the two input circuits. Should only one amplifier be in use, it is important that it be that with input at pins 8 and 9.

## EXTERNAL BIASING CONNECTION

The internal biasing is complete for the inverting gain connection of *Figure 4* except for the external C2 which provides power supply rejection. The bias terminal 1 may be connected directly to C2 and the non-inverting input terminals 6 and 9. Normal gain-set feedback connections to the inverting inputs plus input and output coupling capacitors complete the circuitry. The output will Q up to $V_{CC}/2$ in a fraction of one second.

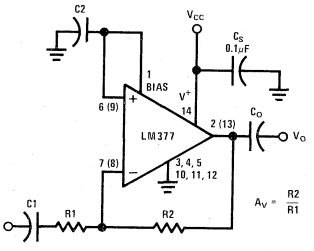


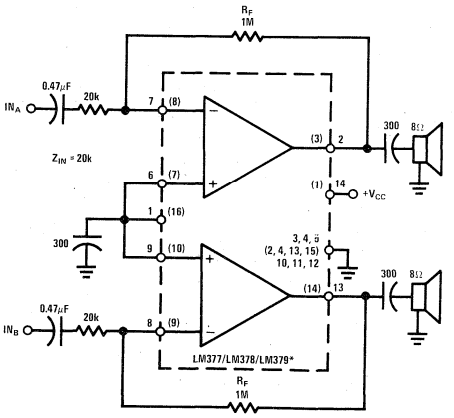

**FIGURE 4. Inverting Amplifier Connection**

The non-inverting circuit of *Figure 2* is only slightly more complex, requiring the input return resistor R3 from input to the bias terminal and additional input capacitor C3. C1 must remain in the circuit at the same or larger value than in *Figure 4*.

## AUDIO AMPLIFIER APPLICATIONS

### 2/4/6 Watt Stereo Amplifier

The obvious and primary intended application is as an audio frequency power amplifier for stereo or quad-raphonic music systems. The amplifier may be operated in either the non-inverting or the inverting modes of *Figures 2 and 4*. The inverting circuit has the lowest parts count so is most economical when driven by relatively low-impedance circuitry. *Figure 5* shows the total parts count for such a stereo amplifier. The feedback resistor value of 1 meg in *Figure 5* is about the largest practical value due to an input bias current max of approximately 1/2μA (100 nA typ). This will cause a −0.1 to 0.5V shift in dc output level, thus limiting peak negative signal




*(LM379 pin nos. in parenthesis)

| | LM377 | LM377/LM378 | LM379 |
|---|---|---|---|
| $P_O$ = | 2W/CH | 3W/CH | 4W/CH |
| $e_i$ = | 80 mV max | 98 mV max | 113 mV max |
| $A_V$ = | 50 | 50 | 50 |
| $V_{CC}$ = | 18V | 24V | 28V |

**FIGURE 5. Inverting Stereo Amplifier**

swing. This output voltage shift can be corrected by the addition of series resistors (equal to the $R_F$ in value) in the + input lines. However, when this is done, a potential exists for high frequency instability due to capacitive coupling of the output signal to the + input. Bypass capacitors could be added at + inputs to prevent such instability, but this increases the parts count equal to that of the non-inverting circuit of *Figure 6* which has a superior input impedance. For applications utilizing high impedance tone and volume controls, the non-inverting connection will most surely be used.

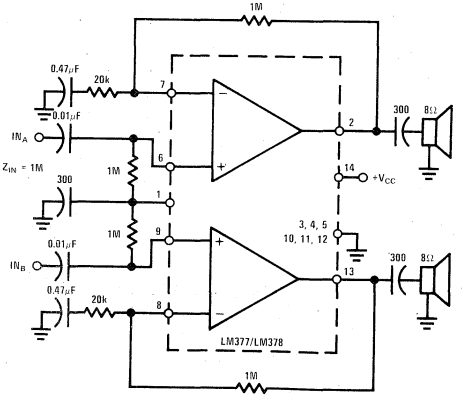
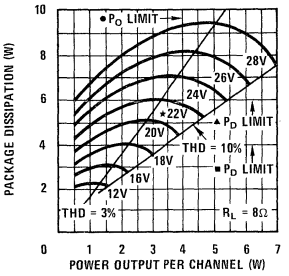


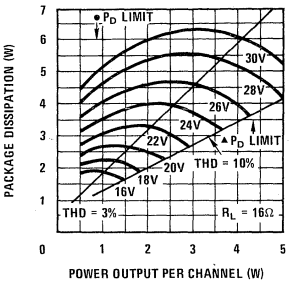

**FIGURE 6. Non-Inverting Stereo Amplifier**

The prime limitations on output power of the LM377 and LM378 will be the type of heat sink employed, supply voltage, and load resistance. Reference to the data sheet curves will indicate the most efficient supply voltages to use for specific power output levels with 8 or 16Ω loads. The pertinent curves are reproduced in *Figures 7 through 10.* For other conditions $P_D = V_{CC}^2/20\ R_L$. At high power out, efficiency exceeds 50%




- Approx. $P_D$ limit acc't. 0.7A rms internal current limit at oper. die temp.
- ▲ $P_D$ limit for LM377/LM378 on PC board w/Staver V7-1 heat sink.
- ■ $P_D$ limit for LM377/LM378 on PC board (2.5 sq. in. Cu)
- ★ Safe limit for LM377.

**FIGURE 7. Device Dissipation for 8Ω Load**




- $P_D$ limit LM377/LM378 on PC board w/Staver V7-1.
- ▲ $P_D$ limit LM377/LM378 on PC board.

**FIGURE 8. Device Dissipation for 16Ω Load**

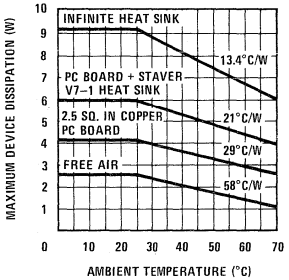



**FIGURE 9. LM377/LM378 Power Derating**

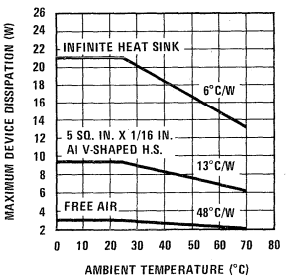



**FIGURE 10. LM379 Power Derating**

and dissipation drops below output power. A dual 2W amplifier must then dissipate about 4.0W with an 18V supply or 4.9W with a 20V supply when $R_L$ = 8Ω. Normally, one would choose the 18V supply for lower dissipation; however, the 20V supply allows reduced distortion levels or considerably higher powers. A dual 4W amplifier will dissipate about 8W with a 26V supply. This is above the dissipation limit for an LM378 with normal heat sink. Accordingly, a fairly efficient heat sink must be employed in order to allow full 8W continuous output from the LM378 *(Figure 9).* The recommended heat sinks are listed in Table I with measured power output levels at $V_S$ = 18 to 29V for LM377 and LM378 (observe voltage limits on LM377) with 8 or 16Ω load.

## POWER OUTPUT PER CHANNEL (BOTH CHANNELS DRIVEN) BEFORE CLIPPING

Power dissipation vs power output/channel (both channels driven) is indicated in *Figures 7 and 8* for load resistances of 8 and 16Ω.

Limiting points to keep in mind, noted on *Figures 7 and 8,* are 4W package dissipation limit for LM377/LM378 when soldered to PC board with 2.5 sq. in. copper, 6W limit when a Staver V7-1 heat sink is added, and internal current limit at about 1.5A peak at 25°C die temperature reducing to about 1A peak at operating die temperature. This results in an approximate $P_O$ = 4W/channel limit for $R_L$ = 8Ω. The onset of clipping occurs just to left of the THD = 3% line in *Figures 7 and 8.*

The overall result is that the LM377 and LM378 with practical heat sinks, are limited to operation below package dissipation of 6W and below $P_O$ = 4W/channel when $R_L$ = 8Ω. Thus maximum $P_O$ = 3W/channel before clipping or 4W/channel at about 6% THD with either device at $V_{CC}$ = 22V. With a 16Ω load the LM378 can deliver 4W/channel with 3–4% THD when $V_{CC}$ = 29–30V. The LM379 is limited to $P_O$ = 4–5W/channel before clipping at $V_{CC}$ = 26–28V, $R_L$ = 8Ω, or 4W/channel at $V_{CC}$ = 30V, $R_L$ = 16Ω. $P_O$ = 6W occurs at 8–10% THD with $V_{CC}$ = 28–30V and $R_L$ = 8Ω.

**TABLE I. Continuous Power Out (Both Channels)**

| HEAT SINK | LM377 $R_L$ = 8Ω | | | LM378 $R_L$ = 16Ω | | |
|---|---|---|---|---|---|---|
| | $V_S$ = 18V | $V_S$ = 20V | $V_S$ = 22V | $V_S$ = 24V | $V_S$ = 26V | $V_S$ = 29V |
| PC Board, 40°C/W | 2.2W | 0.8W | 0.3W | 2.2W | 1W | 0.3W |
| PC Board and Staver V7-1, 12°C/W | 2.2W | 2.7W | 3.1W | 2.2W | 2.5W | 3.3W |

Note that the $P_O$ = 6W rating on LM379 is at 10% THD where peak current is similar to that at $P_O$ = 4W, $V_{CC}$ = 26V, $R_L$ = 8Ω.

What really exists then are power out before clipping of 2W/channel at $V_{CC}$ = 18V with PC board mounting, 3W/channel at $V_{CC}$ = 22V with maximum practical heat sinking on either LM377 or LM378, and 4W/channel at $V_{CC} \geq$ 26V for LM379.

Device dissipation vs ambient temperature with several heat sink types is indicated in *Figures 9 and 10* for convenience of matching heat sink capacity to the circuit needs. In those cases where heat sink capacity is inadequate for device dissipation requirements, the internal thermal limit circuitry will automatically limit device dissipation on signal peaks. The result is similar to peak clipping in its effect and causes severe distortion. The device can provide momentary peak power output in excess of the maximum heat sink limited steady-state levels for a second or so depending upon the margin between maximum steady-state level and the actual average power level prior to the peak demand. Once in thermal limiting, clipping occurs on each positive and/or negative half cycle of a steady waveform.

In the majority of audio amplifier applications, the heat sinking can be considerably smaller due to the approximately 30 dB ratio between rms and peak power levels in music and speech. If we assume willingness to accept clipping at peak levels 20 dB above average level, then average power levels will be 0.2–0.3W/channel in LM377 and LM378. Heat sink requirements are thus significantly reduced as these peak levels occur less than 10% of time periods of several seconds duration. Thus the circuit does not go into thermal overload even though the heat sink is designed for 3W dissipation (LM377 operating at 0.3W/channel, $V_{CC}$ = 18V).

## STABILIZATION

The LM377 series amplifiers are internally stabilized so external compensation capacitors are not required. The high Gain x BW provides a bandwidth greater than 50 kHz as seen in *Figure 11.* These amplifiers are,

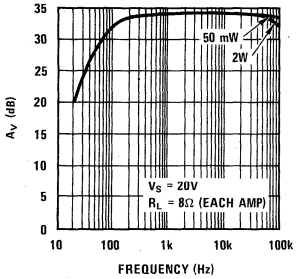



**FIGURE 11. Frequency Response of the Stereo Amp of Figure 5**

however, not intended for closed loop gain below 25. The typical Bode plot of *Figure 12* shows a phase margin of 70° for gain of 5.6 (15 dB) which is stable. At unity gain the phase margin is less than 30° or marginally stable. This margin may vary considerably from device to device due to variation in Gain x BW.

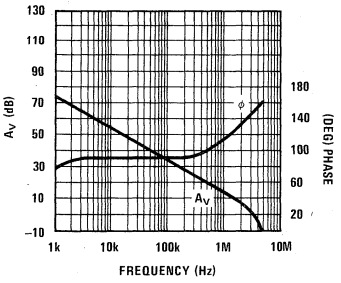



**FIGURE 12. Open Loop Bode Plot (Approximately Worst Case)**

As with any amplifier of high Gain x BW, careful circuit layout is important to insure unconditional stability. Specifically, coupling to the non-inverting inputs from output and feedback elements should be minimized. The supply should also be bypassed with an 0.05–0.1μF ceramic or 0.47μF mylar capacitor within 2 inches of the IC terminals. One layout which accomplishes this is illustrated in *Figure 13.* The signal circuits are symmetrically arranged on either side of the IC package.

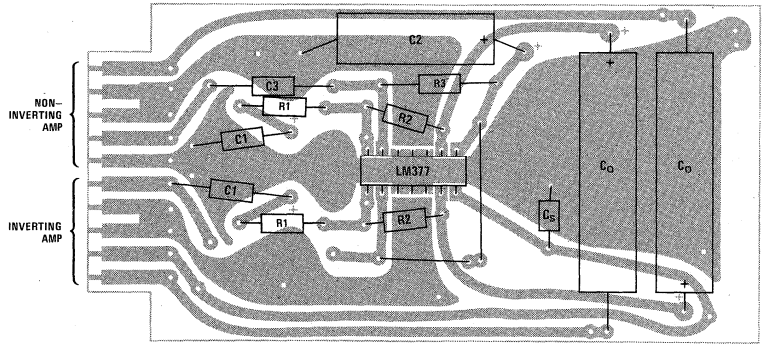



**FIGURE 13. Parts Layout for LM377/LM378 Dual Amplifier**

Operation may be either inverting or non-inverting, therefore, one side is shown connected each way. Normally both sides would be connected in the same sense. The PC board art-work is shown in *Figure 14.* The edge connector could, of course, be omitted and wire connections made to appropriate contacts at either end. This layout is satisfactory for gain as low as 10. Below $A_V$ = 10, instability may occur.

Ground and power connections must be adequate to handle the 1 to 2A peak supply and load currents. Ground loops can be especially troublesome because of these high currents. The load return line should be connected directly to the ground pins of the package on one side and/or the input and feedback ground lines should be connected directly to the ground pins (possibly on the other side of the package). Note that the layout in *Figure 14* has a connection at center of the card edge connector for signal ground and two separate, flanking, terminals for the load and power grounds. The signal ground should not be connected so as to intercept any output signal voltage drop due to resistance between IC ground and load ground.

### 10–12 Watt Channel Boosted Amplifier

Where more power output is desired, the simple booster circuit of *Figure 15* allows power output of 10W/channel

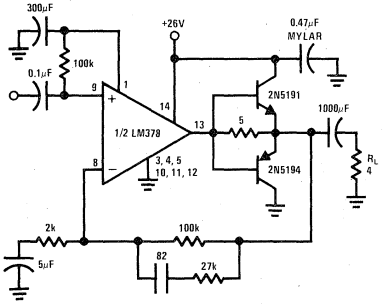



**FIGURE 15. 10 Watt Power Amplifier**

when driven from the LM378. The circuit is exceptionally simple, and the output exhibits lower levels of crossover distortion than does the LM378 alone. This is due to the inclusion of the booster transistors within the feedback loop. At signal levels below 20 mW, the LM378 supplies the load directly through the 5Ω resistor to about 100 mA peak current. Above this level, the booster transistors are biased ON by the load current through the same 5Ω resistor.

The response of the 10W boosted amplifier is indicated in *Figure 16* for power levels below clipping. Distortion

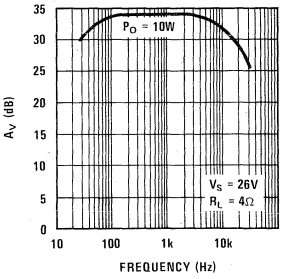



**FIGURE 16. 10 Watt Bosted Amplifier, Frequency Response**

is below 2% from about 50 Hz to 30 Hz. Fifteen watts rms power is available at 10% distortion; however, this represents extreme clipping. Although the LM378 delivers little power, its heat sink must be adequate for about 3W package dissipation. The output transistors must also have an adequate heat sink.

The circuit of *Figure 17* achieves about 12W/channel output prior to clipping. Power output is increased because there is no power loss due to effective series resistance and capacitive reactance of the output coupling capacitor required in the single supply circuit. At power up to 10W/channel, the output is extremely clean, containing less than 0.2% THD midband at 10W. The bandwidth is also improved due to absence of the output coupling capacitor. The frequency response and distortion are plotted in *Figures 18 and 19* for low and high power levels. Note that the input coupling capacitor is still required, even though the input may be ground

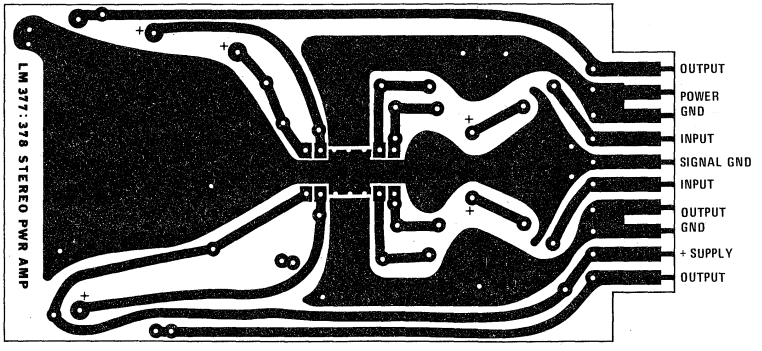



**FIGURE 14. PC Board for LM377/LM378 Dual Amplifier**

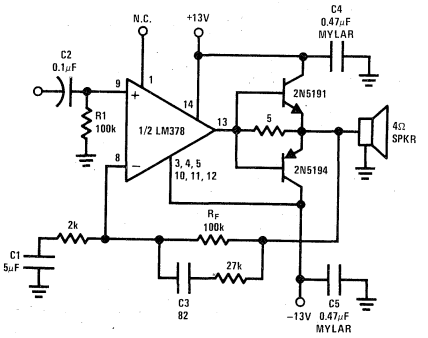



**FIGURE 17. 12 Watt Low-Distortion Power Amplifier**

referenced, in order to isolate and balance the dc input offset due to input bias current. The feedback coupling capacitor, C1, maintains dc loop gain at unity to insure zero dc output voltage and zero dc load current. Capacitors C1 and C2 both contribute to decreasing gain at low frequencies. Either or both may be increased for better low frequency bandwidth. C3 and the 27k resistor provide increased high frequency feedback for improved high frequency distortion characteristics. C4 and C5 are low inductance mylar capacitors connected within 2 inches of the IC terminals to ensure high frequency stability. R1 and $R_f$ are made equal to maintain $V_{OUT\ DC}$ = 0. The output should be within 10 to 20 mV of zero volts dc. The internal bias is unused; pin 1

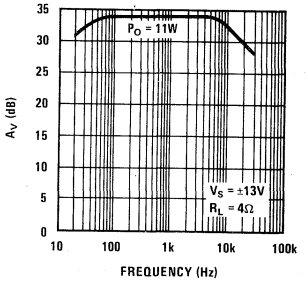



**FIGURE 18. Response for Amplifier of Figure 17**

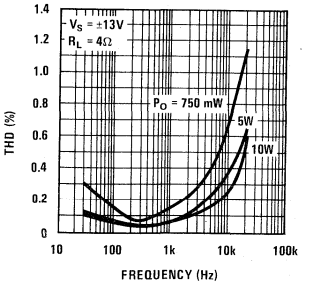



**FIGURE 19. Distortion for Amplifier of Figure 17**

should be open circuit. When experimenting with this circuit, use the amplifier connected to terminals 8, 9 and 13. If using only the amplifier on terminals 6, 7 and 2, connect terminals 8 and 9 to ground (split supply) to cause the internal bias circuits to disconnect.

## Bridge Amplifier

The LM377 series amplifiers are equally useful in the bridge configuration to drive floating loads, which may be loudspeakers, servo motors or whatever. Double the power output can be obtained in this connection, and output coupling capacitors are not required. Load impedance may be either 8 or 16Ω in the bridge circuit of *Figure 20*. Response of this circuit is 20 Hz

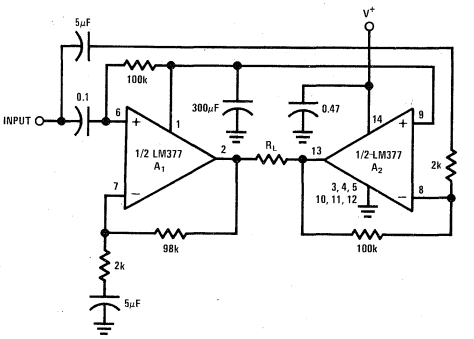



**FIGURE 20. 4-Watt Bridge Amplifier**

to 160 kHz as shown in *Figure 21* and distortion is 0.1% midband at 4W rising to 0.5% at 10 kHz and 50 mW output *Figure 22*. The higher distortion at low power is due to a small amount of crossover notch distortion which becomes more apparent at low powers and high frequencies. The circuit of *Figure 23* is similar except for higher input impedance. In *Figure 23*, the signal drive for the inverting amplifier is derived from the feedback voltage of the non-inverting amplifier. Resistors R1 and R3 are the input and feedback resistors for $A_2$, whereas R1 and R2 are the feedback network for $A_1$. So far as $A_1$ is concerned, R2 sees a virtual ground at the (−) input to $A_2$; therefore, the gain of $A_1$ is (1 + R2/R1). So far as $A_2$ is concerned, its input signal is the voltage appearing at the (−) input to $A_1$. This equals that at the (+) input to $A_1$. The driving point impedance at the (−) input to $A_1$ is very low even though R2 is 100k. $A_1$ can be considered a unity gain amplifier with internal R = R2 = 100k and $R_L$ = R1 = 2k. Then the effective output resistance of the unity gain amplifier is:

$$R_{OUT} = \frac{R_{INTERNAL}}{A_{OL}/A_\beta} = \frac{100k}{600/1} = 167\Omega$$

Layout is critical if output oscillation is to be avoided. Even with careful layout, capacitors C1 and C2 may be required to prevent oscillation. With the values shown, the amplifier will drive a 16Ω load to 4W with less than 0.2% distortion midband, rising to 1% at 20 kHz *(Figure 24)*. Frequency response is 27 Hz to 60 kHz as shown in *Figure 25*. The low frequency roll off is due to the double poles C3 R3 and C4 R1.

## Power Oscillator

One half of an LM377 may be connected as an oscillator to deliver up to 2W to a load. *Figure 26* shows a Wein bridge type of oscillator with FET amplitude stabilization in the negative feedback path. The circuit employs

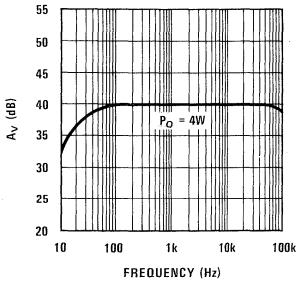



FIGURE 21. Frequency Response, Bridge Amp of Figure 20

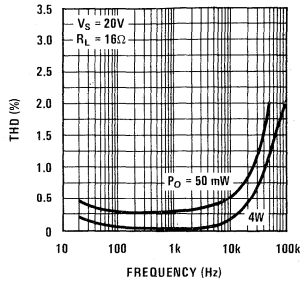



FIGURE 22. Distortion for Bridge Amp of Figure 20

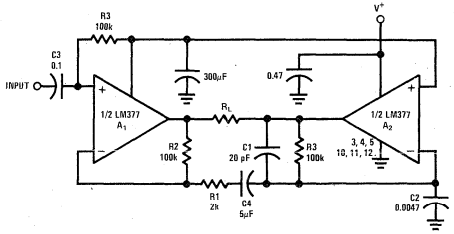



FIGURE 23. 4-Watt Bridge Amplifier with High Input Impedance

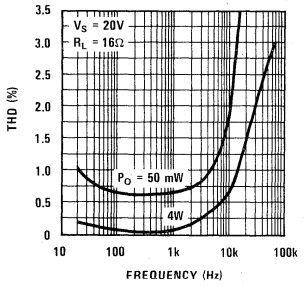



FIGURE 24. Distortion for Bridge Amp of Figure 23

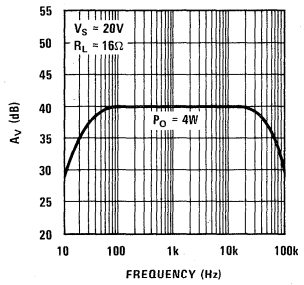



FIGURE 25. Frequency Response, Bridge Amp of Figure 23

internal biasing and operates from a single supply. C3 and C6 allow unity gain dc feedback and isolate the bias from ground. Total harmonic distortion is under 1% to 10 kHz, and could possibly be improved with careful adjustment of R5. The FET acts as the variable element in the feedback attenuator R4 to R6. Minimum negative feedback gain is set by the resistors R4 to R6, while the FET shunts R6 to increase gain in the absence of adequate output signal. The peak detector D2 and C8 senses output level to apply control bias to the FET. Zener diode D1 sets the output level although adjustment could be made if R9 were a potentiometer with R8 connected to the slider. Maximum output level with the values shown is 5.3V rms at 60 Hz. C7 and the attenuator R7 and R8 couple 1/2 the signal of the FET drain to the gate for improved FET linearity and low distortion. The amplitude control loop could be replaced by an incandescant lamp in non-critical circuits *(Figure 27)* although dc offset will suffer by a factor of about 3 (dc gain of the oscillator). R10 matches R3 for improved dc stability; and the network R11, C9 increases high frequency gain for improved stability. Without this RC, oscillation may occur on the negative half cycle of output waveform. A low inductance capacitor, C5, located directly at the supply leads on the package is important to maintain stability and prevent high frequency oscillation on negative half cycle of the output waveform. C5 may be 0.1μF ceramic, or 0.47μF mylar. Layout is important; especially take care to avoid ground loops as discussed in the section on amplifiers. If high frequency instability still occurs, add the R12, C10 network to the output.

*Figure 27* shows the use of the LM377 to drive a small 60 Hz two phase servo motor up to 3W per phase. Applications such as a constant (or selectable) speed phonograph turntable drive are adequately met by this circuit. A split supply is used to simplify the circuit, reduce parts count, and eliminate several large bypass capacitors. An incandescent lamp is used in a simple amplitude stabilization loop. Input dc is minimized by balancing dc resistance at + and − amplifier inputs (R1 = R3 and R6 = R8). High frequency stability is assured by increasing closed-loop gain from approximately 3 at 60 Hz to about 30 above 40 kHz with the network consisting of R3, R4 and C3. The interstage

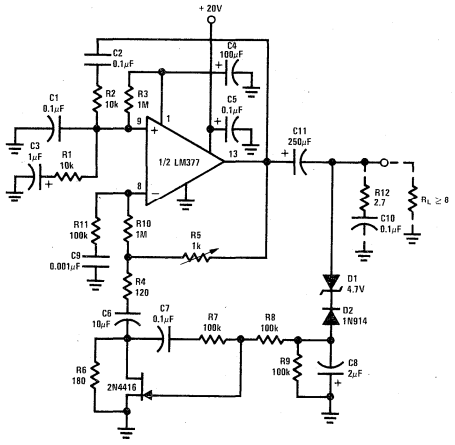



FIGURE 26. Wien Bridge Power Oscillator

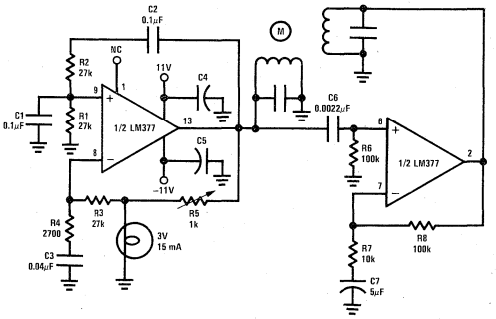
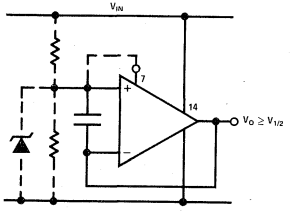
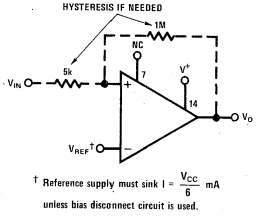


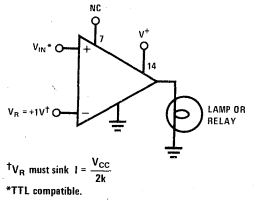

FIGURE 27. Two-Phase Motor Drive




Supply Regulator




Power Comparator




Lamp or Relay Driver

FIGURE 28. Miscellaneous Applications

coupling C6 R6 network shifts phase by 85° at 60 Hz to provide the necessary two phase motor drive signal. The gain of the phase shift network is purposely low so that the buffer amplifier will operate at a gain of 10 for adequate high frequency stability. As in other circuits, the importance of supply bypassing, careful layout, and prevention of output ground loops is to be stressed. The motor windings are tuned to 60 Hz with shunt capacitors. This circuit will drive 8Ω loads to 3W each.

## MISCELLANEOUS APPLICATIONS

A number of non-audio applications come to mind, such as a dual power supply regulator, power comparator, and relay or lamp driver as shown in *Figure 28.* The degree of practicality of any of these will be limited by the special characteristics of the LM377/LM378/LM379 chip. Limitations are a higher than usual input-offset voltage and temperature drift (not troublesome in the intended capacitor coupled applications). As the devices are not unity-gain stable, a shunt capacitor across the inputs is needed in low gain applications such as the supply regulator. The output saturation voltage is 2 to 3V, thus internal power dissipation is non-negligible in relay or lamp driver applications.

As a lamp driver, the LM377 is limited to those applications where its dissipation is outweighed by the advantage of the internal current limiting. The real advantage of this current limiting is that the lamp driver cannot be destroyed by a shorted lamp *if* the lamp common terminal is ground (the LM377 will not survive an output short to supply).

In any of these applications, recall that the internal turn-on circuit will supply current out the (−) input until inputs are raised to $V_{CC}/2$.

## COMPLETE SYSTEMS

The LM377 to LM379 dual power amplifiers are useful in table or console radios, phonographs, tape players, intercoms, or any low to medium power music systems. Several examples of complete audio systems are described. One is a 2-channel audio system for radio, phono, and tape playback. The other is rear channel amplifier pair for extracting "ambience" information from stereo signals and amplifying for 4-channel sound.

*Figures 29 to 30* describe the complete electronic section of a 2-channel sound system with inputs for AM

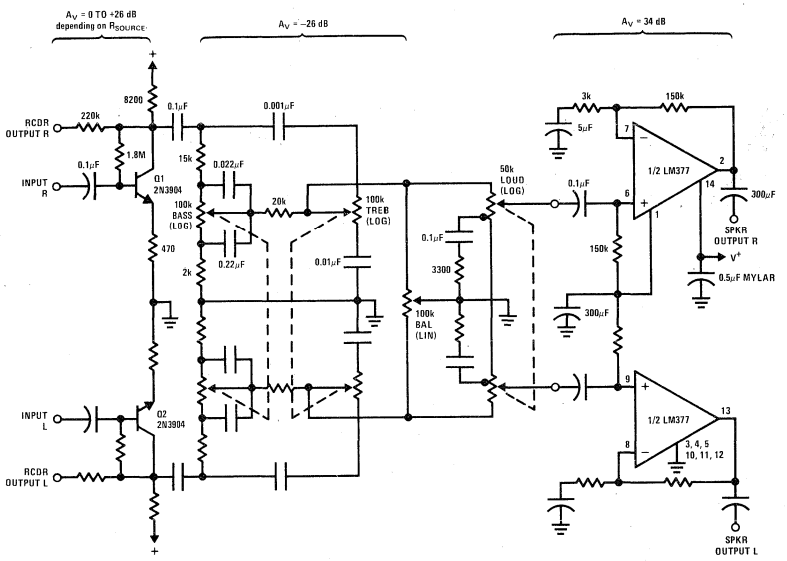



**FIGURE 29. Two-Channel Power Amplifier and Control Circuits**

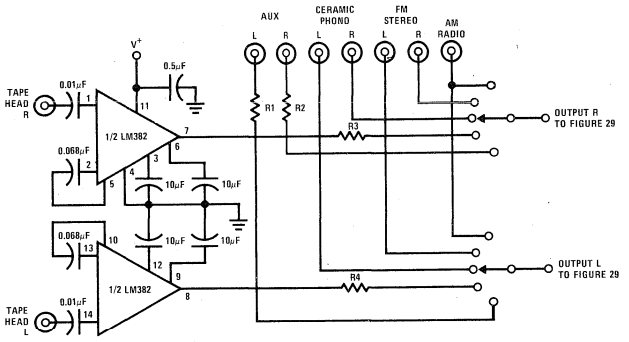



**FIGURE 30. Two-Channel Tape-Playback Amplifier and Signal Switching**

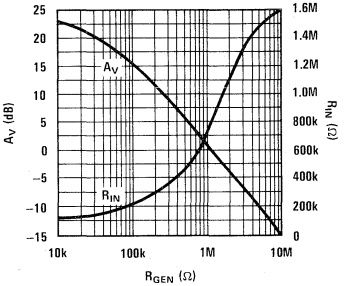



**FIGURE 31. $A_V$ and $R_{IN}$ for Input Stage of Figure 28.**

radio, stereo FM radio, phono, and tape playback. *Figure 29* combines the power amplifier pair with loudness, balance, and tone controls. The tone controls allow boost or cut of bass and/or treble. Transistors Q1 and Q2 act as input line amplifiers with the triple function of (1) presenting a high input impedance to the inputs, especially ceramic phono; (2) providing an amplified output signal to a tape recorder; and (3) providing gain to make up for the loss in the tone controls. Feedback tone controls of the Baxandall type employing transistor gain could be used; but then, with the same transistor count, the first two listed functions of Q1 Q2 would be lost. It is believed that this circuit represents the lowest parts count for the complete system. *Figure 30* is the additional circuitry for input switching and tape playback amplifiers. The LM382 with capacitors as shown provides for NAB tape playback compensation. For further information on the LM382 or the similar LM381 and LM387, refer to the data sheets.

*Figure 31* shows the relationship between signal source impedance and gain or input impedance for the amplifier stage Q1 Q2. Stage gain may be set at a desired value by choice of either the source impedance or insertion of resistors in series with the inputs (as R1 to R4 in *Figure 30*). Gain is variable from −15 to +24 dB by choice of series R from 0 to 10 meg. Gain required for $e_{IN}$ = 100 to 200 mV (approximate value of recovered audio from FM stereo or AM radio) is about 18 to 21 dB overall for 2W into an 8Ω speaker at 1 kHz or 21 to 24 dB for 4W.

The rear channel "ambience" circuit of *Figures 32 and 33* can be added to an existing stereo system to extract a difference signal (R − L or L − R) which, when combined with some direct signal (R or L), adds some fullness, or "concert hall realism" to reproduction of recorded music. Very little power is required at the rear channels, hence an LM377 will suffice for most "ambience" applications. The inputs are merely connected to the existing speaker output terminals of a stereo set, and two more speakers are connected to the ambience circuit outputs. Note that the rear speakers should be connected in opposite phase to those of the front speakers, as indicated by the +/− signs on the diagram of *Figure 32*.

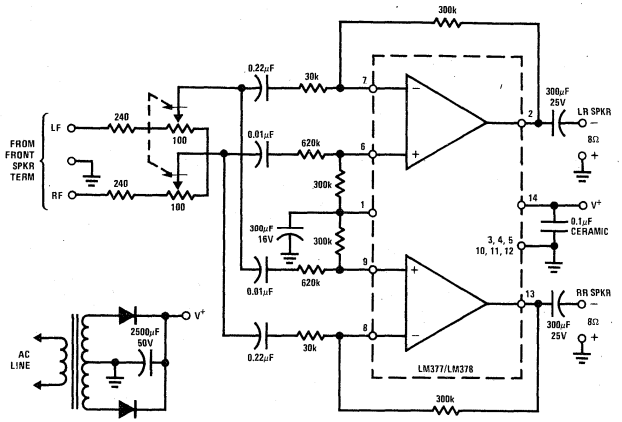



FIGURE 32. Rear Speaker Ambience (4-Channel) Amplifier

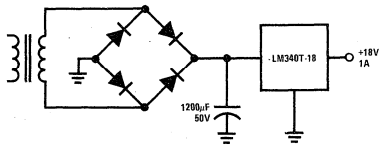



FIGURE 33. Alternate Power Supply for Ambience Circuit

## APPENDIX: INTERPRETATION OF $P_O$ vs $P_D$ CURVES

The angled straight lines on the curves of *Figures A-1* and *A-2* indicate the loci of operating points where clipping occurs. When THD = 3%, the output waveform has noticeable clipping. The THD = 10% line is an operating area of severe clipping. Clipping begins just to the left of the THD = 3% line so this discussion deals only with operation up to, but not quite at, the 3% line.

The three circles on *Figure A-1* are the data sheet spec limits for LM377/LM378/LM379; that is, 2, 4 and 6W/channel with 20, 24 and 28V supplies respectively. Observe that the 2W point is well to the left of the THD = 3% line, or well under clipping. The 4 and 6W points march progressively further toward the THD = 10% line, or deeper into clipping. Also note the dissipation limits in *Figure A-3* for LM377/LM378 on PC board and on PC board with addition of Staver V7-1 heat sink are 4.1 and 6W respectively. These represent the limits for commonly available heat sinks for the DIP package. No doubt a special heat sink fabricated "just-so" could extend the 6W limit to 6 1/2 or 7W, but we'll stop at 6W. Data have been added to *Figure A-4* showing LM379

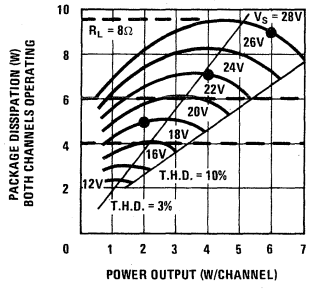



FIGURE A-1. Power Dissipation vs Power Output

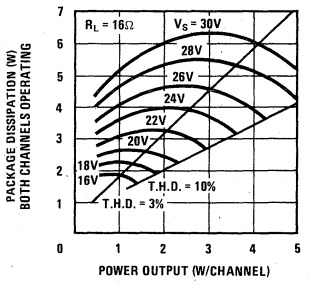



FIGURE A-2. Power Dissipation vs Power Output

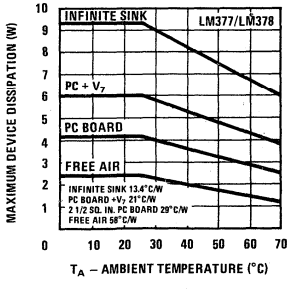



FIGURE A-3. Maximum Dissipation vs Ambient Temperature

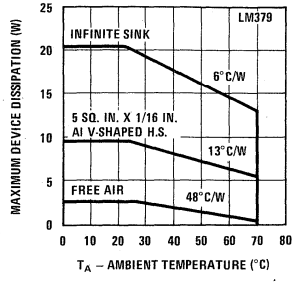



FIGURE A-4. Maximum Dissipation vs Ambient Temperature

dissipation with a simple small heat sink. This heat sink is 5 square inches of 1/16" aluminum in a modified V shape which is clamped to the sink side of the LM379.

These practical limits are transferred to *Figure A-1* as horizontal dashed lines across the $P_O$ vs $P_D$ curves at 4.1, 6 and 9.6W. We see that the reference points, 2W at 20V and 4W at 24V, are above the practical $P_D$ limits for PC board alone and for PC board with Staver V7-1 heat sink. The third point, 6W at 28V is OK so far. What this means is that, in bench testing, the LM377 must have better than PC mounting to meet data sheet specified operation; and the LM378 will likely not meet data sheet specified operation with any practical heat sink. The LM377 will meet specs with the PC board plus Staver heat sink. The LM378 will meet specs with a 7W heat sink, but not with normally available heat sinks. The LM379 will meet specs with the 5 square inch sink described above. What may be most important, however, is performance short of clipping. For that reason, the remainder of this section will deal only with rms power at levels below clipping.

Returning to *Figure A-1*, it appears that the LM377 or LM378 with only PC board heat sinking will be able to deliver 2.2W/channel into 8Ω with an 18V supply. But, if the supply is raised to 20V, the $P_D$ limit is exceeded at 1W. With PC board plus a Staver heat sink, the LM377/LM378 will deliver 3.2W/channel with 22V supply, yet raising the supply to 24V limits us to $P_O$ = 1.9W/channel.

So why use a LM378 if the supply limit is 22V? The reason is that few supplies are regulated in the consumer world. This means that if the supply is 22V under full load, the no-signal supply may rise 10% or more; and the variations in line voltage may add another 10% for a total supply maximum of at least 26.5V. Therefore the LM377 is only recommended for full-load operating supplies of less than 20V. But remember, it can deliver over 2W/channel with an 18V supply on a PC board, or 2 1/2W/channel with 20V supply and Staver heat sink. The LM378 will provide 3.2W/channel with 22V supply and PC board plus Staver heat sinking. With poorly regulated supplies over 20V or with 16Ω load, the LM378 is the obvious choice as higher supply voltages are required to obtain high powers with 16Ω loads. Although no greater power is available than with 8Ω loads.

There is no reasonable $P_D$ limit on the LM379 as we can dissipate nearly 20W with adequate practical heat sinking and 9.6W with minimal sink. Then $V_{CC}$ is the limit, say 30V. That would put us off the graph on *Figure A-1* at about 5.5W/channel or at 3W/channel with 16Ω load. Even at 8Ω and 30V, package dissipation is only 11W, or 9.6W with 28V. The kicker is in the data sheet electrical characteristics under current limit; 1.5A typ when $T_{TAB}$ = 25°C. The tab is above 25°C when package dissipation is 9–11W. Still, this is a realistic test for high speed machine testing. In actual use, the current limit moves down to maybe 1.25A or even less. What does this mean? Consider an 8Ω load in power equation, and that 1–1.25A pk is 0.7–0.88A rms.

$$P = I^2 R$$

$$= (0.7)^2\ 8 = (0.5)\ 8 \quad \text{or} = (0.88)^2\ 8 = (0.77)\ 8$$

$$= 4W \qquad\qquad = 6.2W$$

Now we have the actual limits at $P_{O(MAX)}$ = 4–6.2W at 8Ω or 8W at 16Ω. Trouble is we are limited to 5W at 28V, 8Ω or 5.5W at 30V, 8Ω and 4W at 16Ω by a 30V operating limit. Current limits could run higher than data sheet typicals; many do, in fact. Then we can get more than 4W/channel as a limit. Since this is a typical spec, there is no guarantee either way.

Note with interest that an LM377 with Staver V7-1 heat sink will deliver 3.2W/channel with 22V supply (but hold it close to 22V or use a LM378) and the LM379 will deliver 5W/channel with a 28V supply. The LM379 is the practical choice because it is easier and probably cheaper to heat sink, and there is more $P_D$ headroom to allow for variations in supply voltage (very important). Also, the better the heat sink on the LM379, the lower the tab temperature, and the higher the operating current limit.

Beyond the limits discussed, the temperature or current limits operate, the peaks are clipped, the waveform remains at peak value for a longer portion of the input cycle, the rms $P_O$ increases, $P_D$ decreases, and rms power approaches peak power.

Here is a summary of the performance the customer may encounter.

**TABLE A-1. Max $P_O$ Before Clipping (8Ω Load)**

| Heat Sink = | PC BOARD (29°C/W) | | | PC BOARD + V7-1 (21°C/W) | | | | 13°C/W SINK | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ = | 16 | 18 | 19 | 18 | 20 | 22 | 23 | 26 | 28 | 30 |
| $P_O$/CH = | 1.5 | 2.2 | 1.4 | 2.2 | 2.5 | 3.2 | 1.9 | 4.3 | 5.0 | 5.5 |
| | ├──── LM377 ────┤ | | | | | | | | | |
| | ├──── LM378 ──── | | | | | ──┤ | | | | |
| | ├──── LM379 ──── | | | | | | | | | ──┤ |

Sam Ochi
John Flink
APRIL 1976

# LM143 MONOLITHIC HIGH VOLTAGE OPERATIONAL AMPLIFIER APPLICATIONS

## INTRODUCTION

The LM143 is a general purpose, high voltage operational amplifier featuring ±40V maximum supply voltage operation, output swing to ±37V, ±38V input common-mode range, input overvoltage protection up to ±40V and slew rate greater than 2V/$\mu$s*. Offset null capability plus low input bias and offset currents (8 nA and 1 nA respectively) minimize errors in both high and low source impedance applications. Due to isothermal symmetry of the chip layout, gain is constant for loads $\geq$ 2 k$\Omega$ at output levels to ±37V. Because of these features, the LM143 offers advantages not found in other general purpose op amps. The LM143 may, in fact, be used as an improved performance, plug-in replacement for the LM741 in most applications.

This paper describes the operation of the LM143 and presents applications which take advantage of its unique, high voltage capabilities. Obviously, other applications exist where the low input current and high slew rate of the LM143 are useful. (See AN-29 on the LM108). Application tips are included in the appendix to guide the user toward reliable, trouble-free operation.

## CIRCUIT DESCRIPTION

A simplified schematic of the LM143, shown in *Figure 1*, illustrates the basic circuit operation. The super-$\beta$ input transistors[1], Q1 and Q2, are used as emitter followers to achieve low input bias currents. Although these devices exhibit $\beta$ = 2000–5000, they inherently have a low collector-base breakdown voltage of about 4V. Therefore, active voltage clamps Q3 and Q4 protect Q1 and Q2 under all input conditions including common-mode and differential overvoltage. Other NPNs in the circuit are representative of those found in standard IC op amps, ($\beta \approx 200$, $LV_{CEO}$ = 50–70V).

The input stage differential amplifier Q7 and Q8 with large base width exhibit $LV_{CEO}$ = 90V to 110V and high $BV_{EBO}$ so readily withstand input overvoltages. The total input stage collector current ($I_1$ = 80$\mu$A) is made higher than in most op amps to improve slew rate. Emitter degeneration resistors, R10 and R11, reduce transconductance[2] to limit small signal bandwidth at 1 MHz for a phase margin of 75°. Q16 and Q17 function as active collector loads for Q7 and Q8 and provide differential to single-ended current conversion with full differential gain.

One of the highest breakdown voltages available in standard planar NPN processing is the collector-base, $BV_{CBO}$ which is typically 90V to 120V. To make use of this high voltage capability in the active region, the second stage consists of a cascode (common emitter–common base pair) connection of Q21 and Q23. The internal voltage bias $V_{B1}$, shunts avalanche-induced leakage current away from the base of Q21, avoiding $\beta$ multiplication as found in the $LV_{CEO}$ mode. Q23 and emitter follower Q22 are internally biased at a low voltage so the $BV_{CEO}$ mode is impossible. Frequency compensation is achieved with an internal, high voltage capacitor, $C_C$.

*An externally compensated version of the LM143, the LM144, offers even higher slew rate in most applications. The LM144 is pin-for-pin compatible with the LM101A.

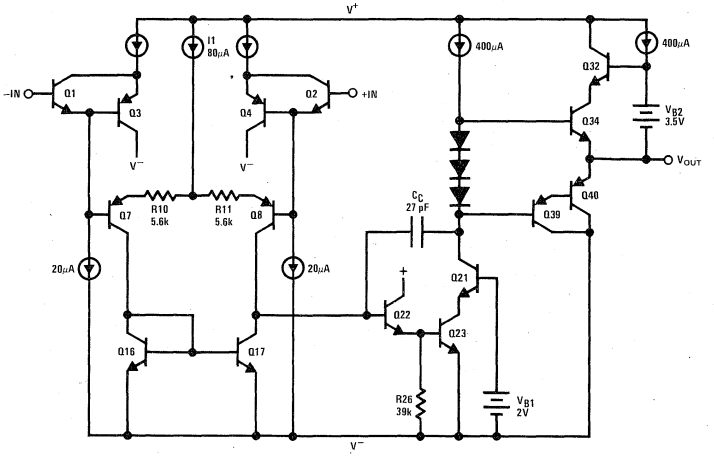



**FIGURE 1. LM143 Simplified Schematic**

The second stage drives a complementary class AB output stage. A cascode connection of Q32 and Q34 is again employed for high breakdown voltage. The associated voltage bias, $V_{B2}$, is internally derived. A Darlington PNP pair, Q39 and Q40 with $BV_{CEO}$ = 100V, provides the active pull-down.

## HIGH VOLTAGE APPLICATIONS

The following applications make use of the high voltage capabilities of the LM143. As with most general purpose op amps, the power supplies should be adequately bypassed to ground with 0.1μF capacitors.

### 130 Vp-p Drive to a Floating Load

A circuit diagram using two LM143's to drive up to 130V peak-to-peak is given in *Figure 2*.

A non-inverting voltage amplifier, with a gain of $A_V$ = 1 + (R2/R1), is followed by a unity gain inverter. The load is applied across the outputs of A1 and A2. Therefore, $V_{OUT}$ = V1 − V2 = V1 − (−V1) = 2V1. If V1 = 65 Vp-p, then 2V1 = 130 Vp-p.

The above circuit was breadboarded and the results are as follows:

i) Maximum output voltage: 138 Vp-p unclipped into 10 kΩ load

ii) Slew rate: 6V/μs

### ±34V Common-Mode Range Instrumentation Amplifier

An instrumentation amplifier with ±34V common-mode range, high input impedance and a gain of X1000 is shown in *Figure 3*.

For a differential input signal, $V_{IN}$, A1 and A2 act as non-inverting amplifiers of gain $A_{V1}$ = 1 + (2R1/R2), where R1 = R3. However, the gain is unity for common-mode signals since voltages V1 and V2 are in phase, and no current flow is developed through R1, R2 and R3. The second stage is simply an op amp connected as a simple differential amplifier of gain, $A_{V2}$ = (R5/R4), where R5 = R7 and R4 = R6. The total gain of the instrumentation amplifier is

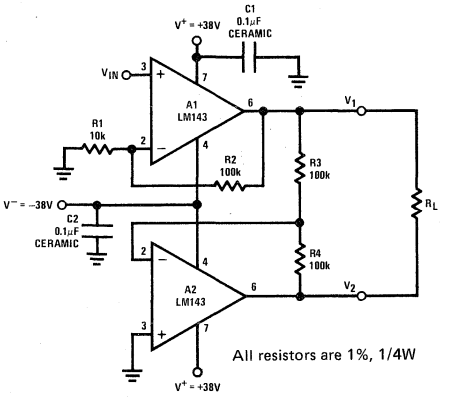
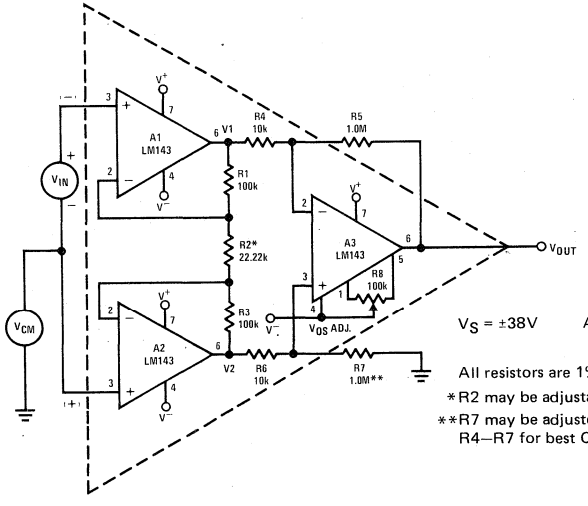



**FIGURE 2. 130V Drive Across a Floating Load**

$$A_V = \left(1 + \frac{2R1}{R2}\right)\left(\frac{R5}{R4}\right) = \left(1 + \frac{2X100k}{22.22k}\right)\left(\frac{1.0M}{10k}\right)$$

$$= 1000$$

R7 may be adjusted to take up the resistance tolerances of R4, R5 and R6 for best common-mode rejection (CMR). Also, R2 may be made adjustable to vary the gain of the instrumentation amplifier without degrading the CMR.




$V_S$ = ±38V $\quad A_V = \left(1 + \frac{2R1}{R2}\right)\frac{R5}{R4}$ Where: R4 = R6, R5 = R7

All resistors are 1%, 1/4W

*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4—R7 for best CMR.

**FIGURE 3. Wide Common-Mode Range Instrumentation Amplifier**

Laboratory evaluation of this circuit revealed noise and CMR data as follows:

i) Frequency response with 10k load and $A_V$ = 1000: −3.0 dB at 8.9 kHz

ii) CMR measurements (common-mode signal of ±34 Vp-p) in *Figure 4*

iii) Noise measurements in *Figure 5*

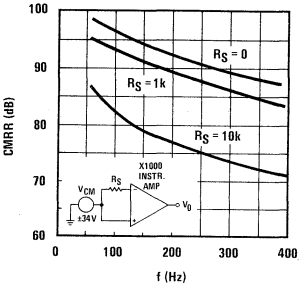



**FIGURE 4. Common-Mode Rejection Measurements**

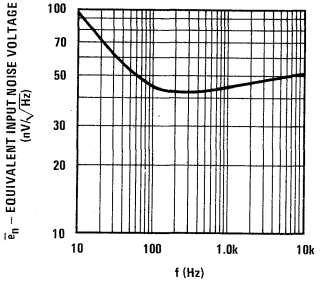
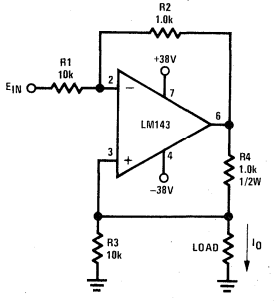



**FIGURE 5. Noise Measurements**

### High Compliance Current Source

A current source with a compliance of ±28V is shown in *Figure 6.*




All resistors 1% metal film, 1/4W unless otherwise specified.

**FIGURE 6. High-Compliance Current Source**

The non-inverting input of the op amp senses the current through R4 to establish an output current, $I_O$ proportional to the input voltage. The expression for $I_O$ is

$$I_O = -\frac{E_{IN}\,R2}{R1\,R4} = -\frac{0.1\text{ mA}}{V}\,E_{IN}.$$

R3 keeps the circuit stable under any value of load resistance. Measured circuit performance is as follows:

$I_{OMAX}$ = ±3.5 mA at $E_{IN}$ = ∓35V

$R_{OUT}$ = 2 MΩ at $I_{OUT}$ = ±2.0 mA

### CURRENT BOOSTED APPLICATIONS

Because of the high voltage capability of the LM143, some thought must be given for the selection of the minimum load resistance. At an ambient temperature of 25°C, the LM143 can dissipate 680 mW. Worst case dissipation arises when the load resistance $R_L$ is connected to one supply and $V_O$ = 0. Then the amplifier sources $I_O = (38V/R_L)$ with 38V internal voltage drop. During this condition,

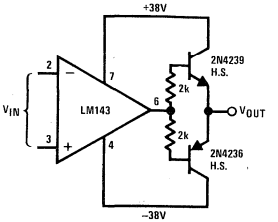
$$P_{MAX} = 680\text{ mW} = \frac{E_L{}^2}{R_L} = \frac{(38V)^2}{R_L}$$

$$\text{or } R_L = \frac{1444V^2}{680\text{ mW}} \approx 2.1\text{ k}\Omega$$

Hence, load resistances less than 2k will cause excessive power dissipation.

### Simple Power Boost Circuit

For loads less than 2 kΩ, a power boost circuit should be added. The simple booster shown in *Figure 7* has the advantage of minimal parts count, but crossover distortion is noticeable and there is no short circuit protection; hence, either the LM143 or the boost transistors may fail under short circuit conditions.



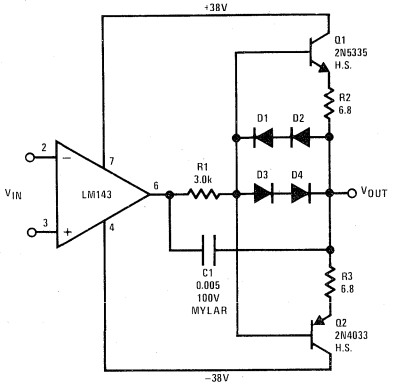

Heat sink is a Thermalloy No. 2230-5 or equivalent.
All resistors are 10%, 1W.

**FIGURE 7. Simple Power Boost Circuit**

### 100 mA Current Boost Circuit

With the addition of 4 diodes, a resistor and a capacitor, the booster circuit can be short circuit protected at 100 mA as shown in *Figure 8*.

R1 protects the LM143 by limiting the maximum drive current to (38V/3.0k) ≅ 12.5 mA, thereby keeping safely within the device dissipation limit of 680 mW. D1–D4 in conjunction with R2 and R3 protect the output transistors Q1 and Q2 by shunting the output drive current if the voltage drop across R2 or R3 exceeds 0.7V.




Heat sink is a Thermalloy No. 2230-5 or equivalent.
All diodes are 1N914.
All resistors are 1/2W, 10%.

**FIGURE 8. 100 mA Current Boost Circuit**

Breadboard Data:

i) Frequency Response: Limited by LM143 frequency response and slew rate.

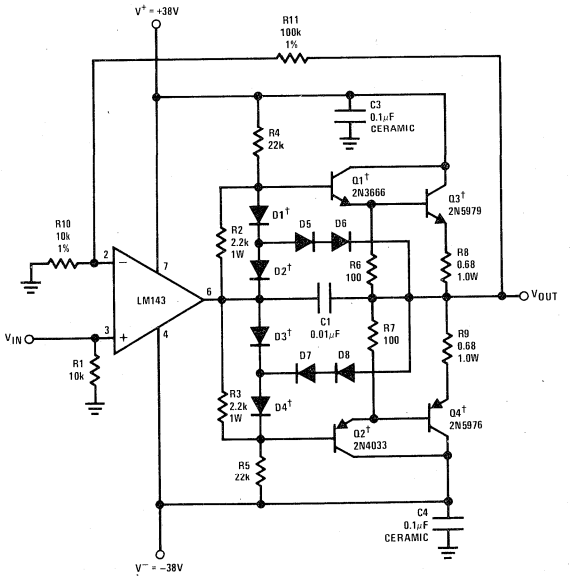
ii) Step response for unity gain, voltage follower configuration: Less than 10% overshoot for 1.0V step with 0.01μF capacitive load, 50% overshoot with 0.47μF capacitive load. The circuit is unconditionally stable for capacitive loads.

iii) Output Voltage: ±33 Vp-p into 400Ω load

### 1.0 Amp Class AB Current Booster

If crossover distortion is objectionable and currents of up to 1.0A are needed, the circuit in *Figure 9* should be used.

The output of the LM143 drives a class AB complementary output stage. The quiescent current for the output stage is set by the current flow through R4, R5 and diodes D1–D4. The diodes D1–D4 are on a common heat sink with the output transistors Q3 and Q4 so that the voltage drops across the diodes and base-




†Put on common heat sink, Thermalloy 6006B or equivalent.
All diodes are 1N3193.
All resistors are 10%, 1/4W except as noted.

**FIGURE 9. 1 Amp Class AB Current Booster with Short Circuit Protection**

emitter junctions of the output transistors will track with temperature, Normally, R4 and R5 supply the current drive for the output Darlingtons, Q1, Q3 and Q2, Q4, but if additional drive is needed, the LM143 supplies the remainder through R2 and R3. For short circuited load, the drive current is bypassed around the output transistors through D1, D5 and D6 during the positive half cycle and through D4, D7 and D8 during the negative half cycle. Drive current bypassing, or output current limiting, occurs whenever R8 or R9 sees more than one diode drop (≅0.7V). An expression for the maximum output current is

$$I_{MAX} \cong \frac{0.7V}{0.68\Omega}$$

$$I_{MAX} \cong 1.0A.$$

Capacitor C1 stabilizes the circuit under most feedback and load conditions and C3 and C4 bypass the power supply. Measured performance is as follows:

i) Maximum output voltage with $R_L = 40\Omega$: +29.6V, −28V with $V_S = \pm 38\ V_{DC}$.

ii) Harmonic distortion measurements of *Figure 10* were measured with a closed loop gain of 10.

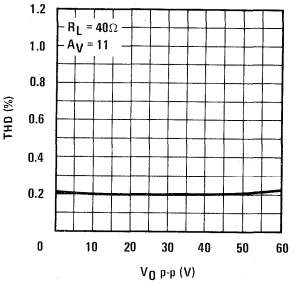
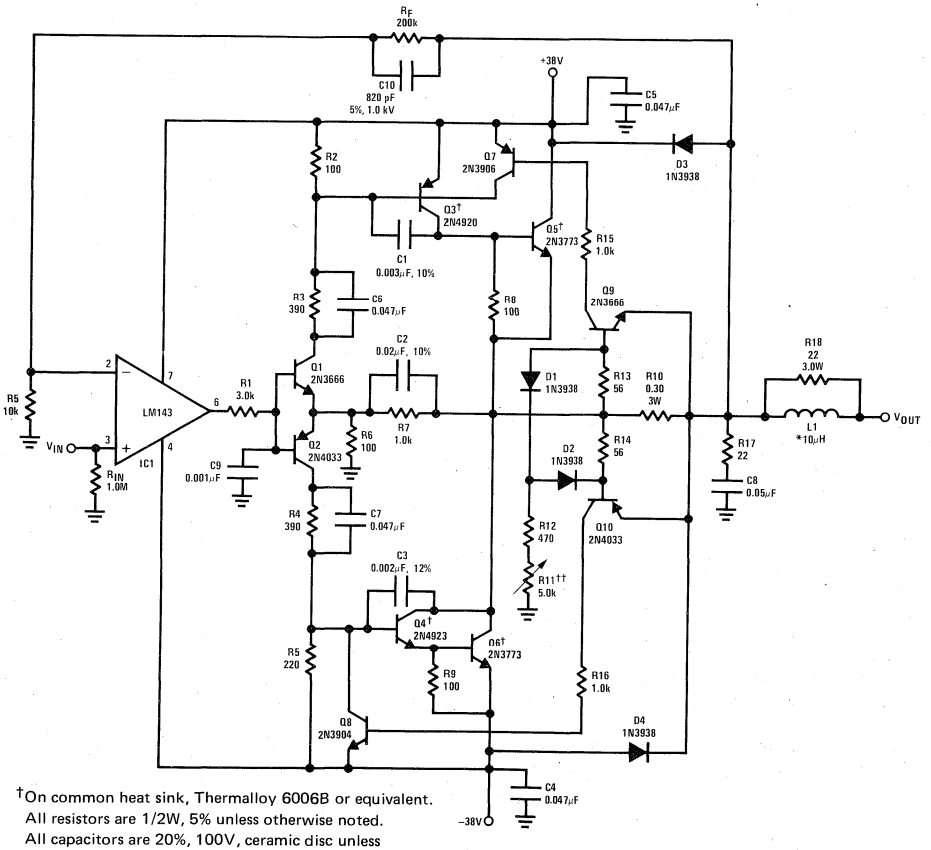



**FIGURE 10. Harmonic Distortion Measurements**

### Very High Current Booster with High Compliance

If very high peak drive current is required in addition to a capability for the output swing to within 4.0V of the supplies under full load, the circuit in *Figure 11* should be used.




†On common heat sink, Thermalloy 6006B or equivalent.
All resistors are 1/2W, 5% unless otherwise noted.
All capacitors are 20%, 100V, ceramic disc unless otherwise noted.
††Output current limit adjust.

**FIGURE 11. Very High Current Booster with High Compliance**

Excluding the LM143, the current booster has three stages. The first stage is made up of Q1 and Q2 which level shifts and boosts the current output of the LM143 to about 100 mA. Q3 and Q4 further boost the output of Q1 and Q2 to about 1.0A. Q5 and Q6 then have adequate drive to source and sink at least 10A. There is no quiescent current path when the output voltage is zero since Q1 and Q2 are biased off.

The short circuit protection circuit is made up of Q7 and Q9 on the positive side and Q8 and Q10 on the negative side. Q9 or Q10 turns on as soon as $V_{BE} \cong 0.7V$ appears across R10 when the output terminal is shorted to ground. Then Q7 or Q8 bypass the drive to the output devices, Q5 and Q6. Since R10 is 0.3Ω, current limiting under short circuited output occurs at 2.3A and is relatively independent of the current limit adjustment resistor, R11. An expression for the maximum output current, $I_{OUT\ MAX}$, with $V_{OUT}$ and R11 as variables is

$$|I_{OUTMAX}| \cong \frac{\frac{(|V_{OUT}| - V_{D1})R13}{R11 + R12 + R13} + V_{BE9}}{R10}$$

$$\cong \frac{\frac{(|V_{OUT}| - 0.7)\ 56\Omega}{R11 + 526\Omega} + 0.7V}{0.3\Omega}$$

The equation is valid for both output polarities. The plot in *Figure 12* superimposes the above equation on the maximum operating area curve for the 2N3773 and illustrates the safe area protection feature.

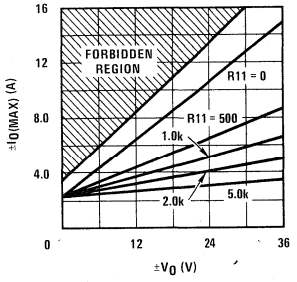



**FIGURE 12. Maximum Output Current as a Function of R11 and $V_{OUT}$**

The diodes, D1 and D2, are in the circuit to keep the base-emitter junctions of Q9 and Q10 from being reversed biased during the opposite polarity output voltage swings. C1, C2, C3, C6, C7 and C9 are judiciously inserted in the circuit to prevent oscillation. R17, R18, C8 and L1 are used in the circuit to maintain stability under all load conditions. Diodes D3 and D4 provide protection for inductive loads.

All measurements taken with a 4Ω load and ±38V supplies unless otherwise stated:

i) Maximum power out: 144 Wrms
ii) Frequency response:
   a) −3.0 dB at 10 kHz at full power
   b) −3.0 dB at 11.5 kHz at 10 Vp-p out
iii) Maximum output voltage: ±34V
iv) Maximum capacitive load: 10μF with 10% overshoot for a small signal step response
v) DC deadband: 20μV
vi) Quiescent current: 12.7 mA (positive supply), 2.1 mA (negative supply)
vii) Input impedance: 1 MΩ
viii) Voltage gain: 21

## HIGH POWER APPLICATIONS

### 90 Wrms Audio Power Amplifier

A circuit diagram of an audio power amplifier which is capable of 90 Wrms into a 4Ω speaker or 70 Wrms into an 8Ω speaker is given in *Figure 13*. The circuit features safe area, short circuit and overload protection, harmonic distortion less than 0.1% at 1.0 kHz, and an all NPN output stage.

The output of the LM143 drives a quasi-complementary output stage made up of Q1, Q2, Q3 and Q4. This quasi-complementary circuit, which makes possible an all NPN output, was chosen over the complementary output circuit due to the lack of low cost high voltage power PNP transistors.

Safe area current limiting occurs whenever the output current is

$$|I_{OUTMAX}| = \frac{\frac{(|V_{OUT}| - V_{D3})R11}{R11 + R13} + V_{BE5}}{R12}$$

where R11 = R15 = 330Ω,

R13 = R14 = 3.9k,
R12 = R16 = 0.25Ω and

$V_{BE5} \cong V_{BE6} \cong V_{D3} \cong V_{D4} \cong 0.7V$.

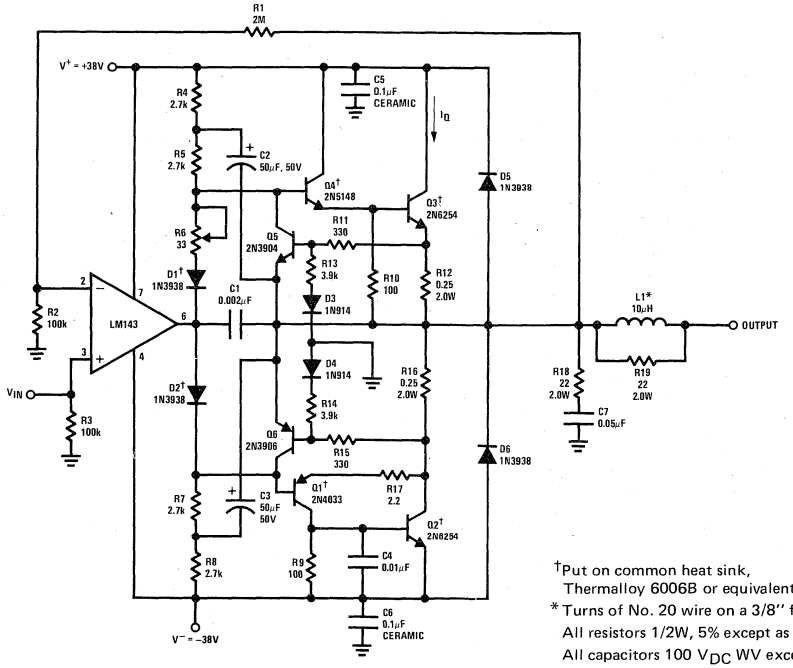
If the output is shorted, the above equation simplifies to

$$I_{OUT\ MAX} = \frac{V_{BE5}}{R12} \cong \frac{0.7V}{0.25\Omega} = 2.8A$$

If the output voltage is 30V,

$$I_{OUT\ MAX} = \frac{\frac{(30V - 0.7V)\ 330}{4.23k} + 0.7V}{0.25\Omega}$$

$$\cong \frac{2.3 + 0.7V}{0.25} = 12A$$




†Put on common heat sink,
Thermalloy 6006B or equivalent.
*Turns of No. 20 wire on a 3/8" form.
All resistors 1/2W, 5% except as noted.
All capacitors 100 $V_{DC}$ WV except as noted.

**FIGURE 13. 90W Audio Power Amplifier**

The maximum output current, $I_{O(MAX)}$, versus $V_O$ is plotted in *Figure 14*. D4 and D3 are in the circuit to keep Q5 off during the negative half of the output voltage cycle and Q6 off during the positive half cycle.

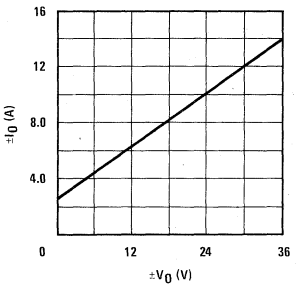



**FIGURE 14. Output Current Limiting as a Function of Output Voltage**

The output stage is biased into class AB operation by using the resistor string R4, R5, R7 and R8 to set the voltage drops across R6, D1 and D2, which then determine the quiescent current through the output transistors. These diodes are thermally coupled to the output devices to track their base-emitter junction voltages with temperature. Low distortion at low power levels is achieved by adjusting R6 to set the quiescent current through Q3 and Q2 to about 100 mA. *Figure 15* shows a plot of distortion at 50 mW versus quiescent current.

C2 and C3 are connected between the output and the R4, R5 and R7, R8 junctions to provide a "bootstrapped" drive potential for the output stage during output voltage swings near the power supply potentials. The absolute magnitudes of the voltages at these junctions exceed the power supply voltages during the high output swings so that adequate current drives to Q4 and Q1 are available. C1 and C4 are used for compensating the output stage. C5 and C6 are used for power supply bypassing. R18, C7, R19 and L1 are included in the circuit to keep the amplifier stable under all load conditions. D5 and D6 provide protection for inductive loads.

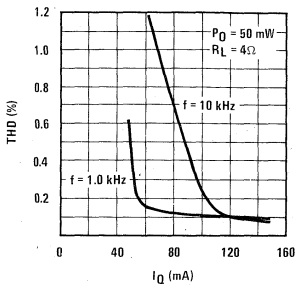



**FIGURE 15. Quiescent Current vs Distortion**

The input impedance of the audio amplifier is simply the value of R3. To keep the output offset voltages to a minimum, R3 ≅ R1 ||R2. The voltage gain is

$$A_V = 1 + \frac{R1}{R2} = 1 + \frac{2.0M}{100k} = 21$$

The following data was taken with $V_S = \pm 38V$:

i) Maximum power output before visible clipping:
   a) 90 Wrms at 1.0 kHz into 4Ω load
   b) 70 Wrms at 1.0 kHz into 8Ω load
ii) Distortion measurement: distortion versus frequency and power is plotted in *Figures 16 and 17.*
iii) Maximum capacitive load: 20μF
iv) Output noise, 10 Hz to 20 kHz: 100μVrms
v) Frequency response:
   a) Small signal (1.0 Vrms into 4.0Ω): −3.0 dB at 40 kHz
   b) Power (90W into 4Ω): −3.0 dB at 29 kHz
   c) Power (70W into 8Ω): −3.0 dB at 30 kHz

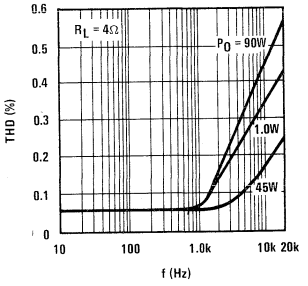



**FIGURE 16. Distortion vs Frequency, $R_L$ = 4Ω**

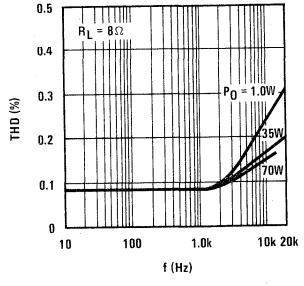



**FIGURE 17. Distortion vs Frequency, $R_L$ = 8Ω**

## POWER SUPPLY CIRCUITS

The ability of the LM143 to withstand up to 80V can be exploited fully in the design of regulated power supplies. The circuits to be described use a zener reference voltage, an IC voltage amplifier, and a discrete power transistor pass element. If care is taken to keep the voltage drop across the pass element within 40V, standard three terminal voltage regulators such as the LM340, LM120, etc. may be used as pass elements and significantly decrease parts count and circuit complexity. Circuits using this approach are given in the LM340 application note (see AN-103).

### A Tracking ±65V Supply with 500 mA Output

A tracking power supply circuit can be made by modifying the circuit for the 130 Vp-p driver circuit. The modified circuit is given in *Figure 18*.

A 2N4275 is used as a stable zener voltage reference of about 6.5V. Its output is amplified from one to about 10 times by the circuitry associated with IC1. The output of IC1 is applied through R10 to the Darlington connected transistors, Q2 and Q3. The feedback resistor, R5, one end of which is connected to the $V^+$ output node, is made variable so that the $V^+$ output voltage will vary from 6.5V to about +65V. The $V^+$ output is applied to a unity gain inverting power amplifier to generate the $V^-$ output voltage. The output circuit of the unity gain inverter uses a composite PNP, Q4 and Q5, to provide the current boost.

Since the input terminals of A2 are at ground potential, the positive supply lead cannot be grounded; instead, it is connected to the output of a 4.7V zener diode, D8, to keep within the input common-mode range.

C1, C3 and C4 are used for decreasing the power supply noise. C2 is used in bypassing most of the noise generated by the reference voltage and C5 and C6 are used to reduce the voltage output noise. Short circuit protection is provided by D1, D2, D3, R10 and R14 on the positive side and by D4, D5, R11 and R15 on the negative side. The short circuit protection circuit is the same as the one used in the 1.0A current booster circuit.

The short circuit current is given by

$$I_{MAX} \cong \frac{V_{BE}}{R14} \cong \frac{V_{BE}}{R15}$$

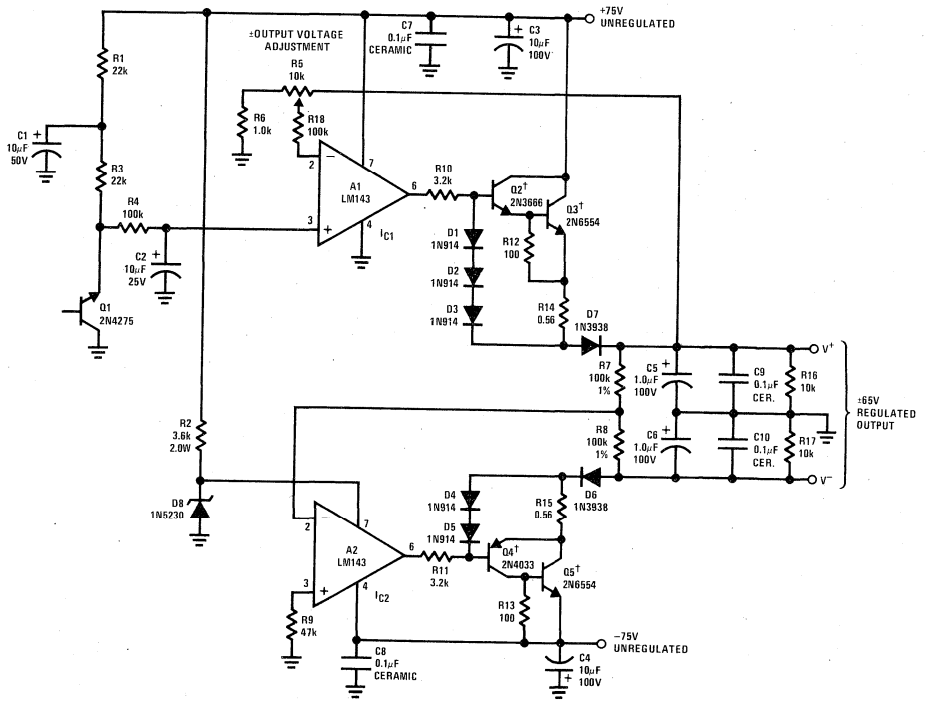
$$\cong \frac{0.7}{0.56} = 1.25A$$

where $V_{BE}$ = voltage drop across a diode.

### +65V, 1.0A Power Supply with Continuously Variable Output Current and Voltage

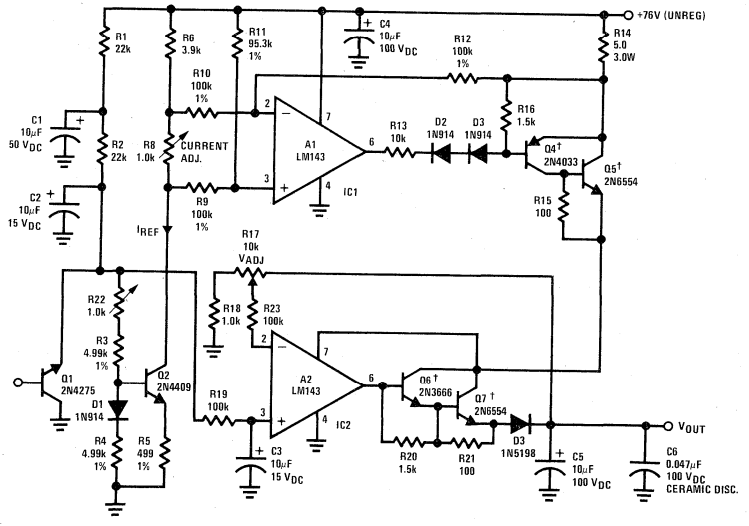
If a continuously variable output current as well as output voltage supply is needed, a power supply circuit given in *Figure 19* will do the job. It has an output range from 7.1V to 65V with an adjustable output current range of 0 to 1.0A.

Basically, the power supply circuit is a non-ideal voltage source in series with a non-ideal current source. A reference voltage of approximately 6.5V is obtained by zenering the base-emitter junction of the 2N4275. The positive temperature coefficient of the zenering voltage is compensated by the negative temperature coefficient of the forward biased base-collector junction. The output of the voltage reference goes to the variable gain power amplifier made up of IC2, Q6, Q7 and their associated components and to a reference current source made up of Q2, D1 and components around them. The variable gain power amplifier multiplies the reference voltage from one to ten times due to the variable feedback resistor, R17. Since the maximum current output of IC2 is at most 20 mA, the Darlington connected Q6 and Q7 are used to boost the available output current to 500 mA.




†Put on common heat sink, Thermalloy 6006B or equivalent.
All resistors are 1/2W, 5%, except as noted.

**FIGURE 18. Tracking 65V, 1A Power Supply with Short Circuit Protection**




†Put on common heat sink, Thermalloy 6006B or equivalent.
All resistors 1/2W, 10% unless otherwise noted.
All capacitors 20%.

**FIGURE 19. 1A, 65V Power Supply with Variable Current Limit**

**Breadboard Data for the Tracking 65V Power Supply**

$V_{IN}$ = ±75V, $I_{OUT}$ = ±500 mA, $T_j$ = 25°C, $T_A$ = 25°C, $V_{OUT}$ = ±40V, unless otherwise specified.

| PARAMETER | CONDITIONS | MEASURED DATA | |
|---|---|---|---|
| | | $+V_{OUT}$ | $-V_{OUT}$ |
| Load Regulation | $0 \leq I_{OUT} \leq 500mA$ | 0.5 mV | 1.0 mV |
| Line Regulation | $\lvert\pm50V\rvert \leq V_{IN} \leq \lvert\pm80V\rvert$ | | |
| | $I_{OUT}$ = ±100 mA | 175 mV | 176 mV |
| | $I_{OUT}$ = ±500 mA | 169 mV | 173 mV |
| Quiescent Current | $I_{OUT}$ = 0 | Pos. Supply | Neg. Supply |
| | | 28.22 mA | 6.55 mA |
| Output Noise Voltage* | 10 Hz ≤ f ≤ 100 kHz | 0.125 mV | 0.135 mV |
| Ripple Rejection | $I_{OUT}$ = ±20 mA, f = 120 Hz | −72.5 dB | −63.4 dB |
| Output Voltage Drift* | | 3.38 mV/°C | 3.43 mV/°C |

*The output noise and drift are due primarily to the zener reference.

**Measured Performance of the 1A, 65V Power Supply**

$V_{IN}$ = +76V, $I_{OUT}$ = 500 mA, $T_j$ = 25°C, $V_{OUT}$ = +40V unless otherwise specified

| PARAMETER | CONDITIONS | MEASURED DATA |
|---|---|---|
| Load Regulation | $0 \leq I_{OUT} \leq 500$ mA (Pulsed Load) | 5.0 mV |
| Line Regulation | $46V \leq V_{IN} \leq 76V$ | |
| | $I_{OUT}$ = 100 mA | 297 mV |
| | $I_{OUT}$ = 500 mA (dc Loads) | 286 mV |
| Maximum Output Voltage | dc Load | 68.6V |
| Quiescent Current | | 21.4 mA |
| Output Noise Voltage* | 10 Hz ≤ f ≤ 100 kHz | 0.280 mV |
| Ripple Rejection | $I_{OUT}$ = 20 mA, f = 120 Hz, $\Delta V_S$ = 3.0 Vp-p, $\Delta V_O$ = 6.0 mVp-p | 66.6 dB |
| Loads are Pulsed Loads | 200μs Pulse Every 200 ms | |

*The output noise is due primarily to zener reference.

The power current source is an op amp used as a differential amplifier which senses the voltage drop across R8 and maintains this same voltage across R14. Hence, the maximum output current is

$$I_{OUT} = \frac{R8}{R14} \times I_{REF} \leq \frac{1.0k}{5.0\Omega} \times 5.0\,mA = 1.0A.$$

Since the output load under most conditions will not demand what the power current source can deliver, Q4 and Q5 will remain in saturation during normal operation. When Q4 and Q5 are pulled out of saturation, the output load voltage will drop until the load current just equals what is available from the power current source. Because the positive supply terminal of IC2 is tied to the collectors of Q4 and Q5, IC2 will supply just enough current drive to Q6 and Q7 to keep itself on. Hence, a current limiting resistor is unnecessary for IC2. A 10k current limiting resistor, R13, is present since the total unregulated power supply voltage is available for IC1. R6 is used to stay within the input common-mode voltage range of IC1.

$I_{REF}$ is derived from the 6.5V reference source, Q1, by using Q2 in a current source configuration. R22 is made adjustable so that $I_{REF}$ can be set for 5.0 mA.

## CONCLUSION

The LM143 is a high performance operational amplifier suited for applications requiring supply voltages up to ±40V. The LM143 is especially useful in power supply circuits where the unregulated voltages are as high as ±40V and in amplifier circuits where output voltages greater than ±30V peak are needed. The LM143 is internally compensated and is pin-for-pin compatible with the LM741. Compared with the LM741, the LM143 exhibits an order of magnitude lower input bias currents, better than five times the slew rate and twice the output voltage swing.

## APPENDIX

Toward the goal of trouble-free applications, this appendix details some of the more subtle features of the LM143 and reviews application hints pertinent both to op amps in general and the LM143 in particular. The complete schematic of the LM143 is shown in *Figure 20.*

The circuit starts drawing supply current, at supply voltages of ±4V, when current is provided to a 7.5V zener diode D5 by the collector FET Q41. The gate-channel junction of Q41 exhibits 100V breakdown as source and drain are lightly doped NPN collector and substrate material. The collector current of Q18 biases current sources Q25 through Q30 and sets the supply current at nearly zero TC.

Q19 furnishes a bias voltage, 5V above the negative supply, for the collectors of Q15, Q20 and Q22. The low impedance 2V reference ($V_{B1}$ in *Figure 1*) for the base of Q21 appears at the emitter of Q20 and has the correct TC to insure that Q23 never saturates. Should this occur, the low resistance of Q23 would cause premature $LV_{CEO}$ breakdown of Q21.

The input transistors, Q1 and Q2, are biased by Q13 and Q14 which have a breakdown voltage essentially equal to $BV_{CBO}$ by virtue of the high emitter impedance, R18 and R19, relative to the low dynamic impedance of D4. In a similar way, Q18 and Q19 stand off essentially the full supply voltage. These devices have a high output impedance caused by series feedback and so hold the supply current nearly constant to prevent excessive power dissipation at high supply voltages.

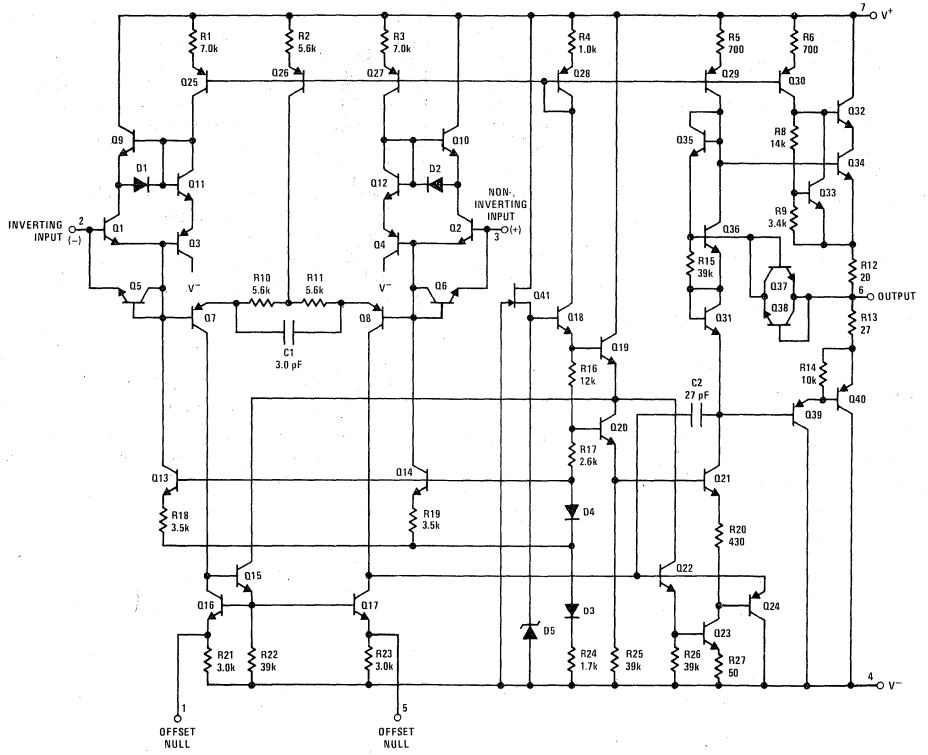



**FIGURE 20. Complete Schematic of the LM143**

While the simple voltage clamping scheme, Q3 and Q4 in *Figure 1*, is adequate, it is prone to oscillation when built with high $\beta$ PNPs. The more elaborate scheme of *Figure 20* prevents instability. This clamping method is similar to that used in the LM108, but allows large differential inputs to exist with complete input overvoltage protection. Q9 and Q10, which withstand the high input common-mode voltage, have a $BV_{CBO}$-type breakdown due to the low impedance diodes seen from the base leads and the high impedance of Q1 and Q2 (enhanced by 100% series feedback) in the emitter leads. Input overvoltage protection also holds up under high-level transient input voltages.

With a large negative-going step input, as could occur in the unity-gain voltage follower configuration, diode-connected Q6 turns "ON," protecting the emitter-base junction of Q2 from zener breakdown and subsequent long-term $\beta$ degradation. At the same time, stray capacitance at the collector of Q2 is discharged by D2 through Q4 and Q12. This holds Q10 in a true $BV_{CBO}$ mode (emitter open-circuited) and clamps the voltage across Q2 to 3 $V_{BE}$.

With a large positive-going step input, stray capacitance at the collectors of Q2 and Q12 is charged by the forward-biased collector junction of Q2. As before, with D2 conducting, Q10 is again in the $BV_{CBO}$ breakdown mode. Since the inverting input can be subject to the same transients, Q1 is afforded the same protection.

Distributed capacitance associated with R10 and R11, together with the collector-base capacitance of Q26, cause a high frequency transmission pole (the "tail" pole[2]) which can degrade phase margin. This is avoided by adding a small lead capacitor, C1, which provides an alternative low-impedance signal path, thus bypassing the tail pole.

The offset null resistors, R21 and R23, are made larger than that strictly necessary to null the offset voltage. This reduces the transconductance of Q17 and, therefore, the noise gain of the active loads into R10 and R11. By this simple expedient, broadband input noise voltage is substantially reduced.

The voltage reference for the output stage ($V_{B2}$ in *Figure 1*) is realized by actively simulating a 4-diode stack. The voltage across Q33, given by (1 + R8/R9) $V_{BE}$, is about 3.5V. Biased at 400$\mu$A from Q30, the circuit presents a low impedance, less than 50$\Omega$, to the base of Q32. Since the TC of the reference is negative, Q34 is designed to always remain out of saturation under worst-case conditions of high temperature and high output current. This avoids potential destructive breakdown of Q32.

Current limiting for Q32 and Q34 is provided by diode-connected Q37 and resistor R12. When the voltage drop across R12 turns on Q37, it removes base drive from Q34. In a similar fashion, current limiting in the negative direction is initiated when the voltage drop across R13 causes Q38 to conduct. This current is limited in Q21 by R20 to about 1 mA. When this occurs, base drive is removed from Q39.

Although output short circuits to ground or either supply can be sustained indefinitely at supply voltages lower than ±22V, short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of their maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. As with all IC op amps, voltage reversal between the power supplies will almost always result in a destroyed unit.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.

## REFERENCES


1. R. J. Widlar, "Super Gain Transistors for ICs," National Semiconductor TP-11, March 1969.
2. J. E. Solomon, "The Monolithic Op Amp: A Tutorial Study," IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974.

Jim Sherwin
AUGUST 1975

# A LINEAR MULTIPLE GAIN-CONTROLLED AMPLIFIER

## INTRODUCTION

A linear control function over three decades of gain can be achieved with a FET in the feedback path of a non-inverting amplifier. Besides the ultimate simplicity of the circuit, multiple tracking gain control circuits can be constructed with dual op amps and monolithic dual FET's or quad op amps and monolithic quad FET's. Such circuits could even be integrated with ion-implanted FET's on single or multiple monolithic op amp chips. The gain control range may be designed for less than 2 to 1 or higher than 1000:1, but input voltage levels are limited by acceptable levels of distortion. Bandwidth is dependent on maximum gain and unity gain bandwidth of the op amp used. The gain control circuit is especially suitable for volume expansion applications.

## GAIN CONTROL WITH FETS

The FET has long been used as a voltage controlled resistor (VCR), often as the shunt arm in the series-shunt attenuator of *Figure 1.* Advantages of the FET as a VCR are that:

1. The control signal is almost perfectly isolated from the controlled signal path, and
2. The resistance can be made to vary over an almost infinite max/min ratio.

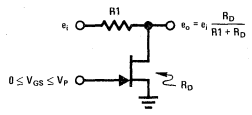



**FIGURE 1. Voltage Controlled FET Attenuator**

Disadvantages are that:

1. The FET behaves as a linear resistance only for small values of source-drain voltage $V_{DS}$,
2. Non-linearity (of resistance) increases as the control voltage $V_{GS}$ approaches cut-off voltage $V_P$ when the resistance is maximum,
3. The relationship of resistance $r_d$ to $V_{GS}$ is reciprocal rather than direct linear,
4. VCR multiples with matched resistance characteristics over their full control range have been extremely difficult to obtain at any kind of reasonable price, and
5. Production spread in $V_P$ requires separate bias set and gain set on each circuit.

Examination of the FET drain characteristics in *Figure 2* will reveal the essential non-linearity of $r_d$ at high signal levels, especially as $V_{GS}$ approaches $V_P$. This non-linear region must be avoided in order to achieve tolerable distortion levels. One obvious way is to limit $V_{DS}$ to small values when $r_d$ is high as suggested by *Figures 2c and 2d,* another is to utilize FET's with high $V_P$ as suggested by reference to *Figures 2b and 2d.*

The reciprocal relationship of $r_d$ and $V_{GS}$ is an advantage, as it is precisely that which allows the linear control of gain in the circuit to be described. The availability of matched monolithic dual FET's such as the NSC 2N3958 (watch out for the matched pairs as their resistance match close to $V_P$ may not be as good as that of the monolithic versions) make available low cost duals with very closely matched resistance characteristics over the full control range. There are even some monolithic quads becoming available (monolithic version of National Semiconductor's AH5009). The final problem of the production range of $V_P$ can be much improved with ion-implant diffusion techniques whereby lot variation in $V_P$ may be held to within a few tenths of one volt.

The gain control circuit is that of an ordinary non-inverting op amp with feedback. The usual circuit is modified in *Figure 3a* to include a FET as controlled resistor. The gain function is normal except that $r_d$ replaces R2 in the usual form.

$$A_V = 1 + \frac{R1}{r_d} \tag{1}$$

Now $r_d$ can be equated to a control voltage $V_C$ as follows:

$$r_d = r_o \frac{V_P}{V_P - V_{GS}} \tag{2}$$

Where:

$$r_o = r_d \Big|_{V_{GS} = 0}$$

$$r_d = r_o \frac{V_P}{V_C} \tag{3}$$

Where:

$$V_C = V_P - V_{GS}$$

The gain function is thus seen to be linear with $V_C$.

$$A_V = 1 + \frac{R1}{r_o} \frac{V_C}{V_P} \tag{4}$$

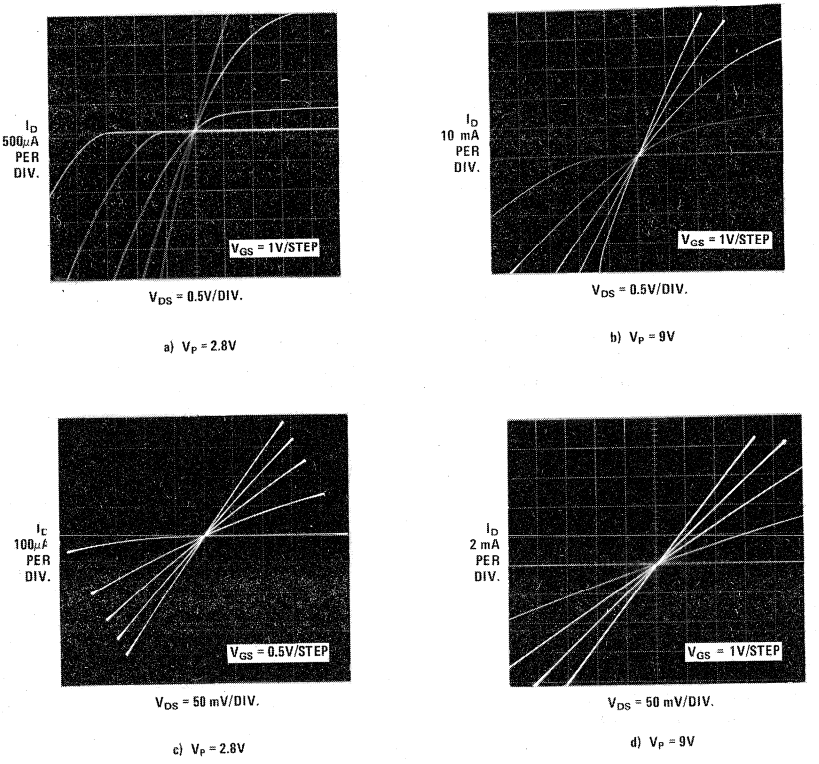



**FIGURE 2. AC Output Characteristics of FET**

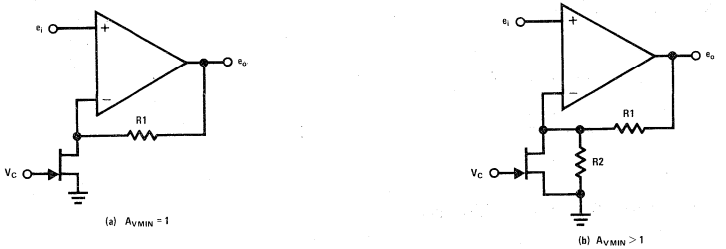



**FIGURE 3. FET/Op Amp Gain Control Circuit**

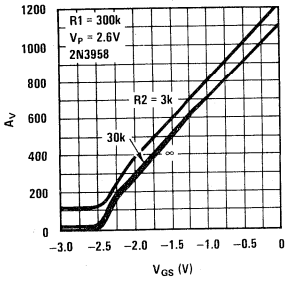



**FIGURE 4. Gain vs Control Voltage For Short Channel FET**

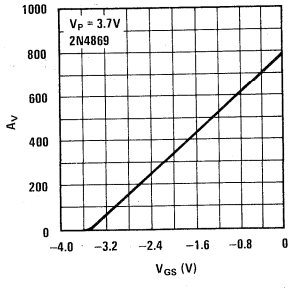



**FIGURE 5. Gain vs Control Voltage For Long Channel FET**

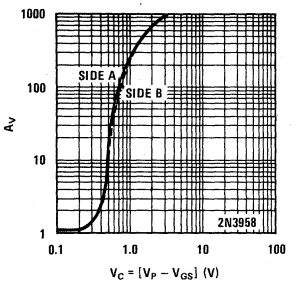



**FIGURE 6. Control-Gain Match For Dual FET**

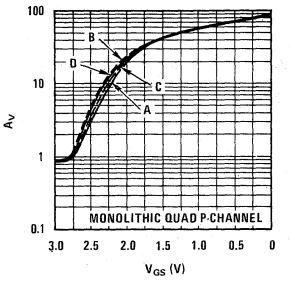
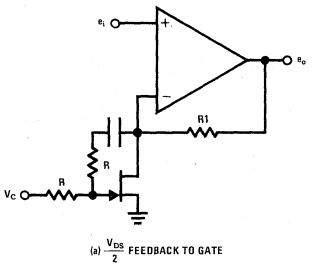



**FIGURE 7. Monolithic Quad Gain Control Tracking**



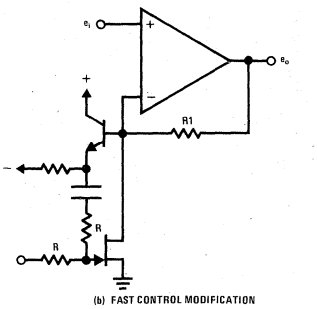




**FIGURE 8. Circuit to Reduce Distortion**

At $V_C = 0$, the gain reduces to unity; and at $V_C = V_P$, the gain increases to $1 + R1/r_o$ which may be as high as 1000 or so. If it is desired to limit the minimum gain to some value greater than unity, another resistor R2 may be added as in *Figure 3b*. Then the gain equation becomes:

$$A_V = 1 + \frac{R1}{\frac{R2\, r_o\, (V_P/V_C)}{R2 + r_o\, (V_P/V_C)}}$$

$$= 1 + \frac{R1\,[R2 + r_o\, (V_P/V_C)]}{R2\, r_o (V_P/V_C)}$$

$$A_V = 1 + \frac{R1}{R2} + \frac{R1\, V_C}{r_o\, V_P} \qquad (5)$$

In either case, the gain function is linear with $V_C$.

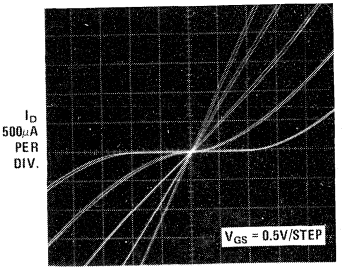
The circuits of *Figure 3* do indeed show a linear gain versus control voltage as plotted in *Figure 4* for several values of minimum gain. There is some non-linearity near minimum gain which appears in all curves. This is certainly due to a non-ideal characteristic of the FET caused by finite contact and bulk resistance at source and drain. *Figure 5* shows a similar control curve for a FET with longer channel in which the controlled channel resistance is a greater part of the total resistance than that of the short channel device of *Figure 4*. For those applications requiring a more precisely linear control of gain, the long channel devices will be preferable.

Several variable-gain circuits can be made to track when monolithic multiple FET's are used as the control elements with matched feedback resistors. A monolithic FET dual (NSC 2N3958) used in two identical control circuits shows remarkable tracking over the entire control range, even when $V_{GS}$ is near $V_P$ where variations would be expected to be most apparent. The plots appear in *Figure 6*. Similar performance for a quad gain control using a monolithic P-channel quad FET (NSC monolithic equivalent to AH5009) is shown in *Figure 7*.

## DISTORTION

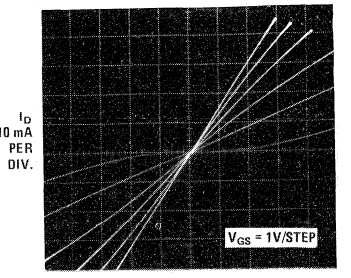
Reference to *Figure 2* will show that the FET acts as a linear resistance only for relatively small values of drain-source voltage, in either polarity. This is particularly apparent for positive $V_{DS}$ (for N-channel FET) and $V_{GS}$ approaching $V_P$. The difference between *Figures 2c and 2d* indicates that the maximum allowed applied signal will be greater for high $V_P$ as compared with low $V_P$.

It is possible to improve the linearity characteristics somewhat by applying a part of the $V_{DS}$ in series with the control voltage applied as $V_{GS}$. The circuit to accomplish this is that shown in *Figure 8*. It happens that about half of $V_{DS}$ applied to the gate provides the greatest improvement for small signals. The addition of two resistors and one capacitor as in *Figure 8a* is all that is required. The capacitor simply blocks the control voltage from the FET drain and the op amp input. *Figure 8b* shows the addition of an emitter follower to



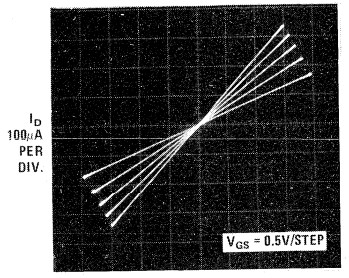

$V_{DS}$ = 0.5V/DIV.

a) $V_P$ = 2.8V



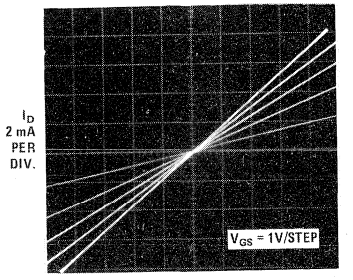

$V_{DS}$ = 0.5V/DIV.

b) $V_P$ = 9V




$V_{DS}$ = 50 mV/DIV.

c) $V_P$ = 2.8V




$V_{DS}$ = 50 mV/DIV.

d) $V_P$ = 9V

**FIGURE 9. AC Output Characteristics of FET with Feedback Linearization**

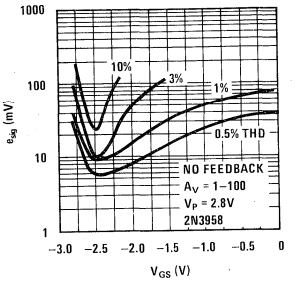



**FIGURE 10. Distortion With $V_P$ = 2.8V**

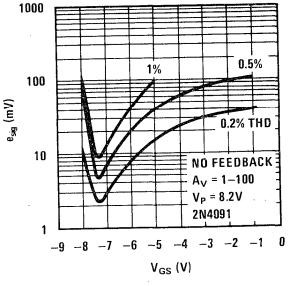



**FIGURE 11. Distortion With $V_P$ = 8.2V**

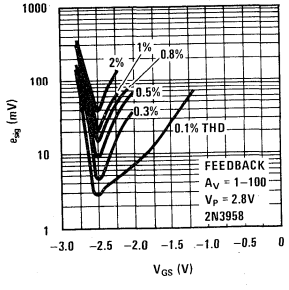



**FIGURE 12. Distortion With $V_P$ = 2.8V, With Linearization**

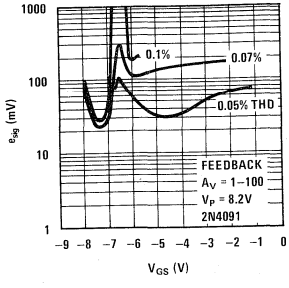



**FIGURE 13. Distortion With $V_P$ = 8.2V, Linearized**

prevent abrupt changes in $V_C$ from coupling to the op amp. *Figure 9* shows the improved linearity of the drain characteristics as compared to *Figure 2.* The improvement is also seen in the distortion versus input signal plots of *Figures 10–13.* Note particularly that the distortion at any value of $V_C$ is primarily a function of input signal (which equals the feedback signal applied to the FET drain at the inverting input). Some modification is made to this direct relationship if an R2 is shunted across the FET as in *Figure 3b.* Measured distortion at low signal level is the result of noise rather than of signal distortion. Maximum gain is limited to about 100 in these plots so as to avoid the region of lower S/N. The noise is that of the op amp input stage and the signal source resistance plus the contribution of the FET which is essentially the thermal noise of $r_d$.

## BANDWIDTH AND CONTROL TIME CONSTANT

The circuit bandwidth is the closed loop bandwidth of the op amp used at the (instantaneous) set gain. The gain control time constant is that of the input circuit to the FET (dependent on the value of R in *Figure 8*) limited by the slew rate of the op amp. The FET itself reacts practically instantly, producing a step change in feedback ratio. Control time constant is thus a few microseconds at most.

## APPLICATIONS

Three obvious applications present themselves; they are:

1. Remote or multichannel gain control

2. Volume expansion

3. Volume compression/limiting

To this short list might be added a number of others, including applications in noise reduction and quad sound techniques.

The gain-controlled amplifier of *Figure 14* has a gain range of 1–1000, a maximum output level of 8.5 Vrms, and a bandwidth of better than 20 kHz at maximum gain. The FET used has high $V_P$ for maximum freedom from distortion. *Figures 15 and 16* show the gain function and constant distortion contour lines. Note that the gain control curve is non-linear near unity gain because the 2N4091 is a short channel FET. Distortion is quite low except as limited by maximum output voltage. Note that the maximum $e_{in}$ is restricted by output saturation. The LM318 is used in the example only to achieve wideband response at maximum gain. The amplifier input voltage must be restricted to about 8 mVrms at maximum gain when the S/N will be about 60 dB over a 10 kHz bandwidth.

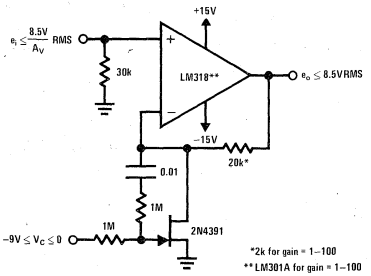



**FIGURE 14. Amplifier With Gain Range = 1–1000**

A more practical circuit might employ a gain range of 1–100. Then the amplifier could be a LM301A and still achieve a 10 kHz bandpass at maximum gain. The input signal could, accordingly, be increased to 80 mVrms for a S/N of 80 dB. This performance can be extended to dual and quad control circuits with tracking gain functions, but watch the bandwidth as required at maximum gain. Any of the several dual op amps could be used with the 2N3958 (monolithic dual from NSC), or the LM324 quad op amp can be used in limited gain times bandwidth applications with a quad monolithic FET. *Figure 17* shows all details of an ac coupled tracking quad gain control with 40 dB range. Gain varies over 1–100 range, bandwidth is 10 kHz minimum, S/N is better than 70 dB with 4.3 Vrms maximum output. *Figure 7* shows the gain curve and matching characteristics.

Noise considerations could be important in this method of gain control, as the signal is amplified rather than attenuated. To realize the function of a 40 dB variable attenuator, it is necessary to install a fixed attenuator at the amplifier input and perhaps also at the output. This will reduce the minimum signal level to millivolts, thus a low noise amplifier is desirable. The LM381 dual low-noise ac coupled amplifier could be used in a 40 dB

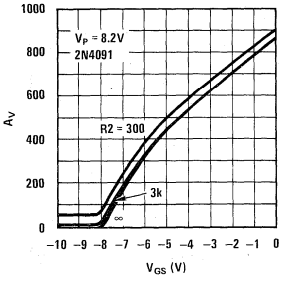



**FIGURE 15. Gain For Circuit of Figure 14**

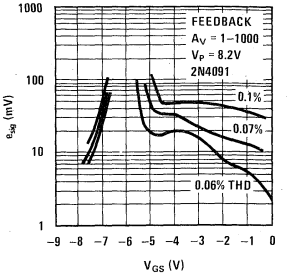



**FIGURE 16. Distortion For Circuit of Figure 14**

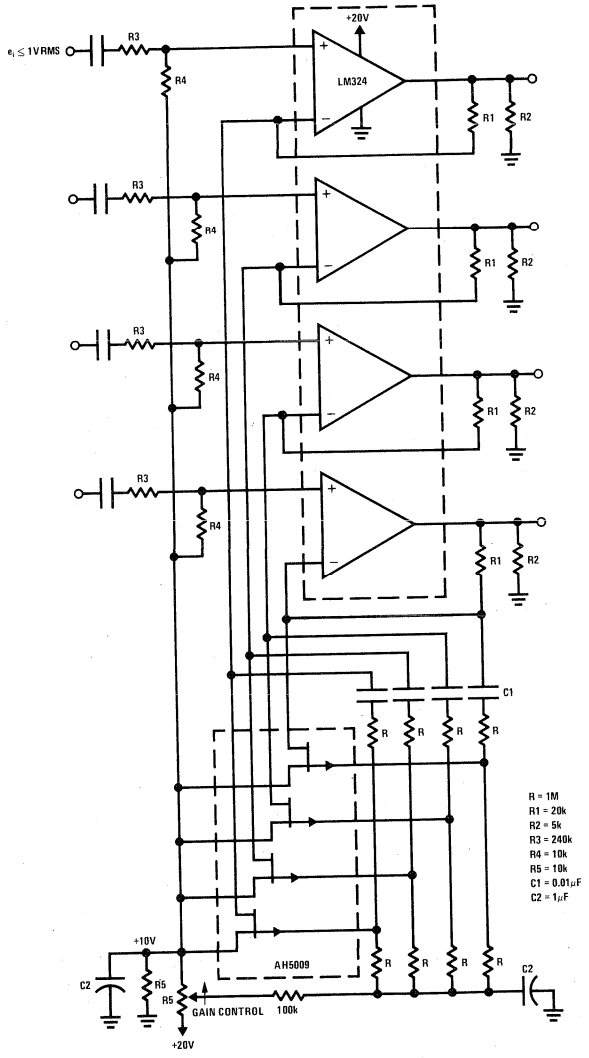



FIGURE 17. Quad Gain Control

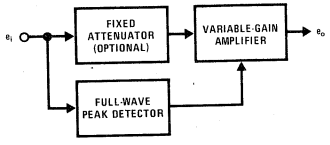



FIGURE 18. Volume Expander/Compressor Block Diagram

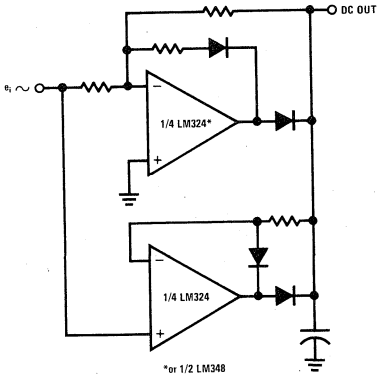



FIGURE 19. Full Wave Linear Precision Peak Detector

audio attenuator to realize S/N about 100 dB or in a 60 dB attenuator to realize 80 dB S/N. Improvements in S/N can be made by reducing system bandwidth in fixed or low frequency operation. Minimum noise is also achieved by using the minimum practical amplifier source resistance. Values as low as 1 kΩ are advantageous.

The effect of temperature will be to change the gain according to the temperature sensitivity of the FET. This effect can be reduced by using a silicon resistor for the feedback resistor, R1. If the FET were to be integrated onto the op amp chip, an attempt should be made to include R1 on the chip as well.

The application to a volume expander circuit is of interest as the control is linear, the required control range is only about 1:4, and the input signal is small for the low gain condition when distortion would otherwise be most apparent. The elements of a volume expander are indicated in *Figure 18.* The gain controlled amplifier need only exhibit a 12 dB variation in gain, being lowest for small signals. The slope of gain versus control should be linear, more specifically the slope of (log) gain in dB versus (log) signal in dB should be linear. A practical range is 12 dB gain change over a 30 dB input signal range. The peak detector should be linear down to very small signals, exhibit a fast attack or charge time of a millisecond or less, a discharge time constant of about 2 seconds, and operate on the first half cycle (full-wave detector). The detector should, therefore, be a full-wave precision linear peak detector with low internal impedance; the requirements can be met with the circuit of *Figure 19.*

The expander circuit shown in *Figure 20* will perform as desired. The gain control function is plotted in *Figure 21;* distortion is below 0.1% at all levels. Resistors R3 and R4 are added in order to modify the linear control curve to the desired log curve. Note that the input signal is attenuated prior to amplification in order to reduce distortion and maintain an overall gain of approximately 0 dB at midrange of expansion. The noise with the LM124 over a 20 kHz bandwidth is, of course, a function of signal; but the maximum signal to noise ratio is 80 dB. The circuit could be adapted to stereo or quad sound as in *Figures 22–23.* Questions for individual design concern the method of control. Whether to expand all channels together, and whether to derive the control signals individually from each channel, a summation from 2 to 4 channels, or from a single channel (assuming that high level from any channel indicates high levels from all channels). Note that the FET is biased OFF (minimum gain) for low signals, and increasing signals progressively bias the FET ON (maximum gain).

The volume compression circuit is a logical mate to the expander. The only difference would be that the FET is initially biased ON (maximum gain) for low signals, and

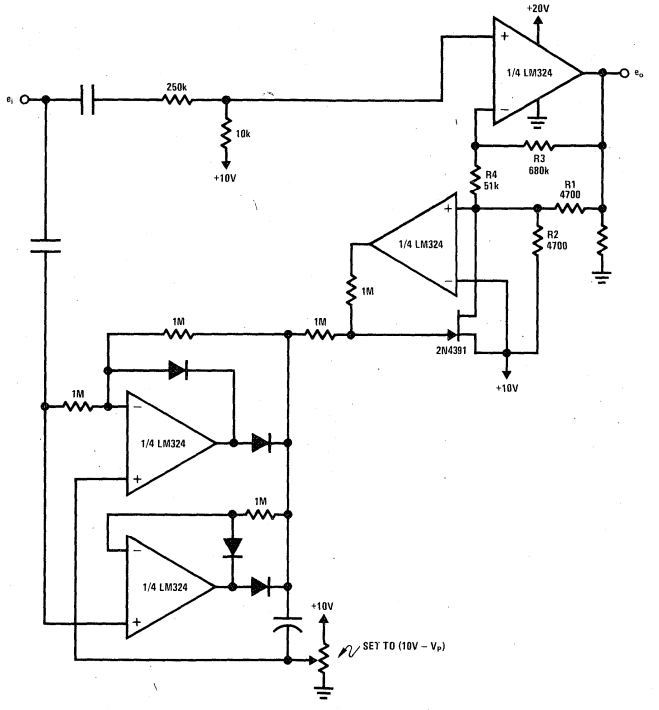



**FIGURE 20. Volume Expander Circuit**

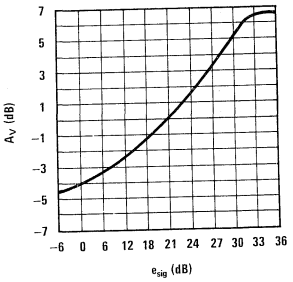



**FIGURE 21. Expander Gain Characteristic**

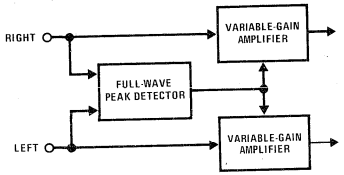
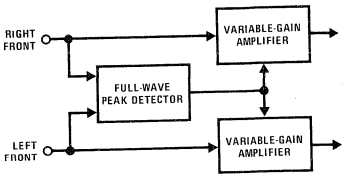



**FIGURE 22. Stereo Expander Block**



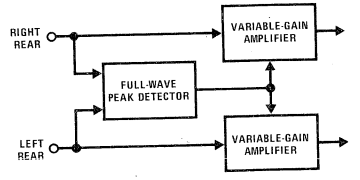




**FIGURE 23. Four-Channel Expander Block**

increasing signals progressively bias the FET OFF (minimum gain). A disadvantage is that the circuit produces greatest distortion in the low gain condition when signals are highest. Maximum S/N is degraded by 24 dB over that of the expander, minimum S/N is the same.

## CONCLUSION

The combination of FET and op amp provides a linear dc (voltage) control of gain over a range to 60 dB. As the circuit realizes positive gain, rather than being a controlled attenuator, the input signal is limited. Input signal is further limited to several hundred millivolts by the non-linearity of the FET (which sees the full input signal). Because input signals will generally be in the 10–300 mV range, noise performance of the selected op amp will be important. Even so, S/N of 60–100 dB is obtainable with standard amplifiers. Tracking pair or quad gain-control amplifiers are realizable with existing monolithic dual or quad FET's, and the combination of FET and op amp lends itself to simple integration. The circuit is well-suited to remote and multiple linear gain control and to volume expander/compressors. The volume expander is especially interesting as the signal level and gain conditions result in extremely low distortion and more than adequate signal-to-noise ratio.

Peter Lefferts
DECEMBER 1974

# THE MONOLITHIC TEMPERATURE TRANSDUCER–A NEW INTERFACING CONCEPT

## INTRODUCTION

The percentage of analog and analog/digital signal handling done by monolithic integrated circuits is ever increasing. However, until now almost all input signals were voltages generated by often complex and expensive transducers needing special input wiring to the integrated circuit.

Now with the ability of an IC to *directly* sense absolute temperature, and provide a linear, buffered electrical output, the situation has greatly changed. A number of physical parameters can now be sensed directly by the National LX5600 monolithic transducer with a resulting saving in hardware, wiring, and therefore cost.

For example, using temperature sensing as an "interface"; position, air velocity, liquid presence, and conductivity can be measured or controlled. Rate of temperature change can be sensed to improve the performance of on-off temperature controllers. The monolithic transducer allows a much simplified servo for improving surface or moving-surface temperature measurements. The purpose of this note is to illustrate the possibility and practicality of a number of these sensing techniques.

As background for the rest of this note, the block diagram and operation of the thermometer will be briefly described. Also methods of powering the LX5600 will be outlined, and a special integrated power transistor ideal for isolating the thermometer from heavy or variable loads will be presented.

## TRANSDUCER DESIGN

*Figure 1* illustrates how the 3 separate functions of the thermometer IC are arranged so that only 4 external connections are needed. The zener and its amplifier form a shunt regulator with a typical impedance of 3Ω. The reference is quite stable with temperature so that a potentiometer across pin 3 and 4 can be used to set up a Centigrade or Farenheit zero calibration. This would be used when the thermometer is applied in its linear mode, such as with pins 1 and 2 shorted together so that the op amp forms a unity gain follower.

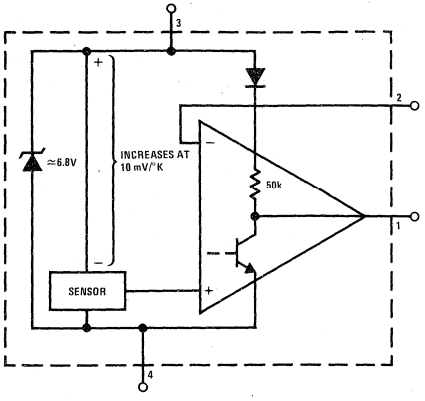



**FIGURE 1. Block Diagram**

Similarly a pot across 3 and 4 with the wiper to pin 2 determines a temperature set-point since the op amp can be operated "open loop," which will cause the output at pin 1 to swing about 30V for a 0.2°C (or Kelvin) change at the sensor around the set point.

The sensor section, with its associated amplifier, generates a negative going signal of 10 mV/°K. For instance, at 0°C this signal would be −2.73V (with respect to pin 3) and appear at the plus terminal of the internal operational amplifier. The actual sensor principle is somewhat more sophisticated than a resistance or diode-drop change with temperature. It uses the difference in $V_{be}$ between matched transistors which involves operating two transistors at greatly differing collector currents but with their bases in parallel. If this collector current ratio is controlled there will be a very predictable difference of emitter voltage. Further, this voltage varies with temperature in a known and reproducible manner. This voltage change is less dependent on processing variations than any of the other known semiconductor effects. Further details on these effects can be found in the reference. (1)

The internal op amp provides a consistent, very light loading of the sensor output. Having a feedback terminal available, gains from unity up to 100 or so are feedback controllable, or an open-loop gain of several thousand is available. PNP input transistors allow the op amp to function as a comparator over a large range of inputs. Internal compensation is provided. Output is a collector with a 50k load (pull-up) resistor provided, that is, however diode decoupled for output voltages higher than the pin 3 supply voltage. A complete schematic of the transducer is provided in the appendix.

## POWERING THE TRANSDUCER

Successful application of the LX5600 starts with providing power in the optimum way. Since the device senses its own temperature, it follows that minimum internal power dissipation is desirable. With no output load, the internal electronics (op amp, etc.) typically need about 1/2 mA to operate correctly. If the zener shunt regulator is to operate also, 1 mA is recommended. Let us examine the four powering methods of *Figure 2* with regard to zener operation and temperature rise. Still air operation, a 6.8V zener, and 0.17°C/mW temperature rise for a TO-5 package are assumed for the following discussion.

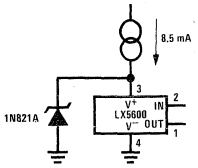



FIGURE 2a. Constant Voltage Mode

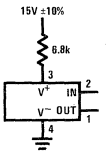



FIGURE 2b. Dropping Resistor Method

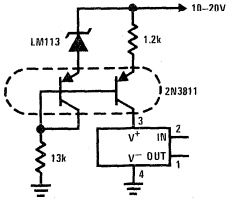



FIGURE 2c. Precision Current Source

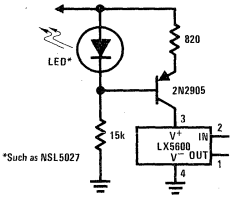



FIGURE 2d. Low Cost Current Source

FIGURE 2. Powering the Monolithic Transducer

*Figure 2a* illustrates minimum device dissipation by sacrificing use of the internal reference. A typical unit would self-heat only about 0.5°C and would vary only about 0.1°C over supply and temperature variations. This connection is particularly useful for accurate air temperature measurements and is very suitable for differential measurements where a second transducer can supply the reference.

The simplest method is *Figure 2b* using only a resistor. With the supply variations shown, the reference typically varies less than 1 mV. The temperature rise is only about 1.25°C with plus or minus about a quarter degree for supply variations. With a modestly-regulated supply, the resistor powering method obviously becomes very good. However, if one considers an aging automotive battery with a loaded output of only 11V available, a 3.9k resistor would be needed to insure 1 mA of current. Then the same battery being heavily charged (15 $V_{DC}$) would supply twice the current to the thermometer with an *increase* of self-heating of about 1.2°C.

One of the applications to follow involves reading outside air temperature. Since most people are accustomed to reading temperature in °F, the over 2°F error of the above example will be noticeable. The two constant current supplies to be described solve this problem. Total *change* in self-heating becomes well less than 0.1°F over a 100°C temperature range and a 2:1 supply voltage range. Further, the internal reference is properly powered, with current changes causing less than 1 mV change in $V_Z$.

The reference current source of *Figure 2c* uses the precision 1.22V reference diode which changes only about 1% over the entire −55°C to +125°C temperature range. A diode-connected transistor, temperature compensates the constant current transistor so almost exactly the reference voltage appears also across the emitter resistor, stabilizing the current.

The source of *Figure 2c* is probably of greater cost and precision than is needed in this application. The *Figure 2d* current source is much less expensive and yet reasonably stable. With only about a volt needed between power input and collector output, it is much superior to the usual zener referenced current source requiring 5 to 6V of such loss.

A little used characteristic of light emitting diodes is employed in stabilizing this current source. At the low currents used, the LED has a typical drop of 1.5 to 1.7V, or about 0.8 to 1V *more* than the junction drop of a small transistor. Thus, when paired as shown in *Figure 2d* the remaining voltage appears across the transistor's emitter resistor. Further this voltage is temperature *stable* since the LED's junction temperature coefficient is just about the same as a transistor's base-emitter junction coefficient. In both cases this is about −2 mV/°C. Preliminary tests indicate that adjustments of the temperature coefficient can be made by changing the ratios of transistor to LED current, and that once a stable combination is found similar parts (same part number and same process) should reproduce the stability obtained within 1 or 2%, over the −55°C to 100°C range. Doubling LED current only results in approximately 40 mV increased junction drop, so a 2:1 supply change will only result in a 5% further current change.

## OPTIMUM LOAD ISOLATION

The need to minimize power dissipation has already been emphasized. In fact the previous heat rise figures were based on zero load on the thermometer's output transistor. Certain of the applications to be presented involve driving of lamps, solenoids, or heaters. Much would be lost in simplicity if the thermometer had to drive a buffer amplifier followed by two or more cascaded power transistors.

To solve this problem the LM195/LM395 monolithic power transistor is used. An ampere of load current may be handled requiring only a few microamperes drive from the monolithic thermometer. Under this condition, power dissipation due to the thermometer's output signal can be as little as 1% of the total device dissipation, and thus be negligible in causing temperature error.

The block diagram of *Figure 3* shows how this very high gain is achieved. Integrated on the same chip as the power transistor is an NPN emitter follower driver which is driven by another PNP emitter follower. The

emitter-base drops of these two drivers are in the opposite direction, and tend to substantially cancel. Remaining is the emitter-base drop of the power transistor so input signals seem to see a power transistor of normal input voltage but abnormal current gain resulting from the three transistor cascade. Further, the input resistor and integrated PNP transistor allow +40V and −20V overdrives to the base without damage.

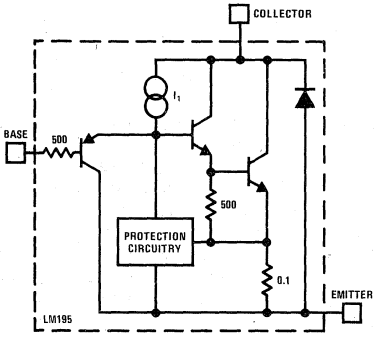



**FIGURE 3. Simplified Circuit of the LM195**

Reliability under adverse environments is enhanced by other protective circuitry that has been integrated in with this transistor. Collector current is limited to 2 amperes by sensing drop across the 0.1Ω emitter resistor internally. Junction temperature is limited by turning off the output transistor at 170°C junction temperature, using an internal temperature sensor. Thus the LM195 is extremely difficult to destroy except by exceeding collector voltage from a low impedance supply. (2)

## APPLICATIONS AREAS

Applications areas will be covered in two sections. First, in the obvious area of temperature sensing and control, several uses with different types of output signals will be illustrated. Then some other sensing functions will be covered. All circuits shown have been breadboarded and are functional, but have not been given field testing at this time.

When a 15V supply is shown, the circuit is assumed a lab or instrument application. When a supply varying from 11V to 15V is shown, it is intended that this represent a 12V automotive battery or similar unregulated supply. The circuit has then been tested over a range of 10V to 16V, without significant degradation of performance.

## TELEMETRY INTERFACE

Various pieces of mobile test equipment such as instrumentation recorders or telemetry subcarrier VCOs operate best with a calibrated 0 to +5V input. In some cases a low output impedance is also helpful. The LX5600, for certain design reasons, indicates increasing temperature by a negative going voltage with respect to the positive supply pin. Thus the thermometer's output must be inverted, level shifted, and given an extra voltage gain of 4 to provide the illustrated output.

*Figure 4* provides the methods of doing this. Q1 supplies the thermometer with a constant current as previously described. The output transistor, Q2, provides the inverting function and requires very little base drive, holding down transducer dissipation. The entire system now requires dc feedback around it to stabilize gain (and thus the full scale calibration) and to eliminate supply and base-emitter voltage variations from the output. Feedback to pin 2 of the transducer is shown (by *Figure 1*) to be the "minus" input to an operational amplifier within the transducer. Thus the output signal needs to be reinverted by the LM201A operational amplifier.

The system has an open loop gain of 5,000 to 10,000, so the attenuation of the output signal that is fed back negatively determines closed loop gain. The reinverting op amp actually has an attenuation of 0.27. The 250Ω pot in the output divider is thus the full-scale adjust and trims the attenuation to 0.25, or a gain of 4. Pin 3 of the transducer provides the voltage reference for the zero adjust divider. At the calibration point of 0°C, the LM201A output must be at a nominal 2.73V below pin 3 of the transducer. Since voltages at both ends of the 30k, 110k network are known at 0°C, it is easy to predict the voltage adjustment at pin 3 of the LM201A required to fulfill this condition.

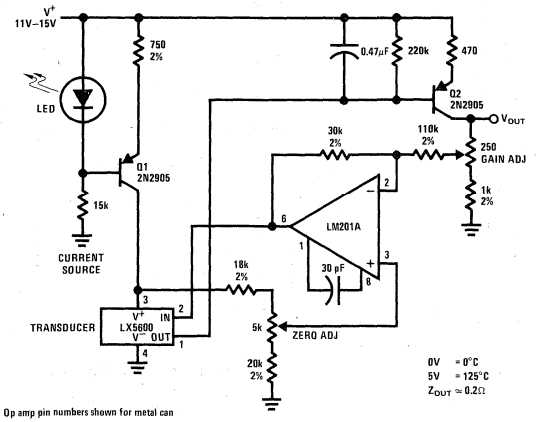



**FIGURE 4. Telemetry Interface**

The 0.47$\mu$F capacitor loading the transducer's output is required for stability against oscillations. The system has a very long feedback loop (3 different amplifiers), thus it is extremely easy for the total phase shifts to become 180° at a relatively low frequency. The large capacitor lowers overall gain to less than one at a frequency much less than this. There is no adverse effect on performance since temperature is such a slow moving parameter.

By design, the full-scale adjust has no effect when $V_{OUT}$ is at zero. This means that if zero is calibrated first, and full-scale second, the controls are non-interacting. Calibrating to 4V out, at boiling water temperature may be convenient. The unit we calibrated exhibited a 0.1% independent linearity up to 100°C, and less than 2 mV output change (1/20°C) with a 4V supply change. One little trick is needed for exact zero calibration. Due to loading by the op amp network, a temporary bias of about 0.1 mA is needed at the full-scale pot wiper to read a true zero out. The minus current can be temporarily provided by a 100k resistor and 9V "transistor battery." Obviously, other calibrating points can be chosen, and other ranges can be obtained by changing the different resistor networks.

A few precautions may be needed. For maximum accuracy three of the ground points should be common, or brought to the same point with separate wires. These points are the bottoms of the two dividers, and pin 4 of the thermometer. The others are less critical. If long wires, or a noisy supply is anticipated the $V^+$ pin (pin 7) of the LM201A should be bypassed. Since the $V^-$ pin of the op amp is at ground, resistor networks for other ranges must be such that none of the input or outputs have to go closer than 2V to ground (3V under coldest conditions).

For the purposes of this and other circuits discussed, resistors are all 1/2 watt unless noted, and have the following characteristics. One percent resistors should be high stability metal film or wire wound types (e.g., 50 ppm/°C). Resistors marked 2% can be lower cost medium stability types such as tin oxide. Others can be standard 5% carbon types.

## TEMPERATURE TO FREQUENCY CONVERTER

For test data transmission, or to interface conveniently with existing digital displays, a proportional frequency signal may be desirable. In trying to determine the lowest cost package for an automotive exterior temperature indicator, a novel system evolved. It was obvious that a simple circuit in the same protective enclosure as the transducer would minimize cost and wiring. If the single positive supply wire could be made to carry the output signal frequency, it would represent an irreducible minimum cost to hook up.

The above aim was achieved using only the transducer, a very low cost IC (array), a few external parts, and a single supply/output wire. During the short negative output pulses on the supply wire, an internal 22$\mu$F capacitor keeps the converter electronics running. Pulse repetition rate is directly proportional to absolute temperature. Again, a LED/transistor constant-current source provides an ideal, modulateable supply from a varying voltage source.

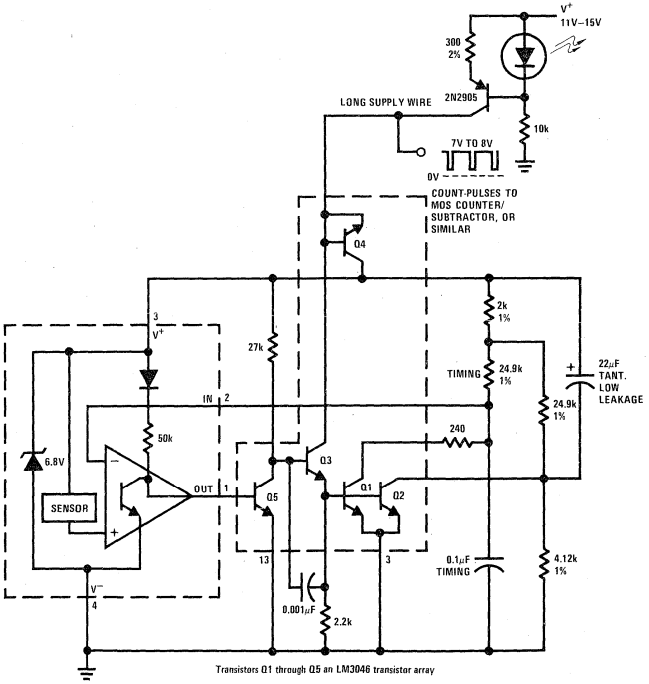



**FIGURE 5. Temperature to Frequency Converter**

The type of oscillator is similar to a number of "timer" circuits. A capacitor ramps up to a reference voltage, and trips a comparator. The comparator immediately lowers the reference to another fixed point and starts the ramp down. Upon reaching the lower reference the conditions are reversed.

In the converter, there are three slight differences. For one, the run-down of the ramp is made very fast, and contributes negligibly to the timing. Secondly, the upper reference the ramp charges to, moves negatively in linear proportion to temperature. Finally, the lower reference is controlled to be a fixed voltage below the upper at all times. This controls the generated sawtooth to a fixed amplitude at all times. However, since the upper comparison limit moves down with increased temperature, the whole dc level of the sawtooth moves down, increasing voltage across the charging resistor linearly with temperature.

Following are the detailed functions of the various components. The op amp inside the transducer is operated open-loop as a comparator. The 0.1$\mu$F timing capacitor is connected directly to the minus input of this amplifier and causes its output to switch "low" when capacitor charge reaches temperature sensor voltage. Transistor Q5 inverts and speeds up the op amp switch transition, and drives the base of Q3. This transistor's collector puts the negative pulse on the supply line, while its emitter drives the bases of Q1 and Q2. As a result, Q1 starts discharging the timing capacitor, and Q2 switches the bottom of the 22$\mu$F filter/coupler capacitor to ground.

This is an important step as it determines exactly how far the timing capacitor discharges. It can be seen that due to the large filter capacitor, voltage at the transducer's pin 3 is immediately lowered by the amount of voltage that had appeared across the 4.12k resistor. The sensor and op amp "plus" input follow this drop exactly. Therefore the new comparison point (toward which the timing capacitor is discharging) is lower by exactly the voltage drop of the 4.12k resistor. This voltage sets sawtooth amplitude to about 1V, with the upper and lower limits following temperature as described.

The voltage across a capacitor is predicted by current x time, divided by the capacitance. Since frequency has the units 1/t then:

$$f = \frac{1}{CV} \qquad (1)$$

In other words, frequency will be linear with current change; with a fixed capacitance and a constant voltage change across the capacitance. There are some second order effects due to the slight change of the RC curve as charging percentage varies from about 30% cold to 20% hot. This was measured as less than 2°F out of a range from −68°F to +127°F. It is believed a compensation can be arranged for this small effect.

The remaining transistor, Q4 of the array, is connected so its collector becomes a decoupling diode. When the supply is modulated with the large negative output pulse, the charge on the critical filter/coupling capacitor is not substantially disturbed during the 10$\mu$s or so discharge time.

There is a simple, but interesting advantage to the single-package concept for the T/F Converter. Since it shares the same thermal environment with the sensor, linear changes with temperature of the oscillator components can be calibrated out as part of the entire system's frequency change with temperature. This somewhat relaxes the requirement for premium components.

## PROBE WITH SERVO'D SHIELD

When only part of a sensor can touch a surface to be measured, it has difficulty reaching the actual surface temperature. This is due to radiative and convective as well as normal conductive effects from all parts not touching the surface. Errors may be 10 or even 20% of the amount by which the surface is hotter than ambient. A very large improvement can be obtained if the sensor is surrounded loosely on all but one side by a thermal shield. The shield should be actively driven to within a degree of the surface temperature.

It sounds like going in circles, (i.e., knowing the surface temperature in order to measure it). However, the system is made to work by having the shield *track* the actual surface temperature sensor. If the coupling between surface and sensor is just a little better than sensor to shield, the whole system converges on a accurate final reading. This explains why there is *insulation* between sensor and shield, while the servo control sensor is soldered directly to the heater transistor.

*Figure 6* provides the mechanical details of the system. The LM195 power transistor is both the main power amplifier and heater, being capable of about 23W of heating as shown. Internal current and thermal limit make this a safe and practical mode of operation, and places a great deal of heat in a small area. The system is also surprisingly fast, with the application of heat electrically being sensed within 1/2 second by the servo sensor. The servo sensor is closer to the heat generating silicon die than any of the rest of the system.

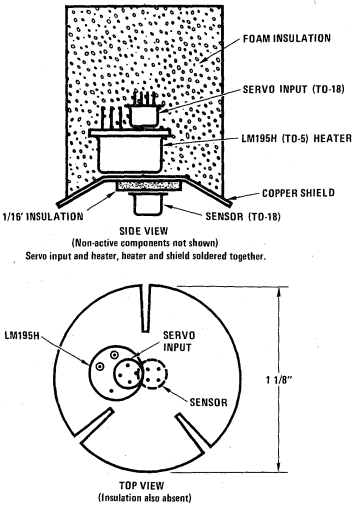



**FIGURE 6. Servo'd Shield**

Circuitry available inside the LX5700 sensors makes the Servo'd Shield Schematic, *Figure 7*, extremely simple. The close tracking of sensors after adjustment, simply allows the output of the surface sensor to become the setpoint signal for the servo input sensor. The 27 kΩ and 3 MΩ resistors set the servo's op amp gain to about 100. This is needed because the LM195H decreases in required base drive as it heats up, thus appearing to add positive feedback, increasing gain of the system. The 100k/56k divider provides a helpful level shift and absorbs bias current generated by the integrated power transistor.

The 100μF capacitor compensates for an interesting thermal characteristic of the system. Especially at lower temperatures, the power transistor heats at least an order of magnitude faster than it cools. The LX5700 op amp can sink much more current than it sources, so the capacitor establishes a slow turn-on, fast turn-off base signal to the LM195. This compensates the system to prevent large heating overshoots.

Several of the other components need explaining. The diode in series with the sensor ground leg allows the internal zener to be non-conducting, so that pin 3 can be adjusted up or down the 40 to 80 mV necessary to cause the two thermometers to track. A DVM with two digits to the right of the decimal will read directly in °C by moving the point right two places. The meter can be zeroed at 0°C by the 1k trimmer. The heavy filter at the "Lo" or minus input to the DVM is needed because many meters with "floating" input are not well isolated, and inject noise back into the sensing system. The negative going thermometer output at the minus DVM terminal enables the temperature displayed to have the correct sign.

As a cautionary note, the 2-wire ground system as shown is needed to reject feedback caused by initial large heating current surges drawn by the LM195H. Passive components shown as in the probe can be in the foam insulation (on standoffs or a miniature board) but would be better placed above the insulation to avoid heating them to probe temperatures also.

## THE ANTICIPATING CONTROLLER

If the conditions are right, and the hardware available, the anticipating controller can be executed rather simply. Normally 2 amplifiers and about 3 different kinds of feedback are required to make a controller stable *and* accurate under varying load conditions. This is due to the unavoidable delay between application of heat and a usable sensor output. The anticipating controller adds a selected amount of phase *leading* signal to the normal amplified output from the temperature sensor. This, at least partially, compensates for the sensing lags.

In the system shown, heater/sensor delays up to about a minute can be compensated for. A simple electronic system can be constructed because of the high sensor output obtainable (100 mV/°C) and the very low bias currents required by the LM216 op amp. This allows use of the 100 MΩ feedback resistor and thus very high differentiator (or anticipating) gain without significant errors. In a test using a heated plate with about a 30 second lag from ideal response, addition of the anticipating signal decreased thermal oscillations from 3° to one or two tenths of a degree.

The LX5700 amplifies its normal 10 mV/°C by about 10 due to the feedback network for its internal op amp. The feedback resistor is the 100k pot and the other gain setting resistance is the series combination of the 5.6k resistor and the setpoint pot resistance at the wiper. The dc gain of the LM216 op amp is set by the 10 MΩ and 100 MΩ resistors at another factor of 10, yielding 1V/°C. Differentiator gain is set by the same 100 MΩ resistance and the 2μF capacitor. A temperature change of 1/20°/second would result in a 1V output if the 100k pot were set to maximum differentiator gain. The 33k resistor in series with the differentiating capacitor, and the 0.001μF feedback capacitor serve to limit high frequency gain and reduce the effects of noise and

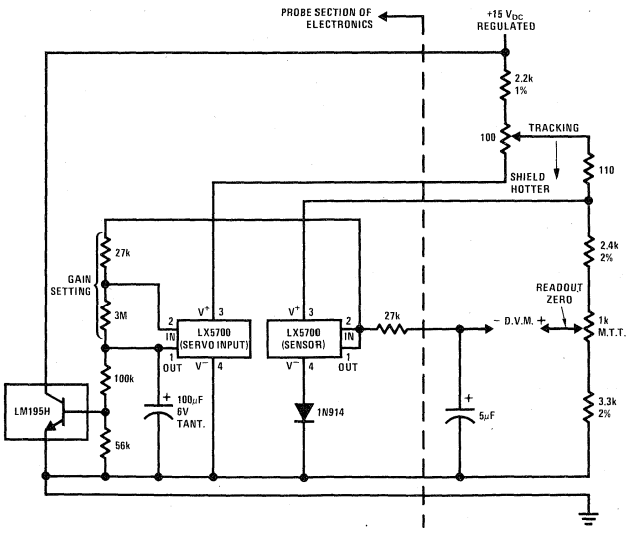
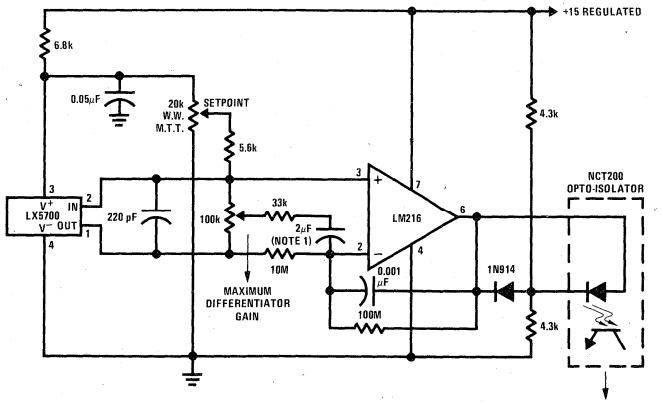



**FIGURE 7. Servo'd Shield Schematic**




Note 1: Must be low leakage film dielectric type.
Note 2: Connections to LED and diode can just be reversed for reverse control action.

**FIGURE 8. Anticipating Controller**

pickup which can otherwise be greatly emphasized in a differentiator.

The output circuit energizes the opto-isolator when the op amp output swings somewhat above the supply centertap set by the two 4.3k resistors. Depending on divider value, current gain of the coupler, and sensitivity of its load, almost arbitrarily small changes of temperature or *rate* of temperature change may control heating or cooling. In some cases gain will have to purposely be reduced to get a stable control point.

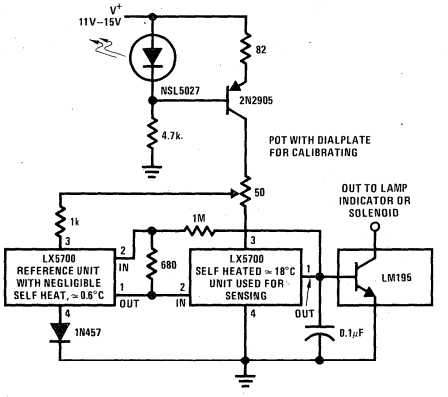
## OTHER SENSING FUNCTIONS

Temperature is easy, but what about temperature difference? Monolithic transducers are very good at sensing this because of their close tracking and the capability of delivering from tens of millivolts to many volts of output for each °C of temperature difference. Any physical process that generates a small temperature gradient to ambient or a reference can be sensed by a pair of transducers. This potentially involves chemical processes, friction, compression of gasses, radiation, evaporation, and a whole raft of heat generating or absorbing phenomena. Three rather simple such applications will be illustrated.

### Liquid or Moving Air Detection

*Figure 9* shows a basic 2 sensor configuration for performing a number of differential temperature functions. As noted, one sensor is heated considerably by internal dissipation, and the other is biased slightly lower at supply voltage pin 3 so that if the "hot" sensor lost half its excess heat, its output (operating essentially open loop) will switch to a "high" state. This of course turns on the power transistor. The feedback network consisting of a 1M resistor and 680Ω resistor provides slightly less than 1/2°C hysteresis or snap action which prevents partial outputs or oscillation near the setpoint.

Adjustments are not too critical due to the large temperature differences that are created. Cooling of the sensing unit by an electrically non-conducting liquid (such as oil) is about 16°C. Still liquid was used for the measurement. Air at about 400 FPM (a little under 5 mph) provides about 10°C cooling.




Output "OFF" if sensing unit becomes hot, i.e., out of liquid or airstream.
Reference unit is 1 inch from the sensing unit in airstreams, and below the sensor in liquid sensing systems.

**FIGURE 9. Liquid or Moving Air Detection**

For either application the adjustment is fairly simple. With the sensing transducer in the "hot" condition (still-air, or out of liquid for 2 minutes) find the pot setting that just turns the power output off. Then with the sensing transducer in the cool condition (in liquid or moving air) for 30 seconds, find the setting that just turns the output on. Since these two settings "overlap," a final setting between these two will provide stable operation. If it is noted that response in the heating direction is markedly slower, displacing the adjustment toward the "cool" setting (referring to the pot dialplate) can partially compensate for this.

If the detector is used as a failsafe sensor in a system cooled by a fan, the sensor's self-heating delay gives time for said cooling fan to come up to speed without requiring a special delay or override for system start-up. Speed of response can have good or bad effects on the over-all system. The sensors are essentially slow enough so that momentary air blockage or liquid splashing won't give erroneous signals. In liquid sensing, drops

adhering to the sensing transducer can slow it down by 2 or 3 to 1. A "drip point" such as 3/8" long piece of #28 bare wire soldered to the lowest part of the case helps. Insulating supports, or lead insulation, within 1/2" of the sensing LX5700 slows it down considerably.

**Wind Velocity**

Actual "air speed" has more effect on gasoline mileage than road speed at above 40 mph. Further there is great interest by sailboat racers as to wind velocity or air speed. Again, a differential between a heated and unheated transducer can be used in this sensing job.

Briefly, the setpoint input (pin 2) of the transducer that is to sense velocity, is biased so that its voltage is always equivalent to a number of degrees above ambient. This voltage is obtained by adding a small dc level to the output of an ambient sensing transducer. The output of the velocity transducing LX5700 is used to control its own heating; holding it the specified number of degrees above ambient. The current to do this is measured, and is obviously a measure of the amount of heating required. As wind velocity rises, so does this current as the transducer "servo's" its temperature to a constant amount above ambient.

In *Figure 10* this amount of heating is set by the wiper voltage of the 20k pot into the 100k/4.12k divider. The bottom of this divider is driven by the LX5600 air temperature reference, connected in unity gain mode. The output of the velocity sensor drives the base of Q1. If this sensor cools, Q1 base goes positive, reducing its emitter current and collector current. The current drawn by the 620Ω collector load doesn't change significantly however. The current now *not* supplied by Q1 is drawn instead through D2, through the meter, and eventually through the reference zener of the velocity sensor. This of course heats the sensor, closing the feedback loop.

The system is made electrically stable by the 0.1 compensating capacitor and the fact that Q1 exhibits practically no collector voltage gain. Q2 is not normally conducting, but it and the divider on its base provide a clamp voltage for the Q1 collector. This prevents a "latchup" mode that occurs if Q1 happens to draw a transient current pulse. The "zero velocity current" adjustment allows this heating current needed at zero velocity to bypass the meter. To avoid a low velocity discontinuity, it is probably best to "zero" the meter at about 1% of full scale.

Sensor Arrangement as shown in *Figure 11*, minimizes the sensitivity of the system to vertical components of wind, and limits the exposed part of the sensor to a controlled area (no lead effects, etc.) which has uniform nondirectionality in the horizontal plane. The breadboard used Balsa wood due to its good insulation qualities *and* very low thermal mass. In the field consideration should be given to prevention of water absorption. No thermal air velocity system will give correct data in rain or dense fog.

The current vs airspeed curve shows the typical decreasing sensitivity with increasing velocity, but a good calibration curve has not been obtained at this time through lack of instrumentation. Response speed is decidedly slower than that of thermocouple types, but in some cases this may be an advantage, such as in determining average airspeed on a gusty day.

**Position Sensing**

This may be the most novel or, on the other hand, strangest of the applications shown. Under certain conditions however, the very considerable position "integration" due to the thermal mass of the sensor may make this system quite practical, and much less expensive than electronic filtering. As shown in *Figures 12 and 13* the essence of the system is a small sliding *heater* acting as a position transmitter. The receiver is a brass tube which allows the total heater output to be transmitted out toward the ends. The temperature reached at each end is proportional to heater position.

Logically, with the heater in the center, both ends reach the same temperature. With the heater at one end, that end is about 50°C warmer than ambient, and

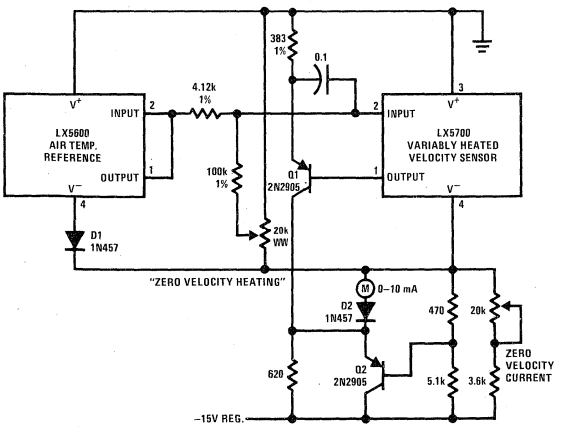



FIGURE 10. Air Velocity Meter

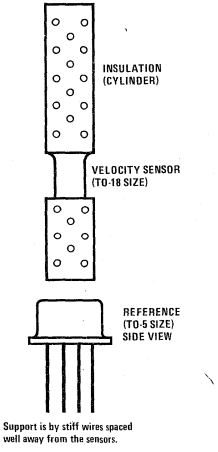



FIGURE 11. Sensor Arrangement

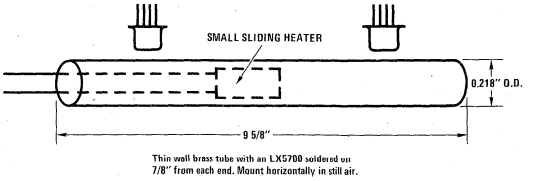



FIGURE 12. Position Sensor Tube

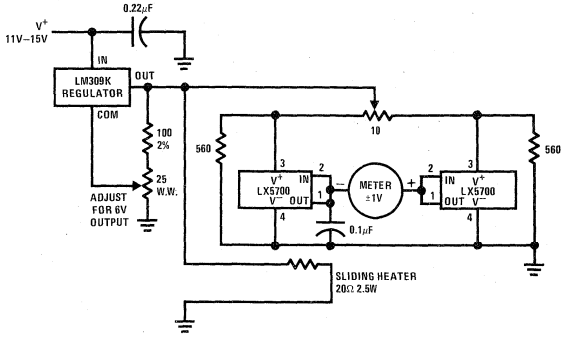



FIGURE 13. Position Sensor Schematic

the other end is near ambient. As the heater moves toward one end, one thermometer becomes more sensitive, and the other less. The differential effects tend to cancel, and the first breadboard unit had a temperature difference linearity within 4% relative to measured position. The heater must stay *between* the sensors to achieve this, with the extra length of tube at the ends helping to linearize the system.

The electrical system powers the sensors at minimum dissipation, and regulates heater power to keep position "gain" constant. The pot simply allows an electrical zero of the two thermometers and meter, which can be done with the heater off. The meter can be a 2 polarity DVM with 600 mV to 1V full scale, or a zero centered mechanical meter with similar deflection either side of zero.

The system takes 2 to 3 minutes to reach 98% of final reading. This may make it a very good position *averaging* system in cases where there is high amplitude vibration. Average truck spring deflection could be read while it is rolling along a rough road for instance. The system will have less wear problems than a sliding position pot and be less expensive than a Linear Variable Transformer system. It may also be useful in a position servo system that needs very heavy filtering.

## SUMMARY AND CONCLUSIONS

Since the monolithic temperature transducer is a relatively new and unique device, this has been primarily an applications paper attempting to broaden the base of practical Integrated Circuit usage. Some general techniques were explained and seven specific systems have been described in construction and performance. Hopefully these concepts will remain after the details are forgotten.

First, there are many considerably different schemes for temperature control or measurement based on the versatility of a transducer that has both amplifying and regulating capability in the same package. This three circuits in one package availability allows consideration of systems that formerly would have been too expensive or complex.

Secondly, the ease of accurately sensing small temperature *differences* leads to sensors for other than just temperature sensing. Sensing liquids, air velocity, and mechanical position have been demonstrated, and other possibilities include rate-of-rise sensors for fire detection, RMS regulators, and humidity gauges. It will be interesting to see what others turn up that we have missed.

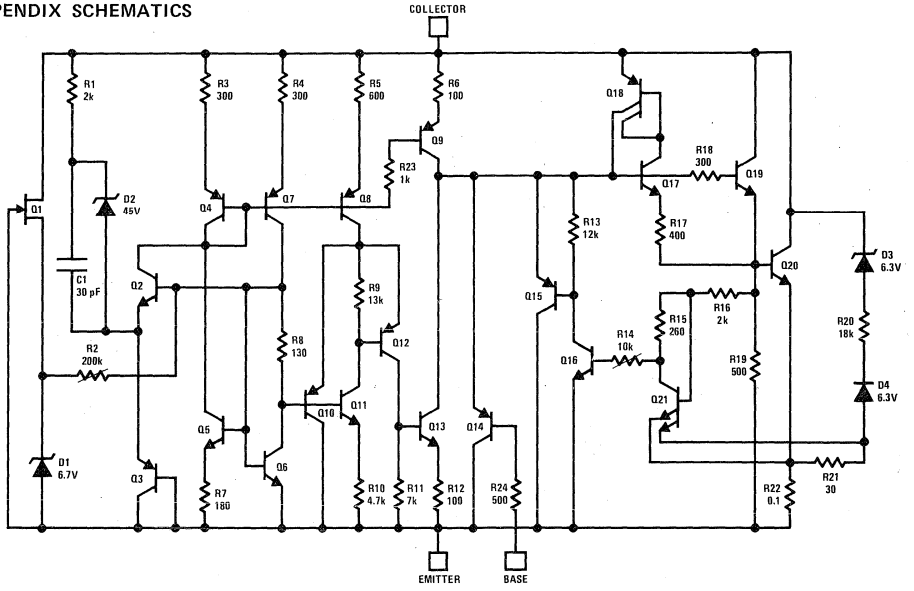
## REFERENCES

(1) Robert C. Dobkin, *1.2 Volt Reference,* National Semiconductor Corporation Application Note 56, December 1971.

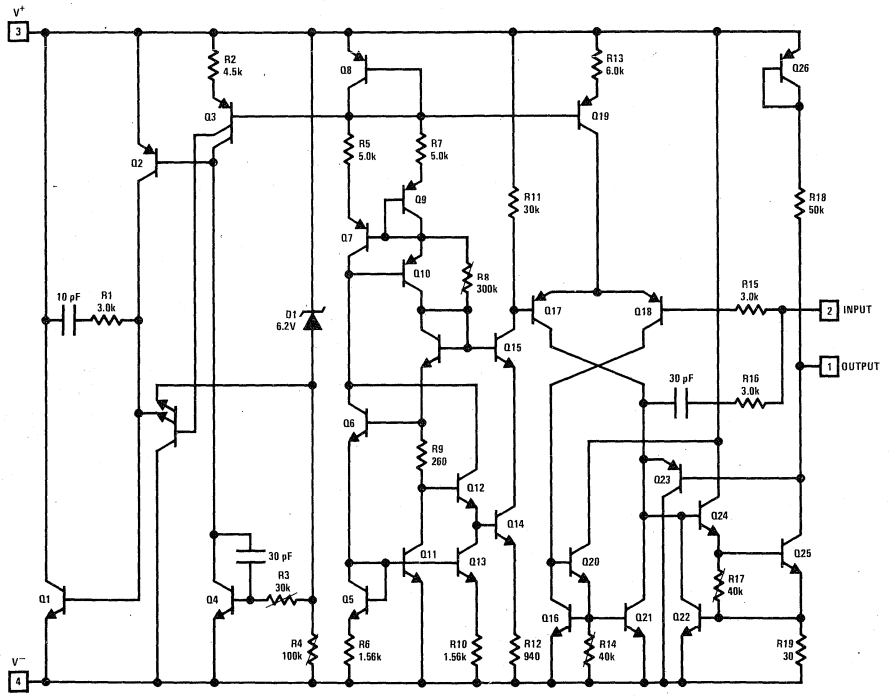
(2) Robert C. Dobkin, *Fast IC Power Transistor with Thermal Protection*, National Semiconductor Corporation Application Note 110, May 1974.

(3) *Transducers, Pressure & Temperature,* National Semiconductor Corporation catalog and handbook, August 1974.

## APPENDIX SCHEMATICS




Schematic Diagram of the LM195




Schematic Diagram of the LX5600/LX5700

Jim Sherwin
Nello Sevastopoulos
Tim Regan
JUNE 1975

# FM REMOTE SPEAKER SYSTEM

## INTRODUCTION

A high quality, noise free, wireless FM transmitter/receiver may be made using the LM566 VCO and LM565 PLL Detector. The LM566 VCO is used to convert the program material into FM format, which is then transformer coupled to standard power lines. At the receiver end the material is detected from the power lines and demodulated by the LM565.

The important difference between this carrier system and others is its excellent quality and freedom from noise. Whereas the ordinary wireless intercom uses an AM carrier and exhibits a poor signal-to-noise ratio (S/N), the system described here uses an FM carrier for inherent freedom from noise and a PLL detection system for additional noise rejection.

The complete system is suitable for high-quality transmission of speech or music, and will operate from any AC outlet anywhere on a one-acre homesite. Frequency response is 20-20,000 Hz and THD is under ½% for speech and music program material.

Transmission distance along a power line is at least adequate to include all outlets in and around a suburban home and yard. Whereas many carrier systems operate satisfactorily only when transmitter and receiver are plugged into the same side of the 120-240V power service line, this system operates equally well with the receiver on either side of the line.

The transmitter is plugged into the AC line at a radio or stereo system source. The signal for the transmitter is ideally taken from the MONITOR or TAPE OUT connectors provided on component system Hi-fi receivers. If these outputs are not available, the signal could be taken from the main or extra speaker terminals, although the remote volume would then be under control of the local gain control. The carrier system receiver need only be plugged into the AC line at the remote listening location. The design includes a 2.5W power amplifier to drive a speaker directly.

## TRANSMITTER

Two input terminals are provided so that both LEFT and RIGHT signals of a stereo set may be combined for mono transmission to a single remote speaker if desired.

The input signal level is adjustable by $R_1$ to prevent over-modulation of the carrier. Adding $C_2$ across each input resistor $R_7$ and $R_8$ improves the frequency response to 20 kHz as shown in *Figure 5.* Although casual listening does not demand such performance, it could be desired in some circumstances.

The VCO free-running frequency, or carrier frequency $f_c$, determined by $R_4$ and $C_4$ is set at 200 kHz which is high enough to be effectively coupled to the AC line. VCO sensitivity under the selected bias conditions with $V_s$ = 12V is about $\pm 0.66\ f_c/V$. For minimum distortion, the deviation should be limited to ±10%; thus maximum input at pin #5 of the VCO is ±0.15V peak. A reduction due to the summing network brings the required input to about 0.2V rms for ±10% modulation of $f_c$, based on nominal output levels from stereo receivers. Input potentiometer $R_1$ is provided to set the required level. The output at pin #3 of the LM566, being a frequency modulated square wave of approximately 6V pk-pk amplitude, is amplified by a single transistor $Q_1$ and coupled to the AC line via the tuned transformer $T_1$. Because $T_1$ is tuned to $f_c$, it appears as a high impedance collector load, so $Q_1$ need not have additional current limiting. The collector signal may be as much as 40-50V pk-pk. Coupling capacitor $C_8$ isolates the transformer from the line at 60 Hz.

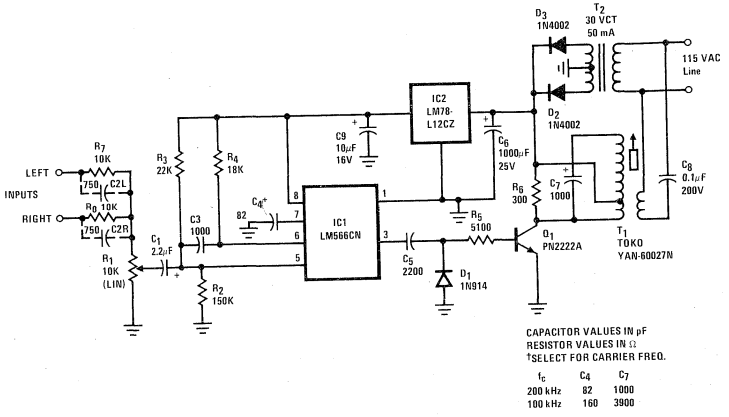



**FIGURE 1. Carrier System Transmitter**

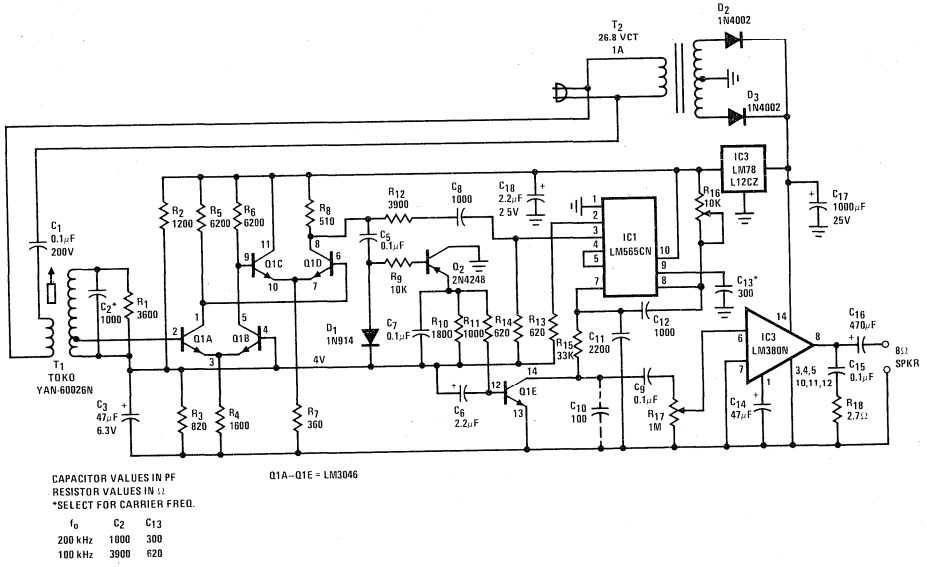



**FIGURE 2. Carrier System Receiver**

A voltage regulator provides necessary supply rejection for the PLL. The power transformer is sized for peak secondary voltage somewhat below the regulator breakdown voltage spec (35V) with a 125V line.

## RECEIVER

The receiver amplifies, limits, and demodulates the received FM signal in the presence of line transient interference sometimes as high as several hundred volts peak. In addition, it provides audio mute in the absence of carrier and 2.5W output to a speaker.

The carrier signal is capacitively coupled from the line to the tuned transformer $T_1$. Loaded Q of the secondary tank $T_1C_2$ is decreased by shunt resistor $R_1$ to enable acceptance of the ±10% modulated carrier, and to prevent excessive tank circuit ringing on noise spikes. The secondary of $T_1$ is tapped to match the base input impedance of $Q_{1A}$. Recovered carrier at the secondary of $T_1$ may be anywhere from 0.2 to 45V p-p; the base of $Q_{1A}$ may see pk-to-pk signal levels of from 12mV to 2.6V.

$Q_{1A}$-$Q_{1D}$ operates as a two-stage limiter amplifier whose output is a symmetrical square wave of about 7V pk-pk with rise and fall times of 100 ns.

The output of the limiting amplifier is applied directly to the mute peak detector, but is reduced to 1V pk-pk for driving the PLL detector.

The PLL detector operates as a narrow band tracking filter which tracks the input signal and provides a low-distortion demodulated audio output with high S/N. The oscillator within the PLL is set to free-run ot or near the carrier frequency of 200 kHz. The free-run frequency is $f_o \approx 1/(3.7\ R_{16}C_{13})$. Since the PLL will lock to a carrier near its free-run frequency, an adjustment of $R_{16}$ is not strictly necessary; $R_{16}$ could be fixed at 4700 or 5100Ω. Actually, the PLL with the indicated value of $C_{11}$ can lock on a carrier within about ±40 kHz of its center frequency. However, rejection of impulse noise in difficult circumstances can be maximized by carefully adjusting $f_o$ to the carrier frequency $f_c$. Adding $C_{10}$ = 100 pF will reduce the carrier level fed to the power amplifier. Even though the listener cannot hear the carrier, the audio amplifier could overload due to carrier signal power.

A mute circuit is included to quiet the receiver in the absence of a carrier. Otherwise, when the transmitter is turned OFF, an excessive noise level would result as the PLL attempts to lock on noise. The mute detector consists of a voltage doubling peak detector $D_1Q_2C_7$. The peak detector shunts the 1-2 mA bias away from $Q_{1E}$ without loading the limiter amplifier. When no carrier is present, the +4V line biases $Q_{1E}$ ON via $R_{10}$ and $R_{11}$; and the audio signal is shorted to ground. When a carrier is present, the 7V square wave from the limiter amplifier is peak detected, and the resultant negative output is integrated by $R_9C_7$, averaged by $R_{10}$ across $C_7$, and further integrated by $R_{11}C_6$. The resultant output of about −4V subtracts from the +4V bias supply, thus depriving $Q_{1E}$ of base current. Peak detector integration and averaging prevents noise spikes from deactivating the mute in the absence of a carrier when the limiter amplifier output is a series of narrow 7V spikes.

The LM380 supplies 2.5W of audio power to an 8 ohm load. Although this is adequate for casual listening in the kitchen or garage, for hi-fi listening, a larger amplifier may be desired.

## CONSTRUCTION

PC board layout and stuffing diagrams are shown in *Figures 3* & *4.* After the receiver board has been loaded and checked, the power transformer is mounted to the foil side of the board with a piece of fish-paper or electrical insulating cloth between board and transformer. Insulating washers of 1/16-1/4 inch thickness can be used to advantage in holding the transformer away from the foil. The board is laid out so that the volume control potentiometer may be mounted on either side of the board depending on the desired mounting to a panel.

The line coupling coils are available in production quantities from TOKO AMERICA INC, 5520 West Touhy, Skokie, IL.

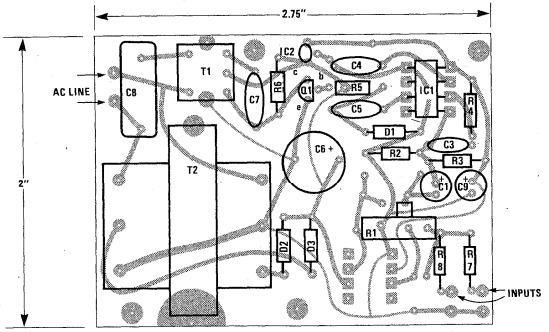



**FIGURE 3. Carrier System Transmitter PC Layout and Loading Diagram (Not Full Scale)**

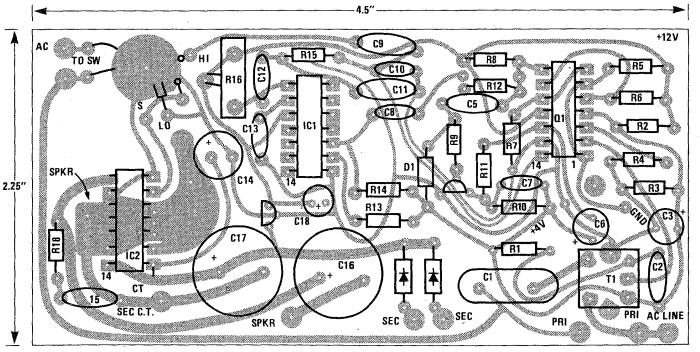



**FIGURE 4. Carrier System Receiver PC Layout and Loading Diagram (Not Full Scale)**

## ADJUSTMENT

Adjustments are few and extremely simple. Transmitter carrier frequency $f_c$ is fixed near 200 kHz by $R_4$ and $C_4$; the exact frequency is unimportant. $T_1$ for both transmitter and receiver are tuned for maximum coupling to and from the AC line. Plug in both receiver and transmitter; no carrier modulation is necessary. Insure that both units are operative. Observe or measure with an AC VTVM the waveform at $T_1$ secondary in the receiver. Tune $T_1$ of the transmitter for maximum observed signal amplitude. Then tune $T_1$ of the receiver for a further maximum. Repeat on the transmitter, then the receiver. Tuning is now complete for the line coupling transformers and should not have to be repeated for either. If the receiver is located some distance from the transmitter in use, or on the opposite side of the 110-220V service line, a re-adjustment of the receiver $T_1$ may be made to maximize rejection of SCR dimmer noise. The receiver PLL free-running frequency is adjusted by $R_{16}$. Set $R_{16}$ near the center of its range. Rotate slowly in either direction until the PLL loses lock (evidenced by a sharp increase in noise and a distorted output). Note the position and then repeat, rotating in the other direction. Note the new position and then center $R_{16}$ between the two noted positions. A fine adjustment may be made for minimum noise with an SCR dimmer in operation. The final adjustment is for modulation amplitude at the transmitter. Connect the audio signal to the transmitter input and adjust the input potentiometer $R_1$ for a signal maximum of about 0.1V rms at the input to the LM566. Adjustment is now complete for both transmitter and receiver and need not be repeated.

## A STEREO SYSTEM

If full stereo or the two rear channels of a quadraphonic system are to be transmitted, both transmitter and receiver must be duplicated with differing carriers. Omit $R_8$ and include $R_7$ & $C_2$ on the transmitter if desired. Carriers could be set to 100 and 200 kHz for the two channels. Actually, they need only be set a distance of 40 kHz apart.

## PERFORMANCE

Overall S/N is about 65 dB. Distortion is below about 1/4% at low frequencies, and in actual program material it should not exceed 1/2% as very little signal power occurs in music above about 1 kHz.

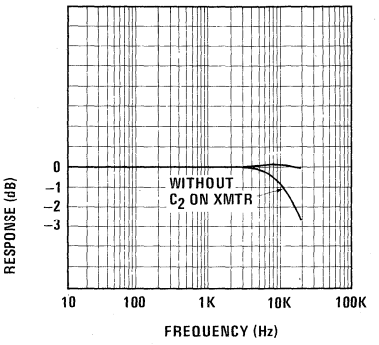



**FIGURE 5. Overall System Performance**
**Transmitter Input to Input of Receiver Power Amplifier**

The 2.5W audio amplifier provides an adequate sound level for casual listening. The LM380 has a fixed gain of 50. Therefore for a 2.5W max output, the input must be 89 mV. This is slightly less than the ±10% deviation level so we are within design requirements. Average program level would run a good 10 dB below this level at 28 mV input.

Noise rejection is more than adequate to suppress line noise due to fluorescent lamps and normal line transients. Appliance motors on the same side of the 110-220V line may produce some noise. Even SCR dimmers produce only a background of impulse noise depending upon the relative location of receiver and SCR. Otherwise, performance is noise-free anywhere in the home. Satisfactory operation was observed in a factory building so long as transmitter and receiver were connected to the same phase of the three-phase service line.

## APPLICATIONS

Additional applications other than home music systems are possible. Intercoms are one possibility, with a separate transmitter and receiver located at each station. A microphone can serve as the source material and the system can act as a monitor for a nursery room. Background music may be added to existing buildings without the expense of running new wiring.

Dennis Bohn
Jim Sherwin
JUNE 1975

# LOW COST IC STEREO RECEIVER

## INTRODUCTION

The recent availability of a broad line of truely high-performance consumer integrated circuits makes it possible to construct a high quality, low noise, low distortion and low cost AM/FM/Stereo receiver, Design emphasis is placed on a high level of performance, minimum factory adjustments and low parts count. As such, the receiver has immediate applications to table-top, high-fidelity, automotive and communications markets.

Provisions are included for the addition of a ceramic phono unit as well as a tapehead amplifier allowing inclusion of eight-track or cassette transport systems. Complete tone control circuitry is provided offering both boost and cut of Bass and Treble frequencies. Left and right channel Balance, and system Volume complete the manual front-panel controls.

Panel meters are employed in the FM system for both signal strength and center tuning, allowing for easy and accurate tuning. A directly driven LED offers immediate indication of FM stereo reception.

The complete design requires just five IC's, restricting the use of discrete active elements to the preassembled FM front-end and the single transistor tone control design.

## FM and FM STEREO

A preassembled front-end was selected as the cost-effective approach to minimum parts count and minimum factory adjustments. This model features an FET input stage providing excellent distortion performance. High selectivity is obtained thru the use of two cascaded ceramic filters yielding an approximate 6-pole response with less than 12 dB insertion loss.

The LM3089 FM IF System does all the major functions necessary for FM processing, including a three stage amplifier/limiter and balanced product detector, as well as an audio preamplifier. A single quadrature coil was used for ease of alignment; yielding recovered audio with THD less than 0.5%, however a double coil may be used to diminish THD to 0.1% if required. Carrier level detectors provide delayed AGC, SIGNAL strength meter drive, and adjustable interstation mute control $R_{11}$. The internal AFC amplifier was used to drive the TUNING meter, giving a visual indication of center tuning.

FM stereo demodulation is accomplished by the use of the LM1800 phase locked loop, thereby eliminating the need for external coils. Only two adjustments are necessary: $R_{14}$, which sets the 19 kHz oscillator, and $R_{17}$,

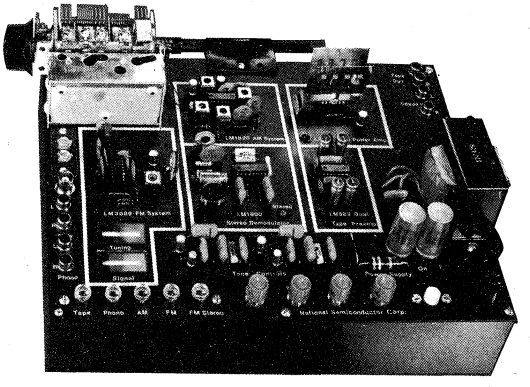



**FIGURE 1. IC Receiver**

which corrects for excess phase shift thru the IF stages, and yields maximum channel separation. Automatic stereo/monaural switching is built-in, and may be used in lieu of mechanical switching if desired. The open collector lamp driver is used to light a LED whenever a stereo station is encountered. (Further details available from application note AN-81.)

## AM

The AM function of the receiver is done completely with the LM1820 AM radio system. While designed for 3 section tuned superheterodyne applications, the LM1820 may be used with the less expensive 2 section tuned designs by omitting the RF stage and redefining its function as 2ND IF stage (see linear brief LB-29). As shown, the LM1820 provides the necessary converter/oscillator, IF, and AGC detector functions, while the external diode $D_1$ does the audio demodulation, $D_1$ is slightly forward biased thru $R_2$ for improved distortion performance. In addition its resistance is used in conjunction with $C_9$ to form the first stage of the required low pass filter; the second stage consists of $R_3$ and $C_{10}$.

## TAPE

The LM382 dual preamplifier was selected for its minimum parts count and low noise capability. With a guaranteed maximum equivalent input noise voltage of 1.2$\mu$Vrms (10 kHz BW), it easily amplifies the low level tape signals while retaining excellent S/N ratio (~64 dB below 2 mV input level). An ion-implanted resistor matrix is supplied on the chip for self-biasing the output to half-supply, and provides the resistors necessary to create the NAB equalization curve; requiring only four external capacitors per channel to complete the amplifier. For production models this preamplifier would normally be mounted directly on the tape player to minimize hum and noise pick-up.

## TONE CONTROLS

A single transistor tone control circuit was designed as the optimum cost/performance trade-off. The transistor is configured in a shunt-shunt feedback design, allowing gain variations between input functions. This is necessary to prevent sudden changes in output level when different inputs are selected. With a shunt feedback design the gain is easily controlled by choice of source impedance per *Figure 5*.

Approximately 20 dB of boost or cut of Bass and/or Treble frequencies is possible with the network shown. The turnover frequencies are approximately 500 Hz and 1600 Hz for bass and treble, respectively. The insertion loss of approximately 27 dB is made up by the gain of the transistor tone control amplifier. Balance and Volume controls are included as shown. Loudness control may be included by using a tapped Volume pot and the associated bass boost RC network if desired. More elaborate tone controls such as Baxandall feedback are possible, but at a premium in cost.

## POWER AMPLIFIER

The stereo power section, consisting of the LM378 dual audio amplifier, delivers 3W/channel with total harmonic distortion (THD) less than 1%, and 4W/channel with THD less than 10%, operating from split supply voltages of ±11V. Split supplies were chosen to facilitate a minimum parts count design. This approach allows direct coupling of the amplifier to the speakers since the output DC level is zero volts (offset voltage will be less than 25 mV), thereby eliminating the need of large coupling capacitors and their associated degradation of power, distortion and cost. Since the input bias voltages are zero volts, the need for bias resistors and the bias-pin supply bypassing capacitor are also eliminated. Input capacitors are omitted and bias current for the positive input is obtained directly thru the Volume pots since the tone control circuitry has been designed such that there is no DC potential applied.

It is important to apply proper supply voltages and adequate heatsinking in using the LM378 (see application note AN-125). Note that while the standby and low output power operating points of the power supply are ±15V, the maximum power out point causes the supply to sag to ±11V therefore reducing package power dissipation to acceptable levels. Socketable heatsinking is possible using a Staver V7-5 heatsink soldered directly to the center three pins on both sides of the LM378.

## POWER SUPPLY

The worst case ripple rejection of 45 dB for the IC's used allows for a simple unregulated power supple, however the discrete front-end and tone control amplifiers require some regulation to preserve the IC performance. A single zener diode $Z_1$ was selected to create a +12V supply for this function. The split supplies required for the power amplifier are derived from a conventional full-wave bridge rectifier operating off of the center-tapped secondary of the line transformer.

## REFERENCES


1. Isbell, T.D. and Mishler, D.S., *"LM1800 Phase Locked Loop FM Stereo Demodulator."* National Semiconductor Application Note AN-81, June 1973.

2. Papanicolaou, E.S. and Mortensen, H.H., *"Low-Cost AM-Radio System Using LM1820 And LM386."* National Semiconductor Linear Brief LB-29, May 1975.

3. Sherwin, J., *"LM377, LM378 And LM379 Dual Two, Four, And Six Watt Power Amplifiers."* National Semiconductor Application Note AN-125, January 1975.

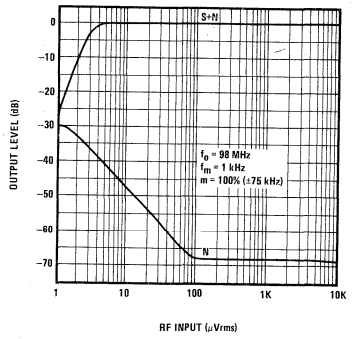



**FIGURE 2. FM Sensitivity**

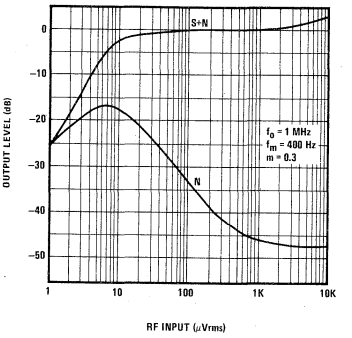



**FIGURE 3. AM Sensitivity**

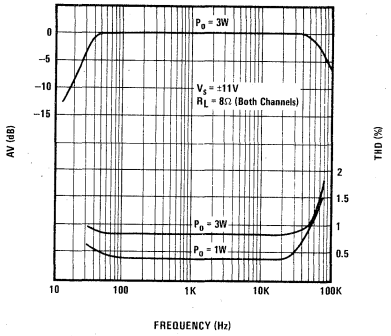



**FIGURE 4. Power Amplifier Frequency Response and Total Harmonic Distortion**

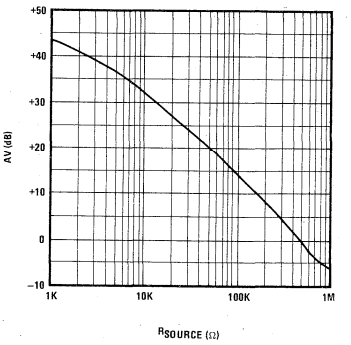



**FIGURE 5. $A_V$ vs. $R_{SOURCE}$ for Tone Control Preamplifier Stage.**

## SPECIFICATIONS

FM-MONO

Sensitivity: 2.5μV for 30 dB quieting
Harmonic Distortion: 0.3%
Hum & Noise: −65 dB
Frequency Response: 50-15 kHz ±3 dB

FM-STEREO

Channel Separation: 45 dB
Harmonic Distortion: 0.4%

AM

Sensitivity: 20μV for 20 dB S+N/N
Harmonic Distortion: 2%
Hum & Noise: −45 dB

TAPE

Frequency Response: NAB equalized ±2 dB
Harmonic Distortion: 0.3%
Hum & Noise: −64 dB below 2 mV input level

AMPLIFIER

Power Output: 3W RMS, per channel into 8 ohms at less than 1% THD from 40-30 kHz
Frequency Response: 35-55 kHz ±3 dB

VENDOR DEVICES

FM Tuner: Waller 32SN2F1-30
Coils: T3: AM Osc. Toko RWO-6A6255
T4: IF, 455 kHz Toko RRC-3A6426N
T5: IF, 455 kHz Toko RRC-3A6427A
T6: IF, 455 kHz Toko RZC-1A6425A
T7: Quadrature, 10.7 MHz - Toko TKXC-33733BS
Ceramic Filters: 10.7 MHz Toko CFS-30AE-10
Selector Switch: IEE/Schadow Type F-4U with FA201 Mech. Reflecting Indicators
Meters: TUNING: #11226, SIGNAL: #11222 Mercer Electronics
Heatsink: Staver V7-5

VENDOR LOCATIONS

Waller Corp., Crystal Lake, Ill. (815) 459-6510
Toko (America), Inc., New York, N.Y. (212) 736-0245
IEE/Schadow Corp., Eden Prairie, Minn. (612) 944-1820
Mercer Electronics (Simpson Electric Co.), Elgin, Ill. (312) 379-1130
Staver Co., Bay Shore, N.Y. (516) 666-8000

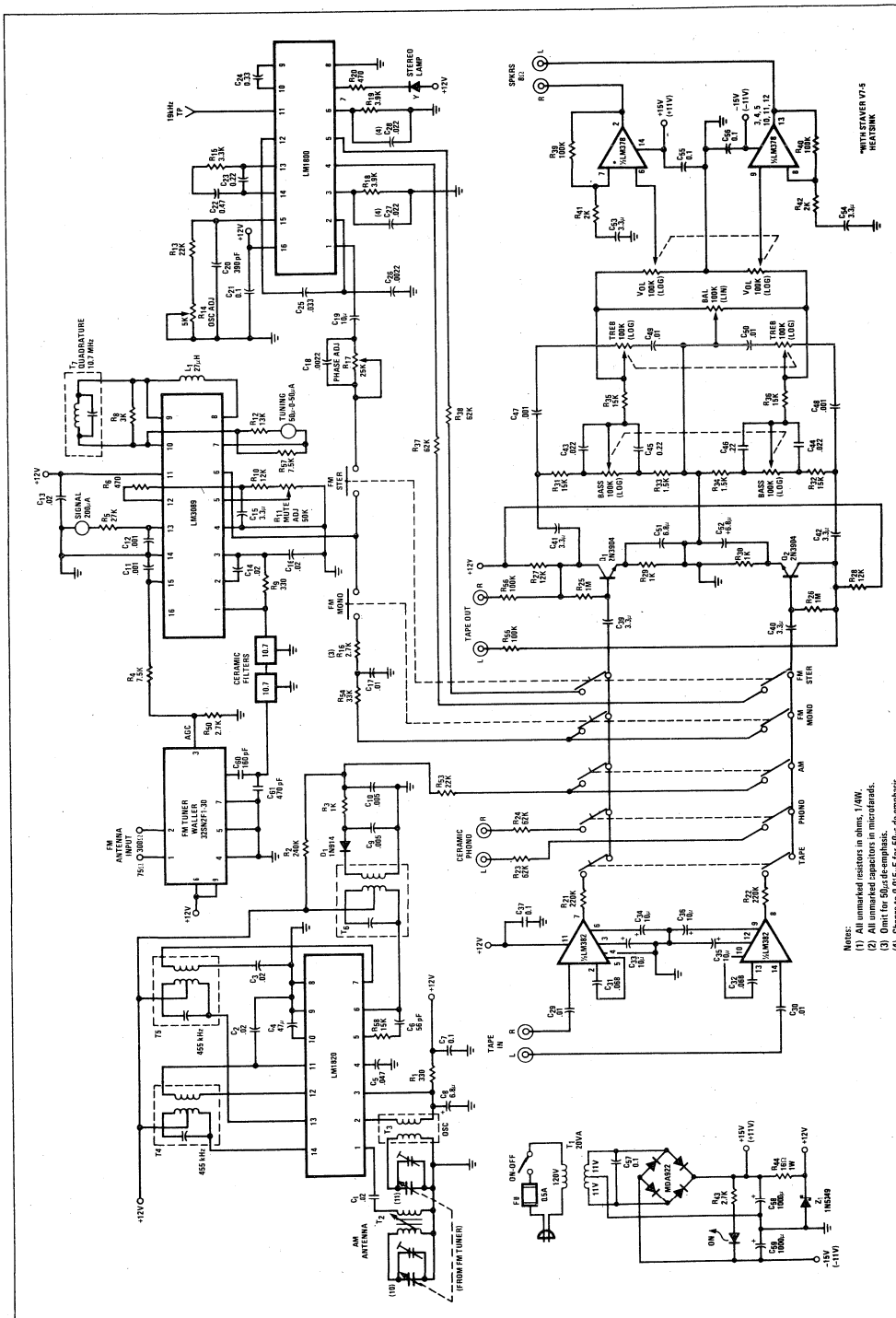



FIGURE 6. Complete Schematic

Notes:
(1) All unmarked resistors in ohms, 1/4W.
(2) All unmarked capacitors in microfarads.
(3) Omit for 50µs de-emphasis.
(4) Change to 0.01µF for 50µs de-emphasis.

John Maxwell
JANUARY 1976

# THE LOW NOISE JFET—THE NOISE PROBLEM SOLVER

The most versatile low noise active device available to the designer today is the Junction Field-Effect Transistor (JFET). JFETs are virtually free of the problems which have plagued bipolar transistors—limited bandwidth, popcorn noise, a complex design procedure to optimize noise performance. In addition, JFETs offer low distortion and very high dynamic range.

Most designers think of JFETs for very high source impedances. However, modern devices offer the designer performance improvements over bipolar transistors in NF for all but lowest impedance (<500Ω) sources and even then may provide improved performance if popcorn noise, bandwidth or circuit component noise is a consideration (see *Figure 1).*

Therefore, the purpose of this article is to review low noise design procedures and indicate the simplicity of designing high performance low noise amplifiers with low cost JFETs.

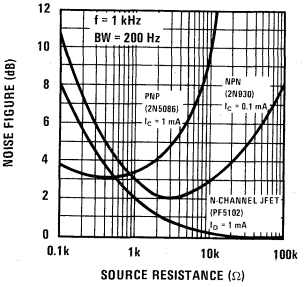
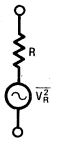



**FIGURE 1. Bipolar and JFET Transistor Noise Comparison**

## REVIEW OF BASICS

Before guidelines are established for designing low noise JFET amplifiers, a method of noise characterization must be chosen. Designers are confronted with a multitude of different noise parameters such as Noise Figure (NF), noise voltage and current densities, noise temperature, noise resistance, etc. Designers are primarily concerned with signal to noise (S/N) ratios preferring noise voltage, ($e_n$) and current ($i_n$) density.

Noise generally manifests itself in three forms: thermal noise, shot noise and flicker or "1/f" noise. Thermal noise arises from thermal agitation of electrons in a conductor and is given by Nyquist's relation:




$$\overline{V_R^2} = 4k\,T\,R\,\Delta f \qquad (1)$$

$\overline{V_R^2}$ = mean square noise voltage
k = Boltzmann constant ($1.38 \times 10^{-23}$ VAS/°K)
T = Absolute temperature (°K)
R = Resistance in ohms
Δf = Noise bandwidth (Hz)

The noise of a resistor may be represented as a spectral density ($V^2$/Hz) or more commonly in $\mu V/\sqrt{Hz}$ or $nV/\sqrt{Hz}$ and is given by:

$$e_{nR} = (\overline{V_R^2}/\Delta f)^{1/2} \qquad (2)$$

It is sometimes more convenient to represent thermal noise as noise current instead of a noise voltage. One needs only to consider the Norton equivalent yielding a noise current density.

$$i_{nR} = \frac{e_{nR}}{R} = \left(\frac{4\,kT}{R}\right)^{1/2} \qquad (3)$$

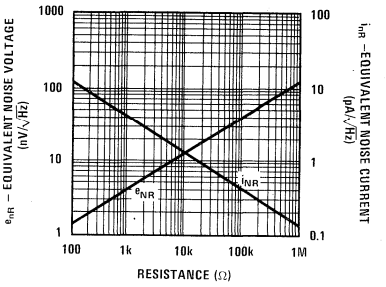



**FIGURE 2. Thermal Noise Voltage and Current Densities vs Resistance.**

The second basic form of noise, shot noise, is due to the randomness of current flow (discrete charge particles) in semiconductor P-N junctions.

$$\overline{i^2} = 2\,q\,I_{DC}\,\Delta f \qquad (4)$$

$\overline{i^2}$ = Mean square noise current
q = Charge of an electron ($1.6 \times 10^{-19}$ AS)
$I_{DC}$ = dc current flowing through the junction (A)
Δf = Noise bandwidth (Hz)

As with thermal noise, shot noise may be represented as a current density ($A^2$/Hz) or $pA/\sqrt{Hz}$.

$$i_n = (\overline{i^2}/\Delta f)^{1/2} \qquad (5)$$

It should be noted that both thermal noise and shot noise are "white" noise sources, i.e., frequency independent.

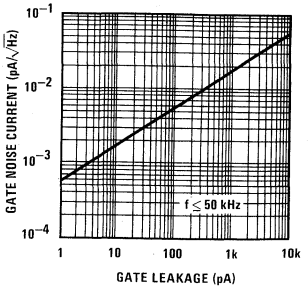



**FIGURE 3. Current Noise vs Gate Leakage Current**

The third basic noise source confronting designers is flicker or "1/f" noise whose density is roughly inversely proportional to frequency starting at about 1 kHz in both JFETs and bipolar transistors and increasing as frequency is decreased. Through careful processing, flicker noise in JFETs has been reduced to levels nearly insignificant to the designer. Flicker noise in JFETs is primarily a noise voltage and is source independent. Flicker noise in bipolar transistors is a function of base and leakage currents increasing with increased source impedance or operating currents.

A simple noise model of a JFET or any amplifying device may be constructed using a thermal and shot noise source which would adequately describe its noise performance allowing signal to noise ratios to be calculated directly.

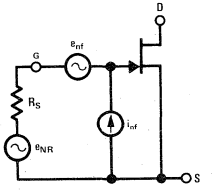



**FIGURE 4. Simple JFET Noise Model**

The input noise per unit bandwidth at some frequency may be calculated from the mean square sum of the noise sources (assuming the JFET noise sources are uncorrelated or independent of one another).

$$e_{nt}^2 = e_{nR}^2 + e_{nf}^2 + i_{nf}^2 R_s^2 \quad (6)$$

The total noise in the same bandwidth $\Delta f$, where the noise sources are independent of frequency, is simply:

$$V_{NOISE} = (e_{nt}^2 \Delta f)^{1/2} \quad (7)$$

Practically, noise sources are not frequency independent except resistor noise with no dc bias. The total input noise for the nonideal case may be calculated by breaking the spectrum up into several small bands and calculating the noise in each band where the noise sources are nearly frequency independent. The total input noise would then be the RMS sum of the noise in each of the bands N1 . . . Nn.

$$V_{NOISE} = (V_{N1}^2 + V_{N2}^2 + \ldots V_{Nn}^2)^{1/2} \quad (8)$$

## THE DESIGN PROCESS

The final circuit configuration and suitable JFET will be determined by the external circuit constraints.

1) Minimum signal to noise ratio (maximum amplifier noise)
2) Type and magnitude of source impedance (resistive or reactive)
3) Amplifier input impedance requirements
4) Bandwidth and maximum frequency of interest
5) Maximum operating temperature
6) Stage gain
7) Power supply voltage and current limitations
8) Circuit configuration, single or dual device

The design procedure is dependent on the type of source and each case must be considered separately. Resistive sources will be considered first because they are the least restrictive for the preamplifier.

### Resistive Sources

Preamplifiers for resistive sources are typically voltage amplifiers requiring a fixed input resistance and capacitance consistent with the maximum frequency of interest and source resistance. In most cases a resistor of the desired value connected between the gate and ground will satisfy the input resistance requirement leaving the maximum input capacitance as the major concern.

The maximum amplifier input capacitance is a function of the JFET source resistor, input resistance, source capacitance and maximum frequency. The maximum allowable input capacitance will be used in eliminating unsuitable JFET geometrics and optimizing the circuit configuration. Sometimes the JFET geometry (or type) with the lowest noise may also have an input capacitance that makes it unsuitable. The JFET input capacitance should be considered before noise in high source resistance, wideband amplifier designs.

$$C_{in} \cong C_{rs}\left(1 + \frac{gm\ R_D}{1 + gm\ R_s}\right) + \frac{C_{gs}^*}{1 + gm\ R_s} \quad (9)$$

$^*C_{gs} = C_{is} - C_{rs}$

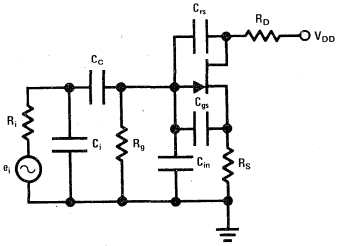



**FIGURE 5. A Typical Resistive Source JFET Amplifier**

If low input capacitance is required, a cascode configuration minimizes input capacitance and still allows high gain within a device type. The cascode configuration can also be used to reduce the voltage across a device, reducing device heating (for high current operation) and gate leakage currents when source impedances are very high.

Once the basic circuit configuration has been decided upon or dictated by gain, bandwidth and power supply limitations, the final JFET selection will be on noise. Redrawing the amplifier in *Figure 4* with all of the noise sources, the total amplifier noise per unit bandwidth can be found.

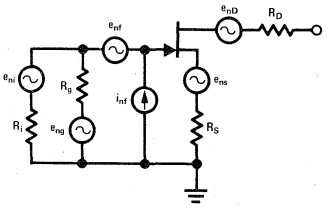



**FIGURE 6. A Typical Resistive Source JFET Amplifier with Noise Sources**

$$e_{nt} = \left[ e_{nig}^2 + e_{nf}^2 + e_{ns}^2 + \frac{e_{nD}^2}{A_V^2} + i_n^2 \ (R_i // R_g)^2 \right]^{1/2} \quad (10)$$

where: $e_{nig}^2$ = The noise of the parallel connection of $R_i$ and $R_g$

$e_{nf}^2$ = The noise voltage of the JFET

$e_{ns}^2$ = The noise of the source resister $R_s$

$\frac{e_{nD}^2}{A_V^2}$ = The noise at the drain (thermal noise of the load plus the second stage noise)

$i_n^2 (R_i // R_g)^2$ = The current noise contribution of the JFET

When the amplifier is operated at room temperature and moderate drain voltages, the current noise term is usually negligible with source resistances as high as 10 MΩ. Depending on the voltage gain of the stage, the drain circuit noise may be negligible, simplifying the input noise expression.

$$e_{nt} = (e_{nig}^2 + e_{nf}^2 + e_{ns}^2)^{1/2} \quad (11)$$

The final JFET selection will be based on the noise requirements from the maximum allowable noise $V_{MAX}$.

$$V_{MAX} = (e_{nf}^2 + e_{ns}^2)^{1/2} \quad (12)$$

Depending on $V_{MAX}$ and $e_{nf}^2$ the source resistor may have to be bypassed to ground to eliminate noise of the bias resistor.

### Capacitive Sources

Preamplifiers for capacitive sources are primarily current amplifiers requiring very high input resistance and controlled input capacitance to match the source capacitance.

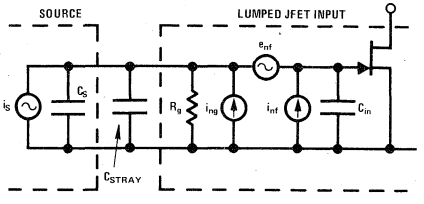



**FIGURE 7. JFET Preamplifier with a Capacitive Source**

The source capacitance should equal the sum of the preamplifier input capacitance and the stray capacitance for maximum frequency response and power transfer from the signal source. Assuming the gate resistor, $R_g$, is so large as to not load the capacitive source, the input noise voltage is:

$$e_{nt} \cong \left[ e_{nf}^2 + (i_{nf}^2 + i^2_{ng}) \left( \frac{R_g^2}{(1 + \omega^2 R_g^2 C^2)} \right) \right]^{1/2} \quad (13)$$

where $C = C_S + C_{in}$

with an input signal of

$$e_s \cong i_s \left( \frac{R_g^2}{1 + \omega^2 R_g^2 C^2} \right)^{1/2} \quad (14)$$

When the source and input capacitance are matched, the final JFET geometry will be selected on two criteria: the noise voltage, $e_n$, and the current noise from the gate leakage, $I_{G(ON)}$, to optimize the signal to noise ratio. As in the resistive source case, the circuit configuration and JFET selection is an iterative process using all of the external circuit constraints and device parameters and limitations.

### Inductive Sources

Amplifiers designed for inductive sources (including transformers) require fixed input resistances (as in the resistive source case) and controlled input capacitance (as in the capacitive source case). The input noise per unit bandwidth will rise with increasing frequency to a maximum value at resonance of the inductive source and the input capacitance or when the shunt resistance of the inductor is larger than the input resistance of the amplifier.

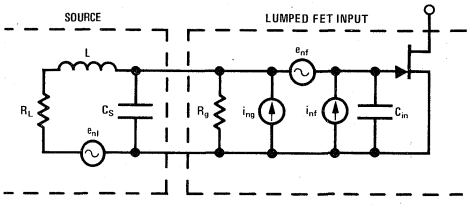



**FIGURE 8. JFET Amplifier with an Inductive Source**

The inductive source amplifier is the most difficult to analyze due to the complex input impedance. The input noise per unit bandwidth is given by:

$$e_{nt}^2 = e_{nf}^2 + (i_{nf}^2)(|Z_{in}|^2) + 4\,kT\,(Re\,(Z_{in})) \quad (15)$$

where $Z = X_{CIN} // R_g$

and $Z_{in} = Z // (Z_L + R_L)$

Usually the current noise of the JFET is negligible, simplifying the expression a little, but not much. The optimization process for inductive sources is very complex and it will require the spectrum to be broken up into several small bands to arrive at a final design. Generally, a JFET with a minimum noise voltage will be the proper choice.

Transformers may be used with JFET amplifiers to minimize noise with very low source impedances. Transformers have both drawbacks and advantages and both must be examined before a transformer design is chosen. Poor frequency response, susceptibility to mechanical and magnetic pickup and thermal noise head the list of disadvantages to be weighed against two very important advantages. First, the noise voltage is transformed by the turns ratio N; second, the resistance is transformed by $N^2$. These can be used to advantage by matching very low values of source resistance to a relatively noisy amplifier and still maintaining a good signal to noise ratio, i.e., the total noise at the source assuming an ideal transformer is

$$e_{nt}^2 = e_{nRs}^2 + \frac{e_{nAmp}^2}{N^2} \qquad (16)$$

## SUMMARY

Low noise amplifier design concepts have been introduced for the three basic types of sources. Basic parameters ($C_{in}$, $e_n$, gm) were discussed that affect both circuit configuration and JFET type. There is no universal low noise JFET or circuit configuration that solves all problems. Each low noise amplifier design is different and must be considered within its own framework of performance requirements.

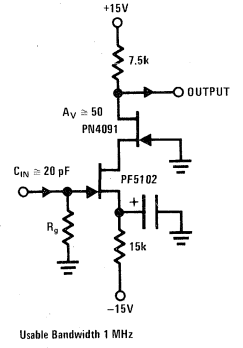
## REFERENCES


A. Van der Ziel, "Noise," Prentice-Hall, 1954.

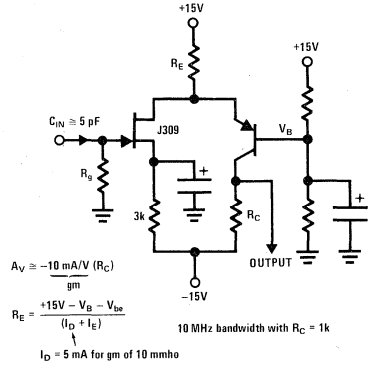
Richard S.C. Cobbold, "Theory and Applications of Field-Effect Transistors," John Wiley & Sons, 1970.

C.D. Motchenbacher and F.C. Fitchen, "Low Noise Electronic Design," John Wiley & Sons, 1973.


## SOME PRACTICAL LOW NOISE JFET INPUT CIRCUITS




a) Wide Band, Low Input Capacitance, Very Low Noise Preamplifier




b) Low Noise, Very Low Input Capacitance Video Amplifier

## APPENDIX A

### Important National JFET Process Parameter Guide

Test Conditions $V_{DS}$ = 15V, $I_D$ = 1 mA ($V_{GS}$ = 0V)*

| PROCESS | $e_n$ @ 10 Hz (nV/$\sqrt{Hz}$) | $e_n$ @ 1 kHz (nV/$\sqrt{Hz}$) | $e_n$ @ 100 kHz (nV/$\sqrt{Hz}$) | $g_{fs}$ (mmho) | $I_{G(ON)}$ (pA) | $C_{GD}$ (pF) | $C_{GS}$ (pF) |
|---|---|---|---|---|---|---|---|
| 50 | 15 | 5 | 2.5 | 3 | 5V 2 pA<br>10V 10 pA<br>15V 1 nA | 0.7 | 2.5 |
| 51 | 5 | 3 | 1.3 | 7 | 30 | 3 | 9 |
| 55 | 10 | 4 | 2.5 | 2.4 | 5 | 2 | 4 |
| 92 | 10 | 4 | 1.5 | 4.5 | 10V 20 pA<br>15V 1 nA | 2 | 4 |
| 83 | 10 | 5 | 2.5 | 2 | 5 | 1 | 2.5 |
| 84* | 50 | 15 | 9 | 0.2 | 0.1 | 0.01 | 2 |
| 94 | 10 | 5 | 2.5 | 2 | 1–2 | 0.01 | 4 |
| 95 | 10 | 4 | 2.5 | 1.5 | 15 | 3.5 | 15 |
| 96 | 5 | 3 | 1.3 | 7 | 30 | 3 | 9 |
| 93 | 15 | 7 | 2 | 3.5 | 10V 20 pA<br>15V 1 nA | 1 | 3.2 |

### National JFET Process Low Noise Amplifier Guide

| PROCESS | 50 | 51 | 55 | 92 | 83 | 84 | 93 | 94 | 95 | 96 |
|---|---|---|---|---|---|---|---|---|---|---|
| Low Noise Application | Single JFET | | | | Dual JFET | | | | | |
| Resistive Ultra-Low $e_n < 5$ nV/$\sqrt{Hz}$ @ 10 Hz | | X | | | | | | | | X |
| Resistive Low Freq < 20 kHz | | X | X | | X | | | X | X | X |
| Resistive Wideband < 10 MHz | X | X | | X | X | | X | X | X | X |
| Resistive Wide Band > 10 MHz | X | | | X | | | X | | | |
| Resistive Very High $R_S > 10$ MΩ | X | | | | | X | | X | | |
| Capacitive Low C < 10 pF | X | | X | X | X | X | X | X | | |
| Capacitive High C > 20 pF | | X | X | | | | | | X | X |
| Inductive | X | X | X | X | X | X | X | X | X | X |

## APPENDIX B

## NOISE PARAMETER CONVERSION

### Noise Figure (NF) to an Effective $e_n$

It is more convenient to present noise data for bipolar transistors in the form of contours of constant noise figure at a fixed frequency or plots of noise figure versus frequency at a fixed source resistance due to large values of noise current ($i_n$). Noise figure must be converted to an effective noise voltage ($e_{nE}$) for comparisions to be made between a BJT and a JFET or for signal to raise ratio calculations.

By definition:

$$NF = 10 \log \frac{\text{Total Output Noise Power}}{\text{Output Noise Power of the Source}} \quad \text{(B1)}$$

From equations 1 and 2, one finds the source noise power to be

$$\text{Source Noise Power} = \frac{e_{nR}^2 \, \Delta f}{R_S} \quad \text{(B2)}$$

for some source resistance $R_S$.

Referring to *Figure 4*, the total output noise power at the input of the amplifier would be:

$$\text{Total Output Noise Power} = \frac{e_{nR}^2 \, \Delta f}{R_S} + \frac{e_{nf}^2 \, \Delta f}{R_S} + i_{nf}^2 \, R_S^2 \, \Delta f \quad \text{(B3)}$$

The noise figure (NF) can now be expressed in terms of the noise source generators, $e_{nR}$, $e_{nf}$ and $i_{nf}$ allowing an expression to convert noise figure (NF) to an effective noise voltage ($e_{nE}$).

$$NF = 10 \log \left(1 + \frac{e_{nf}^2 + i_{nf}^2 \, R_S^2}{e_{nR}^2}\right) \quad \text{(B4)}$$

yielding

$$e_{nf}^2 + i_{nf}^2 \, R_S^2 = e_{nE}^2 = (10^{NF/10} - 1) \, e_{nR}^2 \quad \text{(B5)}$$

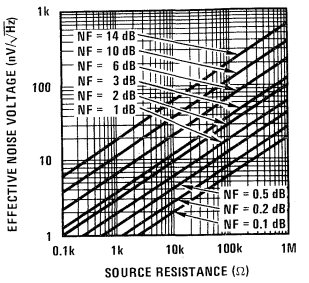



**FIGURE B1. Effective Noise Voltage ($e_{nE}$) vs Noise Figure and Source Resistance ($R_S$)**

### Noise Resistance

The effective noise voltage density ($e_n$) and noise current density ($i_n$) are found directly by referring to *Figure 1*, and reading the values for the corresponding resistances.

$$e_{nR} = (4 \, KTR)^{1/2} \quad (1)$$

$$i_{nR} = \left(\frac{4 \, KT}{R}\right)^{1/2} \quad (3)$$

## APPENDIX C

### JFET Current Noise

At low frequencies the current noise and voltage noise sources are uncorrelated in JFETs with the current noise being pure shot noise due to gate leakage currents. As frequency is increased, the current noise also increases starting at frequencies as low as 50 kHz in some high capacitance device types.

It has been suggested and experimentally verified that the noise current at high frequencies is due to increased gate input conductance.

$$i_n^2 = 4 \, KT\left[\text{Re}\,(Y_{11})\right]^{-1} \quad \text{(C1)}$$

Re ($Y_{11}$) is available on high frequency JFET data sheet as the real portion of the common source input admittance parameters. In effect the channel noise is coupling to the gate circuit through the source-gate and drain gate capacitances. Hence low capacitance devices exhibit lower values of noise current at high frequencies than do high capacitance devices.

Peter Lefferts
OCTOBER 1975

# CONSTANT CURRENT LED

## INTRODUCTION

The NSL4944 is a simple two-lead device normally used as an AC or DC indicator, yet can also be used as a rectifier and constant current source at the same time in associated circuitry. A number of such applications will be illustrated. Further, most of the regulating circuitry is not in series with the LED. This allows the complete regulated LED to operate at only about 300 mV more than a standard red LED. Thus the NSL4944 operates on half the voltage needed by previously available regulated or resistor LEDs. The device is rated for a maximum of 18 V forward and reverse.

These characteristics provide several advantages. Unloaded TTL gates provide enough voltage, in either high or low states, to directly drive the universal indicator. Size and weight can be saved in instruments with a number of indicator lights by reducing the size of filter capacitors or voltage regulators. The NSL4944 can operate on unfiltered DC or at somewhat reduced intensity on 3 to 12 VAC rms. Since the IC within the regulated LED blocks reverse voltage, the device can be used as a low voltage rectifier or polarity indicator.

## DESIGN FEATURES

The LED and its current source, as illustrated in Figure 1, both fit within a standard LED package. The typical operating voltages shown allow the device to operate with lower supplies and take up less room than an LED and component dropping resistor.

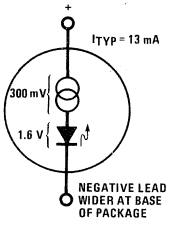



**FIGURE 1. Equivalent Circuit**

Figure 2 shows how some of the operating features of the NSL4944 are achieved. The rectifying characteristic occurs because the only input to the device passes through the IC's PNP emitters. These have a high reverse voltage in standard linear processing. The voltage reference and comparison amplifier operate from the same low voltage that the LED does. The big PNP transistor which passes both $I_{LED}$ and $I_{REF}$ can be operated almost in saturation since the comparison amplifier can pull the PNP base down to only one volt from common.

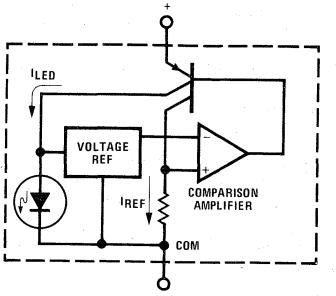



**FIGURE 2. Simplified Schematic**

## INDICATOR POWERING

The following figures contain some of the innumerable ways of providing power to the NSL4944.

Power and parts count is minimized by powering the indicator from a low voltage transformer winding as shown in Figure 3. This method, however, provides only

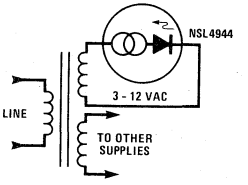



**FIGURE 3. AC Power**

half intensity light, but the apparent visual decrease is not as great. Some flicker occurs if the observer moves his head rapidly. The supply of Figure 4 will provide up to 87% of maximum light output. The bulk of a filter capacitor is still not needed, and at 12 VAC in, flicker will be almost imperceptible since the LED "off" periods will be less than a millisecond. In both situations, the indicator may be switched a number of ways, including bipolar transistors, since only DC can pass through the indicator.

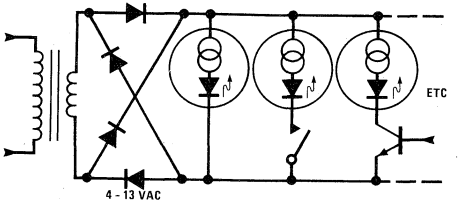



**FIGURE 4. Unfiltered DC Power**

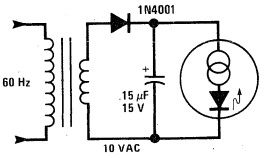



FIGURE 5. Minimizing DC Filtering

As shown in Figure 5, full intensity and zero possible flicker are achieved by minimal DC filtering. The small capacitor shown operates with 10 V p-p ripple and only about 8 V average DC, while the constant current drain characteristics of the NSL4944 allow only a few percent change in light intensity. If a system or instrument with a regulated supply has a number of LED indicators, regulator size and dissipation can be minimized by powering the regulated LEDs from the unregulated voltage.

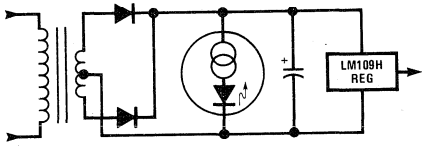



FIGURE 6. Unregulated DC

## LOGIC APPLICATIONS

The low operating voltage and constant current characteristics make the regulated LED an ideal status indicator for digital circuitry. An interesting fact to keep in mind is that full regulator current is not needed to light the LED. If, for example, only 8 mA is available (from a voltage of 1.6 to 1.9 V) the LED will light at a somewhat reduced intensity. The regulator will be switched full on instead of current limiting . . . but in such a situation it doesn't matter.

Any circuit capable of supplying 10 to 20 mA and a voltage swing of at least 1 V can switch the NSL4944 from an off to an on state. Within 25°C of room temperature, an input voltage of 1.3 V will produce little or no light, and 2.3 V will produce 70% to 90% of full output. However, with a small signal change, the pre-existing biases must be correct. The output swing of a TTL stage goes much closer to ground than to the 5 V supply. Therefore, Figure 7-C requires a 3.5 V supply for the indicators to have complete on-off switching.

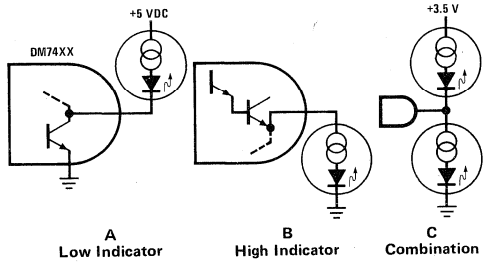



FIGURE 7. TTL Indicators

## CIRCUIT APPLICATIONS

In many circuits or small instruments the need for a constant current source or current limiter arises. FETs can generally only be used as low current sources, so for 10 mA or more, construction of a current source requires 3, 4, or more parts. If an indicator or pilot light is also needed, the regulated LED may be a very economical source of the needed constant current.

The examples below illustrate all three characteristics of the NSL4944. It is a combined rectifier, constant current source, and pilot light.

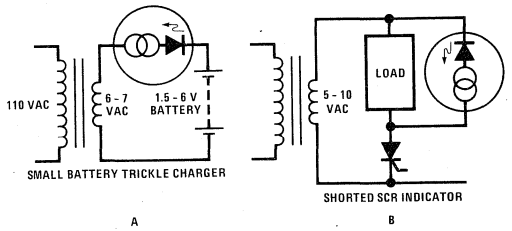



FIGURE 8.

Constant currents have a number of circuit or equipment design uses. Some of these have been combined for illustration in Figure 9. A number of LEDs can "share" a single constant current LED. Further, any of the ordinary LEDs can be turned on and off by a shunting switch without affecting operation of any of the others.

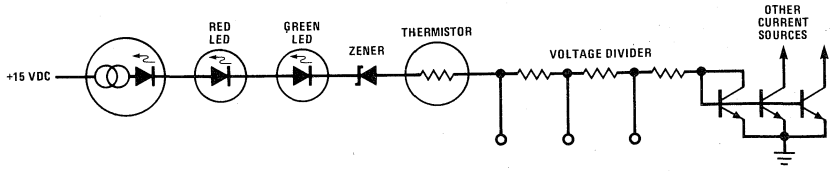



FIGURE 9. Uses for Constant Current

In equipment with unregulated supplies, or supplies having some unfiltered ripple, the 20,000 Ω impedance of the NSL4944 current source will be helpful. Supply ripple and variation passed on to Zener diodes, thermistors, and low value voltage divider bias sources will be greatly reduced. The sensitivity of low value thermistors to temperature changes will be increased. If practical, the regulated LED should be put in the same, or similar temperature environment as the thermistor used for temperature measurement. Otherwise a 20 to 40 degree temperature change at the LED would lead to an apparent one degree change sensed at the thermistor. Multiple current sources find use in some audio amplifier designs, and in power op-amp modules.

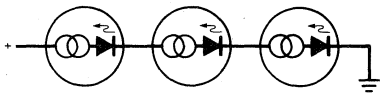


**FIGURE 10. Series NSL4944s**

There are some characteristics of seriesed regulated LEDs, and current sources in general, that should be kept in mind. All the LEDs will light properly, and the string will run at the current of the least current source. This lowest value source will absorb most of the supply voltage, with the other LEDs having only the starting voltage of about 2 V across them. Thus the maximum forward voltage increases only slightly as more devices are added. In the example above it would be 22 V. However, due to non-linear reverse current characteristics, maximum reverse voltages can be added.

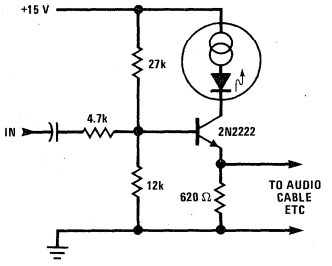



**FIGURE 11. Current Limiting and Short Protection**

A current source can also be a current limiter. Figure 11 shows an NSL4944 put in the collector of an emitter follower such as might be used in a pre-amp or mike mixer cable driver.

Normally voltage across the LED is only 2 V, allowing almost full supply-to-supply swing of the emitter follower output. In comparison a limiting resistor would either greatly increase output impedance, or severely limit output swing. However, if the output cable is accidentally shorted, only a little more than the rated current of the LED will flow. Output transistor dissipation actually decreases under emitter short conditions.

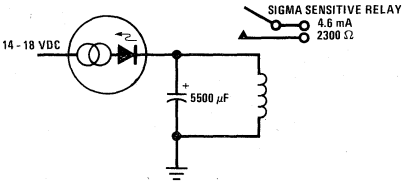



**FIGURE 12. Six Second Time Delay**

Logically, a constant current source is helpful in designing time delay circuits. If the circuit of Figure 12 were built with a resistor, the timing period would only be half the amount shown, and timing would vary over 50% with the supply variations shown.

Instead, the current regulated LED is still drawing within 10% of full current when the relay reaches its 11 V pull-in voltage. The 14 to 18 V supply variation will produce only about a 3% timing variation, a considerable improvement. Variations due to temperature and electrolytic capacitor tolerances will remain, however.

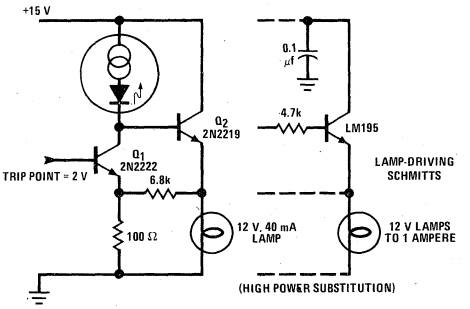



**FIGURE 13. Use as Active Load**

The lamp-driver Schmitt of Figure 13 illustrates a still further use of the NSL4944's constant current source. Substituting a current source for the collector resistor increases the useful voltage gain of $Q_1$. Further, almost full base current remains available to $Q_2$, even when supplying 12 V output, which would not be possible using a resistor. When the lamp and $Q_2$ are off, most of the LED current flows in the 100 Ω resistor, thus determining the circuit's switching or trip point of 2 V.

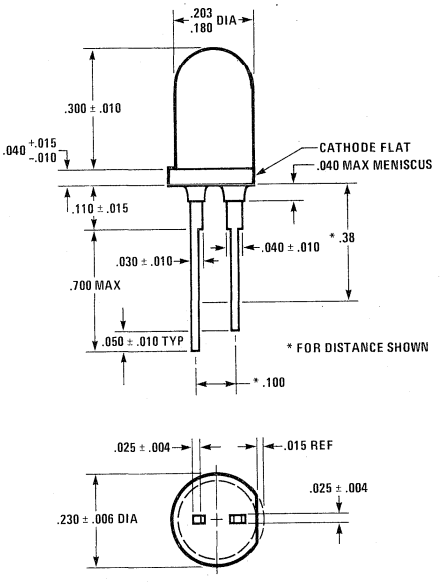
With $Q_1$ saturated, $Q_2$ still provides a volt to the bulb, contributing some preheating and reducing the bulb's starting current surge. On, $Q_2$ provides the bulb with 12 V due to the minimum voltage drop in the constant current LED. The 6.8k feedback resistor sets hysteresis at a measured 50 mV at the input. This can be varied without having to change the rest of the circuit. 10k provides almost "0" hysteresis (undesirable and unstable) while 2k sets a hysteresis of 0.5 V.

## CONCLUSION

A number of applications have been examined for a highly improved two-lead LED/IC. Its indicating capabilities, high reverse voltage, and wide constant current range may make it the most useful of the two-lead, hence simple to use, IC devices. To begin with, it can be lit from AC, unfiltered DC, and very poorly filtered or regulated DC with a savings in parts or size.

The NSL4944 may be driven from the 1 to 1.5 V swing of TTL circuitry, to the 15 to 18 V swing of Linear and MOS circuits. Its rectifying capabilities allow it to act as a small battery charger or reverse voltage monitor for power supplies, batteries, or low voltage SCRs. For all these, and the following functions, the LED "on" indication is in addition to the constant current circuit function performed. The device's constant current can power other LEDs, Zeners, thermistors, or other current or voltage sources. It has been shown that the current regulated LED can be a current limiter, a timing element, or an active load while simplifying and improving circuit performance.

## PHYSICAL DIMENSIONS




NOTE:

1. ±.015 TOLERANCE ON ALL DIMENSIONS UNLESS OTHERWISE SPECIFIED.

Peter Lefferts
DECEMBER 1975

# 1.3 VOLT I.C. FLASHER, OSCILLATOR, TRIGGER, OR ALARM

## INTRODUCTION

Most linear integrated circuits are designed to operate with power supplies of 4.5 to 40 V. Practically no battery/portable equipment is provided with indicator lights due to unacceptable power drain. Even LEDs (solid state lamps) won't light from a 1.5 V battery, and drain the common 9 V radio battery in a few hours.

The LM3909 changes all this. Obtaining long life from a single 1.5 V cell, it opens a whole new area of applications for linear integrated circuits. Sufficient voltage for flashing a light emitting diode is generated with cell voltage down to 1.1 V. In such low duty cycle applications batteries will last for months to years of continuous operation. Such flasher circuits then become practical for marking location of flashlights, emergency equipment, and boat mooring floats in the dark.

The LM3909 is simple in design, easy to use, and includes extra resistors to minimize external circuitry and the size of the completed flasher or oscillator.

## CIRCUIT OPERATION

The circuit below in figure A is the LM3909 connected as the simplest type of oscillator. Ignoring the capacitor for a moment, and assuming 1.5 V on pin 5, current will flow in the 3k and 6k timing resistors through the emitter of $Q_1$. This current will be amplified by about 3 by $Q_2$ and passed to the base of $Q_3$. $Q_3$ will then conduct, pulling down on the base of $Q_4$ and hence the base of $Q_1$. This is a negative feedback since it will reduce timing resistor current and current to the power transistor's base until a balance is reached. This will occur with the collector of $Q_3$ at about 0.5 V, the base of $Q_4$ at about 1 V, and a very small voltage from pin 8 to ground. The difference between these two voltages is the base-emitter drop of $Q_1$ and 2/3 the base-emitter drop of $Q_4$ as set by the high resistance divider from its base to emitter.

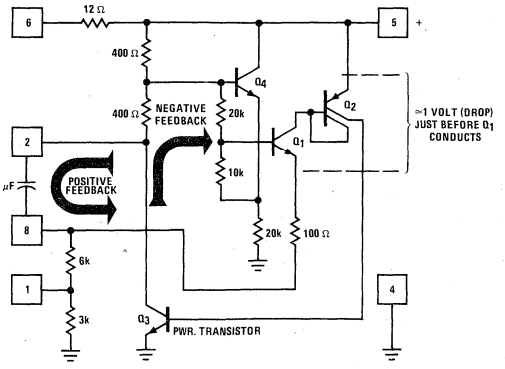



FIGURE A.

Note that negative feedback *voltage* is attenuated by at least 2 due to the divider of two 400 Ω resistors. Now considering the capacitor, its positive feedback is initially unity. Therefore the DC bias condition and the temporary excess positive feedback conditions are met and the circuit must oscillate.

The waveform at pin 8 of the above oscillator is shown below. The waveform at pin 2, the power transistor collector, is almost a rectangle. It extends from a saturation voltage of 0.1 V or less to within about 0.1 V of the supply voltage. The "on" period of course coincides with the negative pulses at pin 8. Other circuit voltages can easily be inferred from these two waveforms.

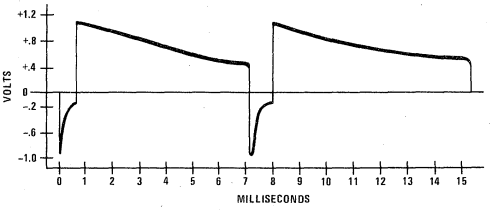



FIGURE B.

The simplicity of LED and incandescent pilot lamp flashers is illustrated below. In the LED flasher, the LM3909 uses the single capacitor for both timing and voltage boosting.

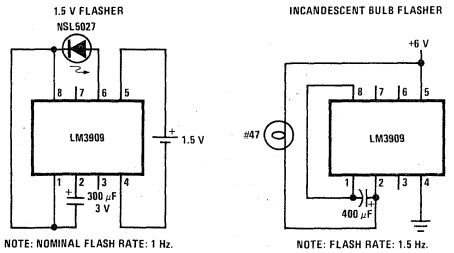



FIGURE 1. Two Simple Flashers

The LM3909, although designed as a LED flasher, is ideal for other applications such as high current, trigger pulse for SCRs and "Triacs." The frequency of oscillation adjusts from under 1 Hz to hundreds of kHz. Waveshape can be set from pulses a few μs wide to approximately a square wave. Thus the LM3909 can perform as a sound effects generator, an audible alarm, or audible continuity checker. Finally it can be a radio (detector/amplifier), low power one-way intercom, two-way telegraph set, or part of a "mini-strobe" light flashing up to 7 times per second.

Operating with only a 1.5 V battery as a supply gives the LM3909 several rather unique characteristics. First, *no* known connection can cause immediate destruction of the IC. Its internal feedback loop insures self-starting of properly loaded oscillator circuits. Experimenters can safely explore the possibilities of the LM3909 as an AC amplifier, one-shot, latch circuit, resistance limit detector, multi-tone oscillator, heat detector, or high frequency oscillator.

With the accent on the practical, a brief circuit description will be given followed by circuits in the following application areas:

Flasher & Indicator Applications

Audio & Oscillator Applications

Trigger & Other Applications

For those who want to modify or design their own circuits using the LM3909, application hints will be covered near the end of this note.

## CIRCUIT DESCRIPTION

The circuit of figure 2 again shows the typical 1.5 V LED flasher, but with the internal circuitry of the IC illustrated.

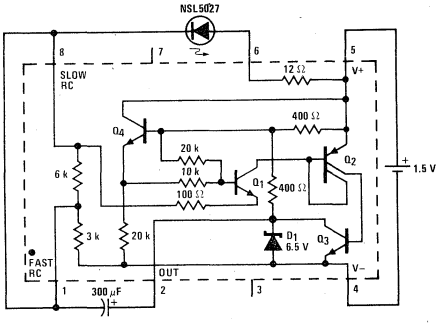



**FIGURE 2. Circuit Operation**

The flasher achieves minimum power usage in two ways. Operated as above, the LED receives current only about 1% of the time. The rest of the time, all transistors but $Q_4$ are off. The 20k resistor from $Q_4$'s emitter to supply-common draws only about 50 $\mu$A. The 300 $\mu$F capacitor is charged through the two 400 $\Omega$ resistors connected to pin 5 and through the 3k resistor connected to pin 4 of the circuit.

Transistors $Q_1$ through $Q_3$ remain off until the capacitor becomes charged to about 1 V. This voltage is determined by the junction drop of $Q_4$, its base-emitter voltage divider, and the junction drop of $Q_1$. When voltage at pin 1 becomes a volt more negative than that at pin 5 (the supply positive terminal) $Q_1$ begins to conduct. This then turns on $Q_2$ and $Q_3$.

The LM3909 then supplies a pulse of high current to the LED. Current amplification of $Q_2$ and $Q_3$ is between 200 and 1000. $Q_3$ can handle over 100 mA and rapidly pulls pin 2 close to supply common (pin 4). Since the capacitor is charged, its other terminal at pin 1 goes *below* the supply common. The voltage at the LED is then higher than battery voltage, and the 12 $\Omega$ resistor between pins 5 and 6 limits the LED current.

Many of the other oscillator circuits work in a similar fashion. If voltage boost is not needed (with or without current limiting) loads can be hooked between pins 2 and 6 or pins 2 and 5.

## APPLICATIONS: Flasher & Indicator

Differing uses and supply voltages will require adjustment of flashing rates. Often it is convenient to leave the capacitor the same value to minimize its size, or to fix the pulse energy to the LED. First, the internal RC resistors can be used to obtain 3k, 6k, or 9k by hooking to or shorting the appropriate pins. Further adjustment methods are shown in the two parts of figure 3 below.

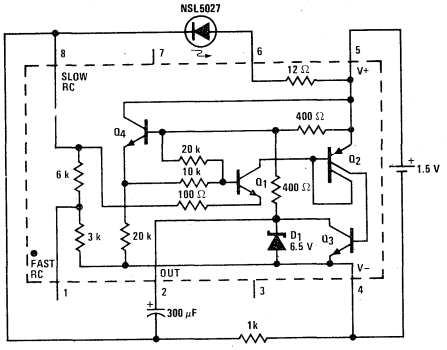



**FIGURE 3a. Fast Blinker**

In figure 3a, it can be seen that the internal RC resistors are shunted by an external 1k between pins 8 and 4. This will give a little over 3 times the flashing rate of the typical 1.5 V flasher of figure 1.

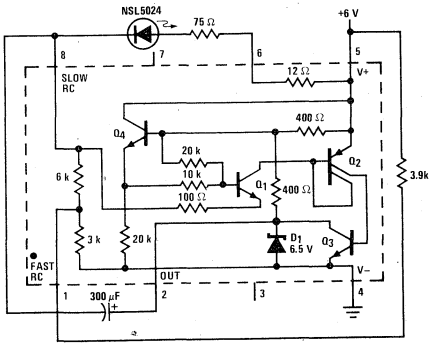



**FIGURE 3b. 6 Volt Flasher**

The 3.9k resistor in figure 3b connected from pin 1 to the 6 V supply raises voltage at the bottom of the 6k RC resistor. Charging current through that resistor is greatly reduced, bringing flashing rate down to about that of the 1.5 V circuit (1 Hz). As will be explained later, this biasing method also insures starting of oscillation even under unfavorable conditions.

Two precautions are taken for circuit reliability. The added 75 Ω series resistor for the LED keeps current peaks within safe limits for the diode and IC. Also, in operation above a 3 V supply, the electrolytic capacitor sees momentary voltage reversals. It should be rated for periodic reversals of 1.5 V.

A continuously appearing indicator light can also be powered from a single 1.5 V cell. Duty cycle and frequency of the current pulses to the LED are increased until the average energy supplied provides sufficient light. At frequencies above 2 kHz, even the fastest movement of the light source or the observer's head will not produce significant flicker.

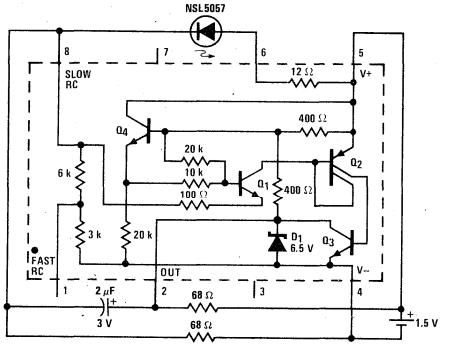



**FIGURE 4. "Continuous" 1.5 V Indicator**

Since this indicator powering circuit uses the smallest capacitor that will reliably provide full output voltage, its operating frequency is well above the 2 kHz point. The indicator is not, however, intended as a long life system, since battery drain is about 12 mA.

High frequency operation requires addition of *two* external resistors, typically of the same value. One, of course, shunts the high internal timing resistors. If only this one were used, the capacitor charging current would have to pass through the two 400 Ω resistors internally connected between pin 5 and the collector of $Q_3$. Oscillation at a slower rate and lower duty cycle than desired would occur, and oscillation might cease altogether before the battery was fully discharged. The second 68 Ω resistor shunting the two 400 Ω resistors eliminates these problems.

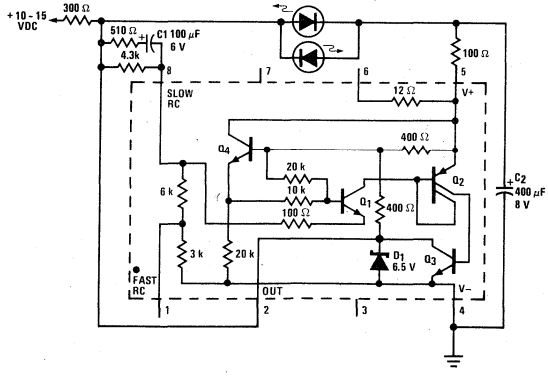



**FIGURE 5. Alternating Flasher**

The circuit above is a relaxation type oscillator flashing 2 LEDs sequentially. With a 12 VDC supply, repetition rate is 2.5 Hz. $C_2$, the timing and storage capacitor, alternately charges through the upper LED and is discharged through the other by the IC's power transistor, $Q_3$.

If a red/green flasher is desired, the green LED should have its anode or plus lead toward pin 5 (like the lower LED). A shorter but higher voltage pulse is available in this position.

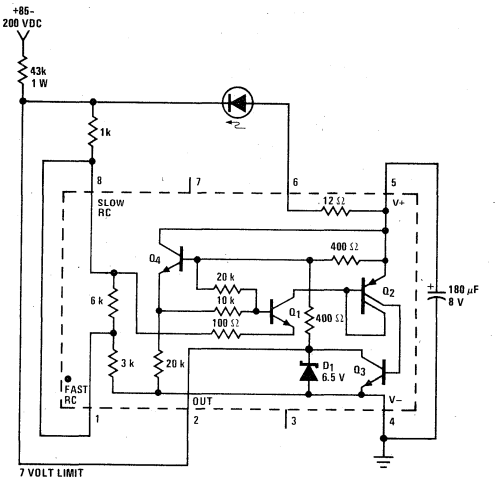



**FIGURE 6. Safe, High Voltage Flasher**

Indication or monitoring of a high voltage power supply at a remote location can be done much more safely than with neon lamps. If the dropping resistor (43k as in figure 6 above) is located at the source end, all other voltages on the line, the IC, and the LED will be limited to less than 7 V, above ground.

The timing capacitor is charged through the dropping resistor and the two 400 Ω collector loads between pins 2 and 5 of the IC. When capacitor voltage reaches about 5 V, there is enough voltage across the 1k resistor (to pin 8) to turn on $Q_1$, and hence trigger on the whole IC to discharge the capacitor through the LED.

There are many other LED applications and variations of circuits. A chart outlining operation of the above circuit at various voltages appears on the LM3909 data sheet. Also shown are circuits for adjusting the flash rate, flashing 4 LEDs in parallel, and details for building a blinking locator light into an ordinary flashlight.

Incandescent bulbs can also be flashed, as already illustrated in figure 1. However, most such bulbs draw more than the 150 mA that the LM3909 can switch. The two following circuits therefore use an added power transistor rated at 1 A or more. In each circuit, an NPN transistor is used, so the power transistor's base drive is obtained from the common or ground pin of the flasher IC.

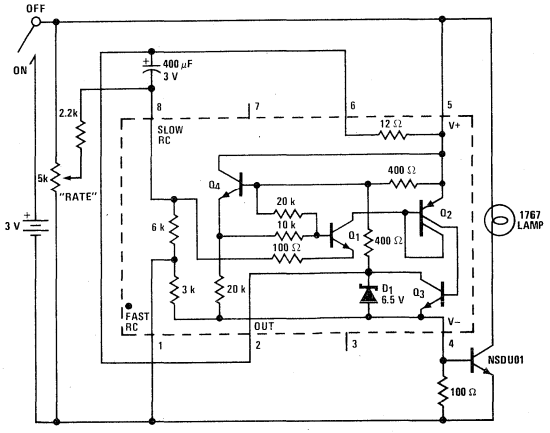



**FIGURE 7. "Mini-Strobe" Variable Flasher**

The 3 V "mini-strobe" of figure 7 may be used as a variable rate warning light or for advertising or special effects. The rate control is so wide range that it adjusts from no flashes at all to continuously on. Chosen for rapid response, the miniature 1767 lamp can be flashed several times a second.

A "mini-strobe" circuit was tested in a Lantern Flashlight with a large reflector. In a dark room, the flashes were almost fast enough to stop a person's motion. As a toy, the fast setting can mimic the strobes at rock concerts or the flicker of old-time movies.

Figure 8 below shows a higher power application such as would use an automotive storage battery for power. It provides about a 1 Hz flash rate and powers a lamp drawing a nominal 600 mA.

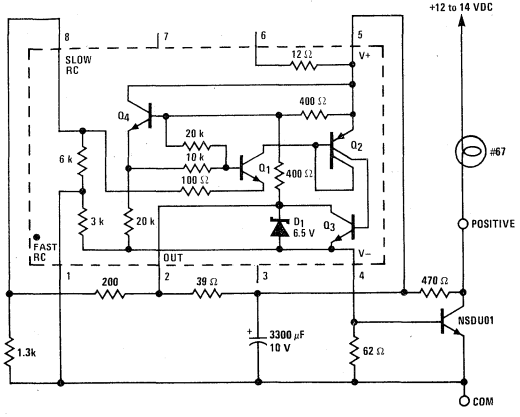



**FIGURE 8. 12 Volt Flasher (2 Wire)**

A particular advantage of this circuit is that it has only 2 external wires and thus may be hooked up in either of the two ways shown below in figure 9. Further, no circuit failure can cause a battery drain greater than that of the bulb itself, continuously lit.

In the circuit of figure 8, the 3300 µF capacitor performs a number of other functions. It makes the LM3909 immune to supply spikes, and provides the means of limiting the IC's supply voltage. Since the LM3909 can only operate with 7.5 V or less on pin 5 (in this circuit) the 200 Ω/1.3k divider attached to pin 8 of the IC causes it to turn fully on at 7 V or less on pin 5. Then the LM3909 discharges the timing capacitor (its own supply voltage) to 4 V or less, whereupon it turns off. The capacitor discharge current comes out of pin 4 of the IC, turning on the NSD U01 transistor. It is the large size of the timing capacitor that allows it to *store* all the needed energy for turning on the power transistor. This in turn permits the whole flasher circuit to operate as a 2 wire device.

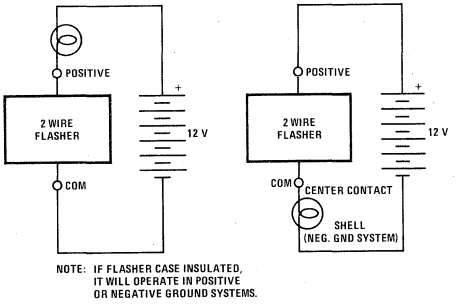



**FIGURE 9. 2 Wire Flasher Usage**

Many other flasher possibilities exist. LED flash rate can be varied from 0 to 20 Hz, or a number of LEDs may be flashed in parallel. With a 3 V supply, yellow and green LEDs may be flashed. A 6 V incandescent "emergency lantern" can be made and its PR-13 bulb may be made to give continuous light or flash by switch selection. This is a more reliable, longer lived system than a lantern with a second thermal flasher bulb. The NSL4944 Current Regulated LED makes possible flashing many LEDs in parallel or with high voltages without series resistors.

## APPLICATIONS: Audio & Oscillator

Very economical continuity checkers, tone generators, and alarms may be made from the LM3909. No matching transformer is needed because the 150 mA capability of the LM3909 output can drive many standard permanent magnet (transistor radio) loudspeakers directly. The 1.5 V battery used in most applications is both lower in cost and longer lasting than the conventional 9 V battery.

In the continuity checker of figure 10, a short, up to about 100 Ω, across the test probes provides enough power for audible oscillation. By probling 2 values in quick succession, small differences such as between a short and 5 Ω can be detected by differences in tone.

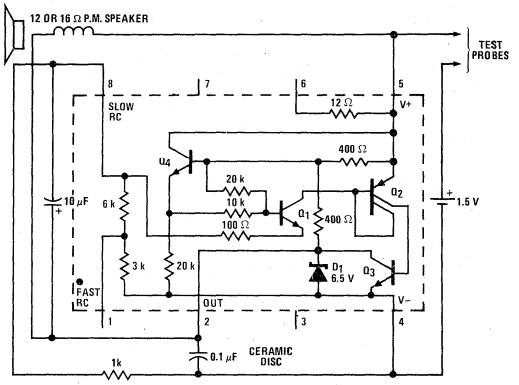



**FIGURE 10. "Buzz Box" Continuity and Coil Checker**

A novel use of this circuit is found in setting the timing of certain types of motorcycles. This is due to the difference in tone that can be heard from the tester depending whether there is a short or not across the low resistance primary of the 'cycle's ignition coil. In other words, the difference between a 1 Ω resistor and a 1 Ω inductor can be heard. Quick checks for shorts and opens in transformers and motors can therefore be made.

Darkrooms, laundry rooms, laboratories, and cellar workshops can often suffer damage from spills or water seepage ruining lumber, chemicals, fertilizer, bags of dry concrete, etc. The circuit of figure 11 is safe on potentially damp floors since there is no connection to the power line. Further, its standby battery drain of 100 μA yields a battery life close to (or, according to some experiments, exceeding) shelf life.

Without moisture, multivibrator transistor $Q_a$ is completely off, and its collector load (6.2k) provides enough current to hold pin 8 of the LM3909 above 0.75 V where it cannot oscillate. When the sense electrodes pass about 0.25 μA, due to moisture, $Q_a$ starts turning on, and since $Q_b$ is already partially biased on, positive feedback now occurs. $Q_a$ and $Q_b$ are now an astable multivibrator which starts at about 1 Hz and oscillates faster as more leakage passes across the sense electrodes.

This "multi" then acts as both an amplifier and a modulator. The pulse waveform at the collector of $Q_a$ varies the timing current through the 3.9k resistor to pin 8 of the LM3909 resulting in a distinctively modulated tone output.

The sensor should be part of the base of the box the alarm circuitry is packaged in. It consists of two electrodes six or eight inches long spaced about 1/8 inch apart. Two strips of stainless steel on insulators, or the appropriate zig-zag path cut in the copper cladding of a circuit board will work well. The bare circuit board between the copper sensing areas should be coated with warm wax so that moisture on the floor, *not* that absorbed by the board, will be detected. The circuit and sensor can be tested by just touching a damp finger to the electrode gap.

Minimum cost, simplicity, and very low power drain are the aims of the Morse Code set of figure 12. One oscillator simultaneously drives speakers at both sending and receiving ends. Calculations and actual use tests indicate life of a single alkaline penlight cell to be 3 months to over a year depending on usage. "Buzzer" type sets use two or more batteries with much shorter life.

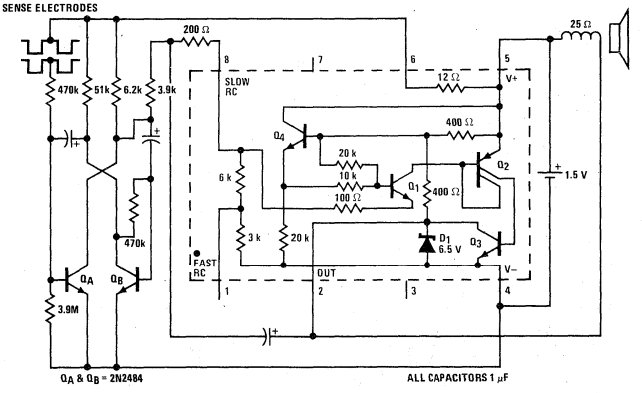



**FIGURE 11. Water Seepage Alarm**

Commonly available, low cost 8 Ω speakers are effectively in series to better match LM3909 characteristics. The three wire system and parallel telegraph keys allow beginners and children to use the set without having to understand use of a "send-receive" switch.

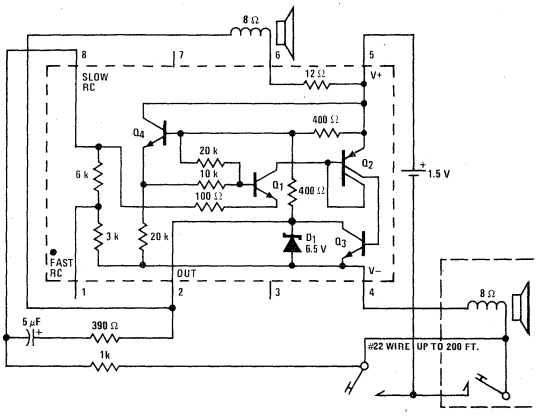



**FIGURE 12. Morse Code Set**

The two resistors are added to obtain a suitable average power output and electrically force the oscillator toward the desired 50% duty cycle. Acoustically, both speakers are operated at resonance (about 400 Hz in the prototype) for maximum pleasing tone with minimum power drain. Each of the two speaker enclosures has holes added to augment this resonance. For each different type or brand of speaker and size of box, hole and capacitor sizes will have to be determined by experiment for the most stable resonant tone over the expected battery voltage variation.

Experiments with the above circuit led to development of the circuit in figure 13. It is optimized to oscillate at any *acoustic* load frequency of resonance! With just a speaker, oscillation occurs at the speaker cone "free-air" resonance. If the speaker is in an enclosure with a higher resonant frequency . . . this becomes the frequency at which the circuit oscillates.

An educational audio demonstration device, or simply an enjoyable toy, has been fabricated as follows. A roughly cubical box of about 64 in.$^3$ was made with one end able to slide in and out like a piston. The box was stiffened with thin layers of pressed wood, etc. Minimum volume with the piston in was about 10 in.$^3$. Speaker, circuit, battery, and all were mounted on the sliding end with the speaker facing out through a 2 1/4 in. hole. A tube was provided (2 1/2 in. long, 5/16 in. ID) to bleed air in and out as the piston was moved while not affecting resonant frequency.

"Slide tones" can be generated, or a tune can be played by properly positioning the piston part and working the push button. Position and direction of the piston are

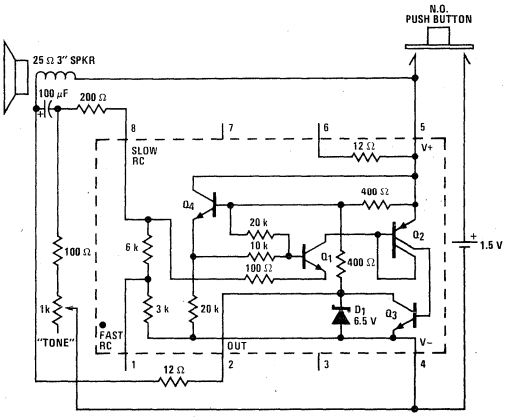



**FIGURE 13. Electronic "Trombone"**

rather intuitive, so it is not difficult to play a reasonable semblance of a tune after a few tries.

The 12 Ω resistor in series with pin 2 (output transistor $Q_3$'s collector) and the speaker, decouples voltages generated by the resonating speaker system from the low impedance switching action of $Q_3$. The 100 μF feedback capacitor would normally set a low or even sub-audio oscillation frequency. Therefore, the major positive feedback voltage to pin 8 is the resonant motion *generated* voltage from the speaker voice coil. Therefore the LM3909 will continue to drive the speaker at the resonance with the highest combined amplitude and frequency.

It can be seen already that the LM3909, having direct speaker drive and resonance following capability, can do things that are a lot less practical with older timer and unijunction circuitry. Two final "sound effect" type of circuits are illustrated below.

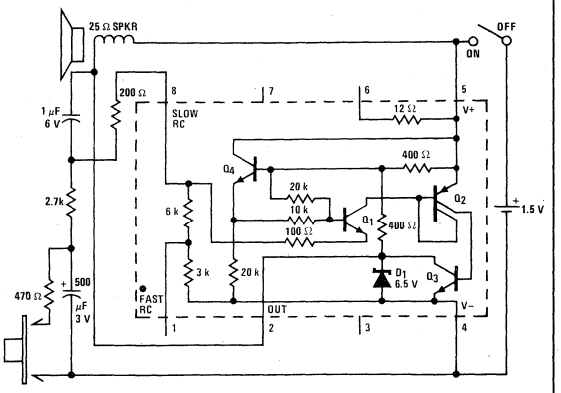



**FIGURE 14a. Fire Siren**

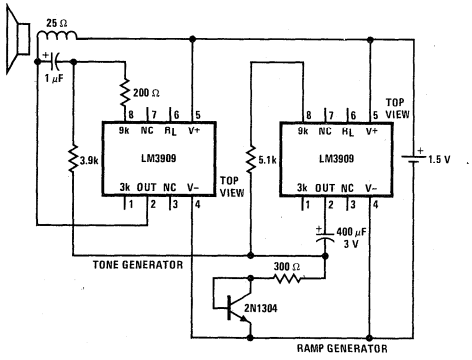



**FIGURE 14b. Whooper Siren**

The siren of figure 14a produces a rapidly rising wail upon pressing the button, and a slower "coasting down" upon release. If it is desirable to have the tone stop sometime after the button is released, an 18k resistor may be placed between pins 8 and 6 of the IC. The sound is then much like that of a motor driven siren.

In this circuit, the oscillation must not be influenced by acoustic resonances. The 1 $\mu$F capacitor and 200 $\Omega$ resistor determine a pulse to the speaker that is wider than that for flashing LEDs, but much narrower than is used in the tuned systems of figures 12 and 13. The repetition rate of speaker pulses is determined by the 2.7k resistor, and the charge on the 500 $\mu$F capacitor. Discharging this capacitor with the pushbutton increases current in the 2.7k resistor causing a rapid upshift in tone.

The "whooper" of figure 14b sounds somewhat like the electronic sirens used on city police cars, ambulances, and airport "crash wagons." The rapid modulation makes the tone seem louder for the same amount of power input.

The tone generator is the same as in the previous siren. Instead of a pushbutton, a rapidly rising and falling modulating voltage is generated by a second LM3909 and its associated 400 $\mu$F capacitor. The 2N1304 transistor is used as a low voltage (germanium) diode. This transistor along with the large feedback resistor (5.1k to pin 8) forces the ramp generator LM3909 into an unusual mode of operation having longer "on" periods than "off" periods. This raises the average tone of the tone generator and makes the modulations seem more even.

## APPLICATIONS: Trigger & Other

With its high pulse current capability, the LM3909 is a good pulse-transformer driver. Further, it uses fewer parts and operates more successfully from low voltage supplies than do the equivalent unijunction circuits. The "Triac" trigger of figure 15 operates from a 5 V logic supply and provides gate trigger pulses of up to 200 mA.

With no gate input, or a TTL logic high input, the LM3909 is biased off since pin 1 is tied to V+. With a logic low at the gate in, the IC provides 10 $\mu$s pulses at about a 7 kC rate. A TTL gate loaded only by this circuit is assumed since otherwise worst-case voltage swing may be insufficient. This trigger is not of the "Synchronized Zero Crossing" type since the first trigger pulse after gating on could occur at any time. However, the repetition rate is such that after the first cycle, a triac is triggered within 8 V of zero with a resistive load and a 115 VAC line.

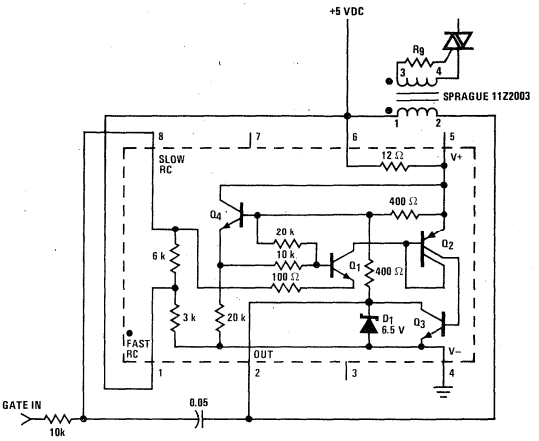



**FIGURE 15. Triac Trigger**

The standard Sprague PC mounting transformer provides a 2:1 current step-up, and suitable isolation between the low voltage circuitry and power lines up to 240 VAC. Resistor $R_g$, which includes transformer winding resistance, can be as little as 3 or 4 $\Omega$ for high current triacs. Low current types may need excessive "holding" current with such low $R_g$, so it may be raised to as much as 100 $\Omega$ with a sensitive gate triac.

Oscillation of the LM3909 will start when the DC bias at pin 8 is between 1.6 and 3.9 V. In figure 15, pin 8 is connected between the 10k input resistor and a 6k resistor to 5 V. With 3.8 V in, pin 8 is at 4.5 V so there is no oscillation. With 1 V, or less, in, pin 8 is at 3.5 V or below and oscillation occurs. From this example, it can be seen that other input resistors or bias dividers can be calculated to gate the LM3909 triac trigger from other logic levels.

A useful electronic lab device is a precision square wave generator/calibrator. If the output is held at a few tenths percent of 1 V, peak-to-peak, it is useful in calibrating oscilloscopes and adjusting 'scope probes. Many lower cost or battery-portable oscilloscopes do not have this feature built in. Also it is useful in checking gain and transient response of various amplifiers including "hi-fi" power amplifiers.

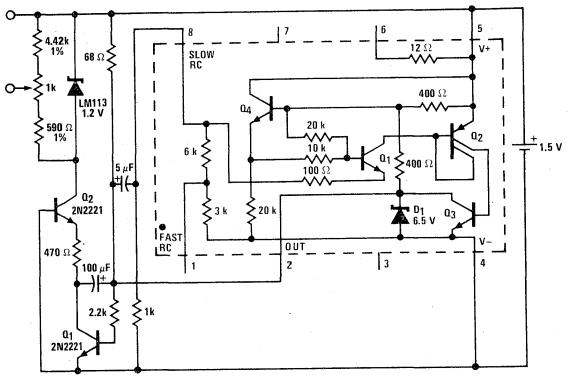



**FIGURE 16. 'Scope Calibrator**

Battery powered equipment is free from both the inconvenience of a line cord, and from some of the noise and hum effects of equipment attached to the power line. Operation for over five hundred hours from a single flashlight "D" cell is the bonus provided by the circuit below. The lowest reference voltage regulator available, the LM113, is used in conjunction with a current source, and the voltage boost characteristic of the LM3909.

Output is a clean rectangular wave which can be adjusted to exactly a 1 V amplitude. A rectangular wave of approximately 1.5 ms "on" and 5.5 ms "off" was chosen for circuit simplicity and low battery drain. Waveform clipping is virtually flat due to complete turn-off of the current switch $Q_2$ and the typical "on" impedance of 0.2 Ω provided by the LM113. The 0.01% temperature coefficient of the LM113 at room temperature allows negligible drift of the waveform amplitude under laboratory conditions. Loading by a 'scope probe will also be insignificant.

The circuit will work properly down to battery voltages of 1.2 V. This is because the 100 μF electrolytic capacitor drives the emitter of $Q_2$ below the supply minus terminal. At a battery voltage of 1.2 V, the collector of $Q_2$ can still swing more than 1.6 V. $Q_1$ uses the "off" periods of the LM3909 to insure that the 100 μF capacitor is charged to almost the entire battery voltage. Thus when the LM3909 turns on and pin 2 drives almost to the minus supply voltage, the negative side of the capacitor is driven 0.9 to 1.2 V below this terminal. Low battery voltage cannot lead to an undetected error in the 1 V squarewave. This is because the waveform becomes distorted rather than just decreasing in amplitude as battery voltage becomes too low.

Taking advantage of the versatility and the indestructability of the LM3909 by a 1.5 V battery, the IC can become an ideal teaching means, or experimental device for the young electronic hobbyist. As well as the circuits already presented, the LM3909 can be made to work as amplifier, radio, and even logic type circuits. The ideas of negative and positive feedback can be presented. The circuits presented below are intended as illustrations or demonstrations of circuitry concepts such as would be used in an experimenter's kit. They are not meant to be used as parts of finished commercial products with specific performance specifications. In other words, working circuits have been breadboarded, but no measurements of performance such as frequency range and distortion have been attempted.

Both tuned circuits above use standard AM radio ferrite antenna coils (loopsticks) with a tap 40% of the turns up from one end. The oscillator works up to 800 kHz or so, and the radio tunes the regular AM broadcast band. Both also use standard (360 pF) AM radio tuning capacitors.

The oscillator has the normal capacitive positive feedback used with LM3909 circuits, but with frequency determined by the tuned circuit loading the output circuit. Detailed operating descriptions of these experimenter's circuits will not be attempted in order to keep down the length of this note. Near the end, a discussion of teh IC's general theory of operation will be given, which should help in understanding the individual circuits.

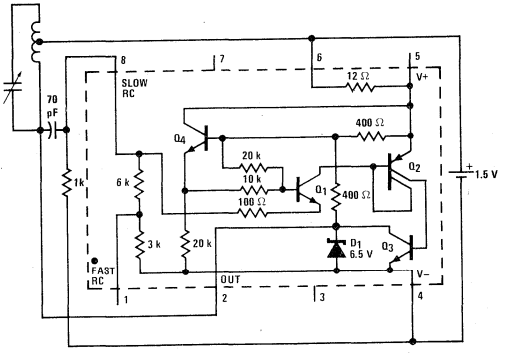



**FIGURE 17. R.F. Oscillator**

In the radio circuit of figure 18, the LM3909 acts as a detector amplifier. It does not oscillate because there is no positive feedback path from pin 2 to pin 8. The tuning ability is only as good as a simple "crystal set," but a local radio station can provide listenable volume

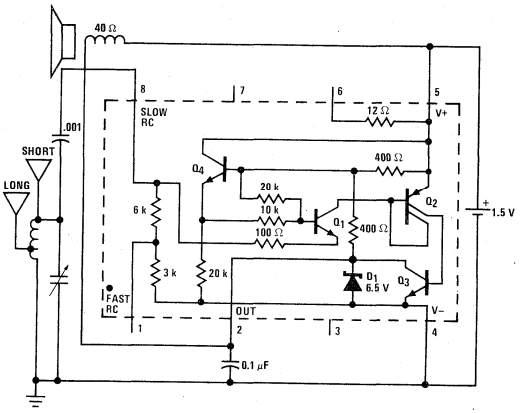



**FIGURE 18. Radio**

with an efficient 6 inch loudspeaker. Extremely low power drain allows a month of continuous radio operation from a single "D" flashlight cell.

Antennae for the radio circuit can be short (10 to 20 feet) and connected directly to the end of the antenna coil as illustrated. Longer antennae (30 to 100 feet) work better if attached to the previously mentioned tap on the coil . . . also illustrated.

The following two circuits are examples of logic or computer type functions. They use 3 V power supplies (2 cells) because the LM3909 was designed not to have any stable or "latching" states with a 1.5 V supply.

Switches on both the above circuits are momentary types. In each case a small charge or impulse affects the circuit's state. The circuit of figure 19 switches to and *holds* its condition whenever the switch changes sides, even if contact is made only very briefly. The circuit of figure 20 delivers about a 1/2 second flash from the LED every time its pushbutton makes contact, whether briefly or for a much longer period of time. Such circuits are used with keyboards, limit switches, and other mechanical contacts that must feed data into electronic digital systems.

By again leaving out the positive feedback capacitor, the LM3909 can become a low power amplifier. This little audio amplifier can be used as a one-way intercom or for "listening in" on various situations. Operating current is only 12 to 15 mA. It can hear fairly faint sounds, and someone speaking directly into the microphone generates a full 1.4 V peak-to-peak at the loudspeaker.

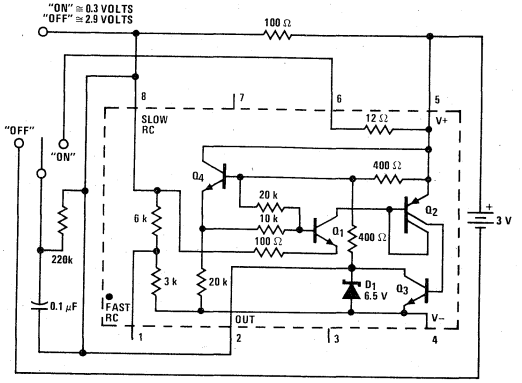



**FIGURE 19. Latch Circuit**

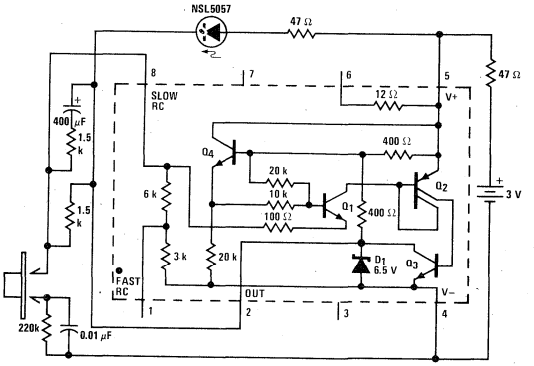



**FIGURE 20. Indicating One-Shot**

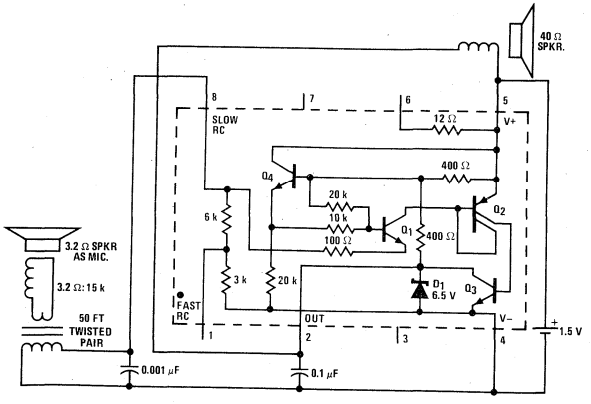



**FIGURE 21. Mini-Power Amplifier**

## APPLICATION HINTS

With 1.5 V supplies, certain problems can occur to stop oscillation or flashing. Due to the way gain is achieved and the type of feedback, too heavy a load may stop an LM3909 from oscillating. 20 Ω of pure resistive *load* will sometimes do it. Strangely enough, lamp filaments, probably because of some inductance, don't seem to follow this rule. Also in flasher circuits, an LED with *leakage* or conductivity between 0.9 and 1.2 V will stop the LM3909. Maybe 1% of LEDs will have this defect because they are not often tested for it.

Great frequency stability was not one of the design aims of the LM3909. In LED flasher circuits it is better than might be expected because the negative temperature coefficient of the LED partially compensates the IC. We planned it this way. Simple oscillators, without the LED, are uncompensated for temperature. This is due to using 1 2/3 of a silicon junction drop as the on-off trip point and the use of the integrated timing resistors with their positive temperature coefficient. Further, most capacitors of 1 μF or over, shown in the circuits, will usually be electrolytics for size reasons. These, however, are not particularly stable with temperature and their initial tolerances vary greatly with type of capacitor.

In most of the oscillator circuits, frequency is also proportional to battery voltage. This must be considered when starting with a completely unused cell at 1.54 V or so and deciding what the "end-of-life" voltage is to be. This can be in the range of 1.1 to 0.9 V, a drastic change. It helps to remember how bright flashlights are with a fresh set of batteries, and how dim they are when the batteries are finally changed.

Flashers and tone generators for alarms are not, however, demanding for stability. Flash rate changes of 50% or tone shifts of 1/2 an octave are not particularly annoying or even too noticeable.

One interesting point is that the low operating power of most of the circuits presented allows them to be powered by *solar cells* as well as regular batteries. In bright sunlight, 3 to 4 cells in series will be needed. In dimmer light, 4 to 6 cells will do the job. Current from cells way under an inch in area generally will be sufficient, but circuits drawing a high pulse current (such as SCR triggers) will need a surge storage capacitor across the solar cell array.

The LM3909 was designed to be inherently self-starting as an oscillator, and LED flasher circuits *are*, at any voltage, because the load is nonlinear. A load with sufficient self inductance will always self-start, although possibly at a higher than expected frequency. There is an exception for largely resistive loads on an oscillator operating with a supply larger than 2 or 2.5 V. A stable state exists with $Q_3$ turned completely "on" and the timing resistors from pin 8 to the supply minus still drawing current. A reliable solution is to bias pin 8 (for instance with a resistor to V+) so that its DC voltage is one half V less than half the supply voltage.

The duty cycle of the basic LED flasher is inherently low since the timing capacitor is also driving the very low LED "on" impedance. For other oscillators the "on" duty cycle can be stretched by adding resistance in series with the timing capacitor. Additionally, nonlinear resistance can be used as timing resistance. (See figure 14b.)

## CONCLUSION

Applications covered in this note range in use from toys to the laboratory, and in frequency from DC to RF. The LM3909 can be used to amuse, teach, or even upon occasion to save a life. As a practical cost consideration the LM3909 IC can often replace a circuit having a number of transistors, associated parts, and high assembly cost.

Further, the LM3909 demonstrates the practicality of very low voltage electronic circuits. They can work at high efficiencies if ingenuity is used to design around transistor junction drops. In such circuits stresses on parts are so low that extremely long life can be predicted. Often transistors, capacitors, etc. that would be rejects at higher voltages can be used. Voltage dividers, protective diodes, etc. often needed at higher voltages can be left out of designs. Power drains are so low that circuits can be made that will last months to years on a single cell.

A single cell is more reliable and has a higher energy density than multiple cells. This is due to lack of cell interconnections and insulation as well as elimination of packaging to hold multiple cells in place.

Jim Sherwin
FEBRUARY 1976

# SPECIFYING A/D AND D/A CONVERTERS

The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you insure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

## MEANING OF PERFORMANCE SPECS

**Resolution** describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in $2^n$. The least significant increment is then $2^{-n}$, or one least significant bit (LSB). In contrast, the most significant bit (MSB) carries a weight of $2^{-1}$. Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in $2^{12}$ (1 part in 4096) or 0.0245% of full scale. A converter with 10V full scale could resolve a 2.45mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0245% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

**Accuracy** is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than ±½ LSB or ±1 part in $2^{12+1}$ (±0.0122% of full scale due to finite resolution). This would be the case in figure 1 if there were no errors. Actually, ±0.0122% FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ±1 LSB accurate, this is equivalent to ±0.0245% or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately.

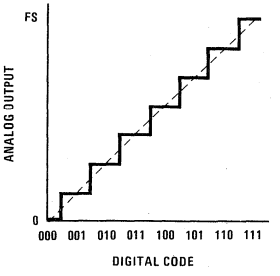



**FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy**

**Quantizing Error** is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset ½ LSB at zero scale as shown in figure 2, exhibits only ±½ LSB maximum output error. If not offset, the error will be $^{+1}_{-0}$ LSB as shown in figure 3. For example, a perfect 12-bit ADC will show a ±½ LSB error of ±0.0122% while the quantizing error of an 8-bit ADC is ±½ part in $2^8$ or ±0.195% of full scale. Quantizing error is not strictly applicable to a DAC; the equivalent effect is more properly a resolution error.

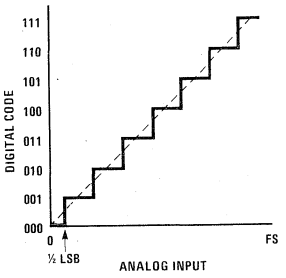



**FIGURE 2. ADC Transfer Curve, ½ LSB Offset at Zero**

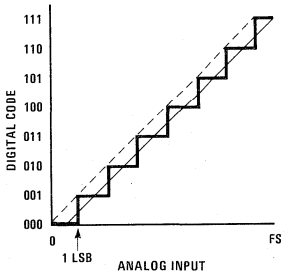



**FIGURE 3. ADC Transfer Curve, No Offset**

**Scale Error** (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See figure 4.) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient.**) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of figure 7, a scale adjustment at ¾ scale could improve the overall ± accuracy compared to an adjustment at full scale.

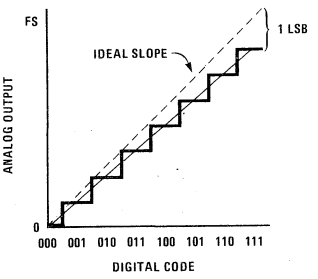



**FIGURE 4. Linear, 1 LSB Scale Error**

**Gain Error** is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

**Offset Error** (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See figure 5.) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.

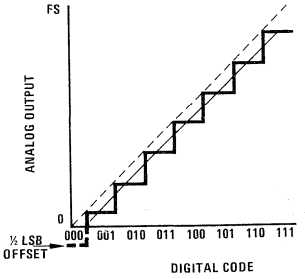



**FIGURE 5. Linear, ½ LSB Offset Error**

**Hysteresis Error** in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches ½ LSB.

**Linearity**, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specifi-

cation of ±½ LSB linearity implies error in addition to the inherent ±½ LSB quantizing or resolution error. In reference to figure 2, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than ±½ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ±1 LSB (½ LSB resolution error plus ½ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A ±½ LSB linearity spec guarantees monotonicity (see below) and ⩽ ±1 LSB differential non-linearity (see below). In the example of figure 6, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond ±½ LSB will allow for a non-monotonic transfer curve. Figure 7 shows a typical non-linear curve; non-linearity is 1¼ LSB yet the curve is smooth and monotonic.

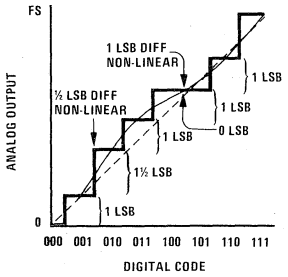



**FIGURE 6. ±½ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)**

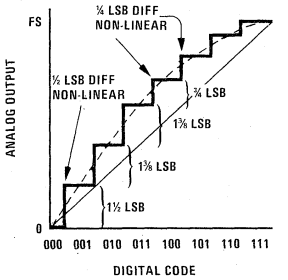



**FIGURE 7. 1¼ LSB Non-Linear, ½ LSB Differential Non-Linearity**

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

**Differential Non-Linearity** indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit ½ LSB differential non-linearity (see figures 6 and 7). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. Figure 6 shows a curve with a ±½ LSB linearity and ±1 LSB differential non-linearity while figure 7 shows a curve with +1¼ LSB linearity and ±½ LSB differential non-linearity. In many user applications, the curve of figure 7 would be preferred over that of figure 6 because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in figure 8 where the linearity spec is ±1 LSB and the differential linearity spec is ±2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in figure 8. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2.6-bit converter?). The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter. Differential non-linearity can always be as much as twice the non-linearity, but no more.

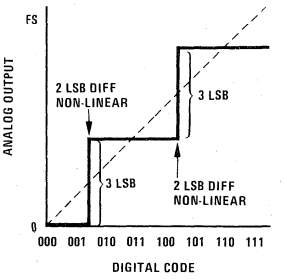



**FIGURE 8. ±1 LSB Linear, ±2 LSB Differential Non-Linear**

**Monotonicity.** A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed ±½ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage in some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A ±½ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than ±½ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with ±½ bit linearity to 10 bits (not ±½ LSB) will be monotonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.

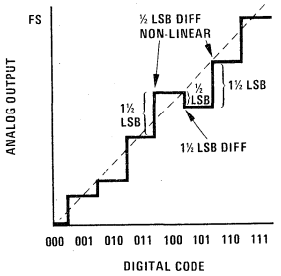
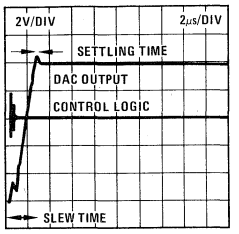
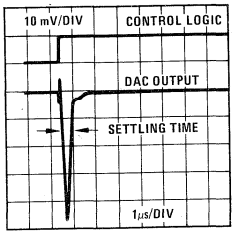



FIGURE 9. Non-Monotonic (Must be > ±½ LSB Non-Linear)




(a) Full-Scale Step




(b) 1 LSB Step

FIGURE 10. DAC Slew and Settling Time

**Settling Time** is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±½ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. Figure 10 delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

**Slew Rate** is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/μs. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in figure 10.

**Overshoot and Glitches** occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These glitches are normally of extremely short duration but could be of ½ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.

**Temperature Coefficient** of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

**Long-Term Drift**, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

**Supply Rejection** relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C.

**Conversion Rate** is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

**Clock Rate** is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

**Input Impedance** of an ADC describes the load placed on the analog source.

**Output Drive Capability** describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

## CODES

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

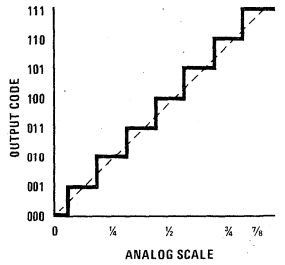
**Natural Binary** (or simply Binary) is the usual $2^n$ code with 2, 4, 8, 16, . . . , $2^n$ progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal. Zero scale is then all "zeros" while full scale is all "ones."

**Complementary Binary** (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

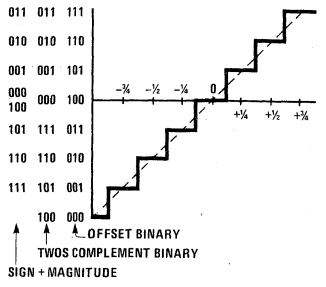
**Binary Coded Decimal** (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

**Offset Binary** is a natural binary code except that it is offset (usually ½ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in figure 11.

**Twos Complement Binary** is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number –8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for ± representation in 4 bits so not a valid code in the ± scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in figure 11. Note that the offset binary representation of the ± scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.




(a) Zero to + Full-Scale




(b) ± Full-Scale

**FIGURE 11. ADC Codes**

**Sign Plus Magnitude** coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in figure 11. Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

## CONTROL

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

**Start Conversion** (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

**End of Conversion** (EOC) is a digital signal from an ADC which informs the external system that the digital output data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

**Clock** signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

## CONCLUSION

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

Robert Dobkin
JUNE 1976

# IC VOLTAGE REFERENCE HAS 1 PPM PER DEGREE DRIFT

A new linear IC now provides the ultimate in highly stable voltage references. Now, a new monolithic IC the LM199, out-performs zeners and can provide a 6.9V reference with a temperature drift of less than 1 ppm/° and excellent long term stability. This new IC, uses a unique subsurface zener to achieve low noise and a highly stable breakdown. Included is an on-chip temperature stabilizer which holds the chip temperature at 90°C, eliminating the effects of ambient temperature changes on reference voltage.

The planar monolithic IC offers superior performance compared to conventional reference diodes. For example, active circuitry buffers the reverse current to the zener giving a dynamic impedance of 0.5Ω and allows the LM199 to operate over a 0.5 mA to 10 mA current range with no change in performance. The low dynamic impedance, coupled with low operating current significantly simplifies the current drive circuitry needed for operation. Since the temperature coefficient is independent of operating current, usually a resistor is all that is needed.

Previously, the task of providing a stable, low temperature coefficient reference voltage was left to a discrete zener diode. However, these diodes often presented significant problems. For example, ordinary zeners can show many millivolts change if there is a temperature gradient across the package due to the zener and temperature compensation diode not being at the same temperature. A 1°C difference may cause a 2 mV shift in reference voltage. Because the on-chip temperature stabilizer maintains constant die temperature, the IC reference is free of voltage shifts due to temperature gradients. Further, the temperature stabilizer, as well as eliminating drift, allows exceptionally fast warm-up over conventional diodes. Also, the LM199 is insensitive to stress on the leads—another source of error with ordinary glass diodes. Finally, the LM199 shows virtually no hysteresis in reference voltage when subject to temperature cycling over a wide temperature range. Temperature cycling the LM199 between 25°C, 150°C and back to 25°C causes less than 50μV change in reference voltage. Standard reference diodes exhibit shifts of 1 mV to 5 mV under the same conditions.

## SUB SURFACE ZENER IMPROVES STABILITY

Previously, breakdown references made in monolithic IC's usually used the emitter-base junction of an NPN transistor as a zener diode. Unfortunately, this junction breaks down at the surface of the silicon and is therefore susceptible to surface effects. The breakdown is noisy, and cannot give long-term stabilities much better than about 0.3%. Further, a surface zener is especially sensitive to contamination in the oxide or charge on the surface of the oxide which can cause short-term instability or turn-on drift.

The new zener moves the breakdown below the surface of the silicon into the bulk yielding a zener that is stable with time and exhibits very low noise. Because the new zener is made with well-controlled diffusions in a planar structure, it is extremely reproducible with an initial 2% tolerance on breakdown voltage.

A cut-away view of the new zener is shown in *Figure 1.* First a small deep P+ diffusion is made into the surface of the silicon. This is then covered by the standard base diffusion. The N+ emitter diffusion is then made completely covering the P+ diffusion. The diode then breaks down where the dopant concentration is greatest, that is, between the P+ and N+. Since the P+ is completely covered by N+ the breakdown is below the surface and at about 6.3V. One connection to the diode is to the N+ and the other is to the P base diffusion. The current flows laterally through the base to the P+ or cathode of the zener. Surface breakdown does not occur since the base P to N+ breakdown voltage is greater than the breakdown of the buried device. The buried zener has been in volume production since 1973 as the reference in the LX5600 temperature transducer.

## CIRCUIT DESCRIPTION

The block diagram of the LM199 is shown in *Figure 2.* Two electrically independent circuits are included on the same chip—a temperature stabilizer and a floating active zener. The only electrical connection between the two

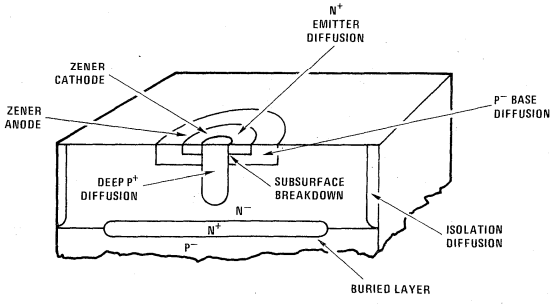



**FIGURE 1. Subsurface Zener Construction**

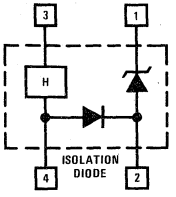



**FIGURE 2. Functional Block Diagram**

circuits is the isolation diode inherent in any junction-isolated integrated circuit. The zener may be used with or without the temperature stabilizer powered. The only operating restriction is that the isolation diode must never become forward biased and the zener must not be biased above the 40V breakdown of the isolation diode.

The actual circuit is shown in *Figure 3.* The temperature stabilizer is composed of Q1 through Q9. FET Q9 provides current to zener D2 and Q8. Current through Q8 turns a loop consisting of D1, Q5, Q6, Q7, R1 and R2. About 5V is applied to the top of R1 from the base of Q7. This causes 400$\mu$A to flow through the divider R1, R2. Transistor Q7 has a controlled gain of 0.3 giving Q7 a total emitter current of about 500$\mu$A. This flows through the emitter of Q6 and drives another controlled gain PNP transistor Q5. The gain of Q5 is about 0.4 so D1 is driven with about 200$\mu$A. Once current flows through Q5, Q8 is reverse biased and the loop is self-sustaining. This circuitry ensures start-up.

The resistor divider applies 400 mV to the base of Q4 while Q7 supplies 120$\mu$A to its collector. At temperatures below the stabilization point, 400 mV is insufficient to cause Q4 to conduct. Thus, all the collector current from Q7 is provided as base drive to a Darlington composed of Q1 and Q2. The Darlington is connected across the supply and initially draws 140 mA (set by current limit transistor Q3). As the chip heats, the turn on voltage for Q4 decreases and Q4 starts to conduct. At about 90°C the current through Q4 appreciably increases and less drive is applied to Q1 and Q2. Power dissipation decreases to whatever is necessary to hold the chip at the stabilization temperature. In this manner, the chip temperature is regulated to better than 2°C for a 100°C temperature range.

The zener section is relatively straight-forward. A buried zener D3 breaks down biasing the base of transistor Q13. Transistor Q13 drives two buffers Q12 and Q11. External current changes through the circuit are fully absorbed by the buffer transistors rather than D3. Current through D3 is held constant at 250$\mu$A by a 2k resistor across the emitter base of Q13 while the emitter-base voltage of Q13 nominally temperature compensates the reference voltage.

The other components, Q14, Q15 and Q16 set the operating current of Q13. Frequency compensation is accomplished with two junction capacitors.

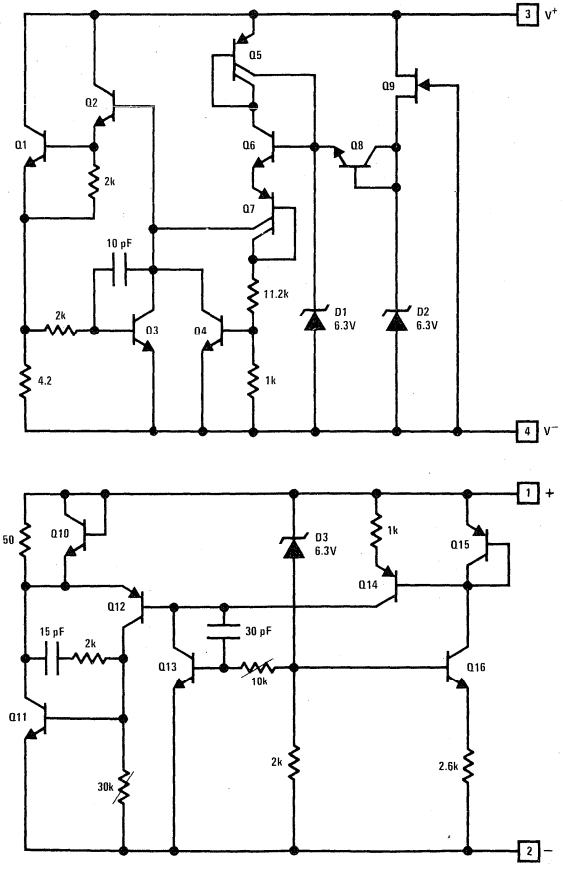



**FIGURE 3. Schematic Diagram of LM199 Precision Reference**

## PERFORMANCE

A polysulfone thermal shield, shown in *Figure 4,* is supplied with the LM199 to minimize power dissipation and improve temperature regulation. Using a thermal shield as well as the small, high thermal resistance TO-46 package allows operation at low power levels without the problems of special IC packages with built-in thermal isolation. Since the LM199 is made on a standard IC assembly line with standard assembly techniques, cost is significantly lower than if special techniques were used. For temperature stabilization only 300 mW are required at 25°C and 660 mW at −55°C.

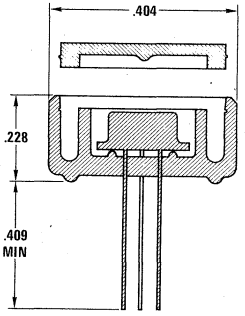



**FIGURE 4. Polysulfone Thermal Shield**

Temperature stabilizing the device at 90°C virtually eliminates temperature drift at ambient temperatures less than 90°C. The reference is nominally temperature compensated and the thermal regulator further decreases the temperature drift. Drift is typically only 0.3 ppm/°C. Stabilizing the temperature at 90°C rather than 125°C significantly reduces power dissipation but still provides very low drift over a major portion of the operating temperature range. Above 90°C ambient, the temperature coefficient is only 15 ppm/°C.

A low drift reference would be virtually useless without equivalent performance in long term stability and low noise. The subsurface breakdown technology yields both of these. Wideband and low frequency noise are both exceptionally low. Wideband noise is shown in *Figure 5* and low frequency noise is shown over a 10 minute period in the photograph of *Figure 6.* Peak to peak noise over a 0.01 Hz to 1 Hz bandwidth is only about 0.7μV.

Long term stability is perhaps one of the most difficult measurements to make. However, conditions for long-term stability measurements on the LM199 are considerably more realistic than for commercially available certified zeners. Standard zeners are measured in ±0.05°C temperature controlled both at an operating current of 7.5 mA ±0.05μA. Further, the standard devices must have stress-free contacts on the leads and the test must not be interrupted during the measurement interval. In contrast, the LM199 is measured in still air of 25°C to 28°C at a reverse current of 1 m[illegible] ±0.5%. This is more typical of actual operating conditions in instruments.

When a group of 10 devices were monitored for long-term stability, the variations all correlated, which indicates changes in the measurement system (limitation of 20 ppm) rather than the LM199.

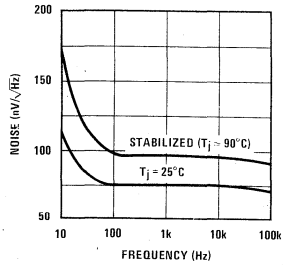



**FIGURE 5. Wideband Noise of the LM199 Reference**

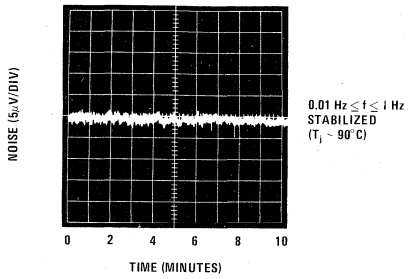



**FIGURE 6. Low Frequency Noise Voltage**

Because the planar structure does not exhibit hysteresis with temperature cycling, long-term stability is not impaired if the device is switched on and off.

The temperature stabilizer heats the small thermal mass of the LM199 to 90°C very quickly. Warm-up time at 25°C and −55°C is shown in *Figure 7.* This fast warm-up is significantly less than the several minutes needed by ordinary diodes to reach equilibrium. Typical specifications are shown in Table I.

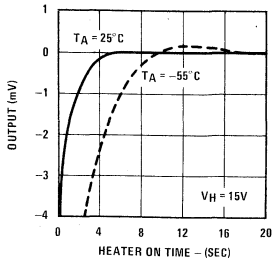



**FIGURE 7. Fast Warmup Time of the LM199**

**Table I. Typical Specifications for the LM199**

| | |
|---|---|
| Reverse Breakdown Voltage | 6.95V |
| Operating Current | 0.5 mA to 10 mA |
| Temperature Coefficient | 0.3 ppm/°C |
| Dynamic Impedance | 0.5Ω |
| RMS Noise (10 Hz to 10 kHz) | 7μV |
| Long-Term Stability | ≤ 20 ppm |
| Temperature Stabilizer Operating Voltage | 9V to 40V |
| Temperature Stabilizer Power Dissipation (25°C) | 300 mW |
| Warm-up Time | 3 Seconds |

## APPLICATIONS

The LM199 is easier to use than standard zeners, but the temperature stability is so good—even better than precision resistors—that care must be taken to prevent external circuitry from limiting performance. Basic operation only requires energizing the temperature stabilizer from a 9V to 40V power source and biasing the reference with between 0.5 mA to 10 mA of current. The low dynamic impedance minimizes the current regulation required compared to ordinary zeners.

The only restriction on biasing the zener is the bias applied to the isolation diode. Firstly, the isolation diode must not be forward biased. This restricts the voltage at either terminal of the zener to a voltage equal to or greater than the $V^-$.

A dc return is needed between the zener and heater to insure the voltage limitation on the isolation diodes are not exceeded. *Figure 8* shows the basic biasing of the LM199.

The active circuitry in the reference section of the LM199 reduces the dynamic impedance of the zener to about 0.5Ω. This is especially useful in biasing the reference. For example, a standard reference diode such as a 1N829 operates at 7.5 mA and has a dynamic impedance of 15Ω. A 1% change in current (75μA) changes the reference voltage by 1.1 mV. Operating the LM199 at 1 mA with the same 1% change in operating current (10μA) results in a reference change of only 5μV. *Figure 9* shows reverse voltage change with current.

Biasing current for the reference can be anywhere from 0.5 mA to 10 mA with little change in performance. This wide current range allows direct replacement of most zener types with no other circuit changes besides the temperature stabilizer connection. Since the dynamic impedance is constant with current changes regulation

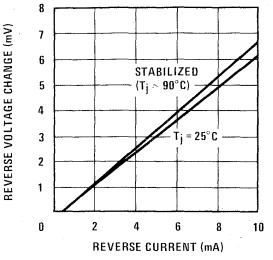



**FIGURE 9. The LM199 Shows Excellent Regulation Against Current Changes**

is better than discrete zeners. For optimum regulation, lower operating currents are preferred since the ratio of source resistance to zener impedance is higher, and the attenuation of input changes is greater. Further, at low currents, the voltage drop in the wiring is minimized.

Mounting is an important consideration for optimum performance. Although the thermal shield minimizes the heat low, the LM199 should not be exposed to a direct air flow such as from a cooling fan. This can cause as much as a 100% increase in power dissipation degrading the thermal regulation and increasing the drift. Normal conviction currents do not degrade performance.

Printed circuit board layout is also important. Firstly, four wire sensing should be used to eliminate ohmic drops in pc traces. Although the voltage drops are small the temperature coefficient of the voltage developed along a copper trace can add significantly to the drift. For example, a trace with 1Ω resistance and 2 mA current flow will develop 2 mV drop. The TC of copper is 0.004%/°C so the 2 mV drop will change at 8μV/°C, this is an additional 1 ppm drift error. Of course, the effects of voltage drops in the printed circuit traces are eliminated with 4-wire operation. The heater current also should not be allowed to flow through the voltage reference traces. Over a −55°C to +125°C temperature

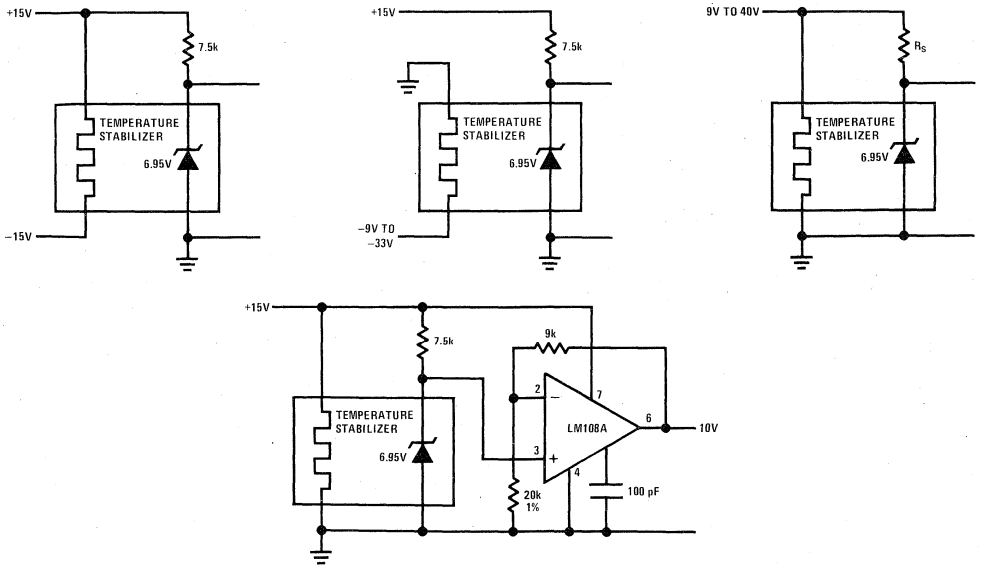



**FIGURE 8. Basic Biasing of the LM199**

range the heater current will change from about 1 mA to over 40 mA. These magnitudes of current flowing reference leads or reference ground can cause huge errors compared to the drift of the LM199.

Thermocouple effects can also cause errors. The kovar leads from the LM199 package form a thermocouple with copper printed circuit board traces. Since the package of the 199 is heated, there is a heat flow along the leads of the LM199 package. If the leads terminate into unequal sizes of copper on the p.c. board greater heat will be absorbed by the larger copper trace and a temperature difference will develop. A temperature *difference* of 1°C between the two leads of the reference will generate about 30μV. Therefore, the copper traces to the zener should be equal in size. This will generally keep the errors due to thermocouple effects under about 15μV.

The LM199 should be mounted flush on the p.c. board with a minimum of space between the thermal shield and the boards. This minimizes air flow across the kovar leads on the board surface which also can cause thermocouple voltages. Air currents across the leads usually appear as ultra-low frequency noise of about 10μV to 20μV amplitude.

It is usually necessary to scale and buffer the output of any reference to some calibrated voltage. *Figure 10* shows a simple buffered reference with a 10V output. The reference is applied to the non-inverting input of the LM108A. An RC rolloff can be inserted in series with the input to the LM108A to roll-off the high frequency noise. The zener heater and op amp are all powered from a single 15V supply. About 1% regulation on the input supply is adequate contributing less than 10μV of error to the output. Feedback resistors around the LM308 scale the output to 10V.

Although the absolute values of the resistors are not extremely important, tracking of temperature coefficients is vital. The 1 ppm/°C drift of the LM199 is easily exceeded by the temperature coefficient of most resistors. Tracking to better than 1 ppm is also not easy to obtain. Wirewound types made of Evenohm or Mangamin are good and also have low thermoelectric effects. Film types such as Vishay resistors are also good. Most potentiometers do not track fixed resistors so it is a good idea to minimize the adjustment range and therefore minimize their effects on the output TC. Overall temperature coefficient of the circuit shown in *Figure 10* is worst case 3 ppm/°C. About 1 ppm is due to the reference, 1 ppm due to the resistors and 1 ppm due to the op amp.

*Figure 11* shows a standard cell replacement with a 1.01V output. A LM321 and LM308 are used to minimize op amp drift to less than 1μV/°C. Note the adjustment connection which minimizes the TC effects of the pot. Set-up for this circuit requires nulling the offset of the op amp first and then adjusting for proper output voltage.

The drift of the LM321 is very predictable and can be used to eliminate overall drift of the system. The drift changes at 3.6μV/°C per millivolt of offset so 1 mV to 2 mV of offset can be introduced to minimize the overall TC.

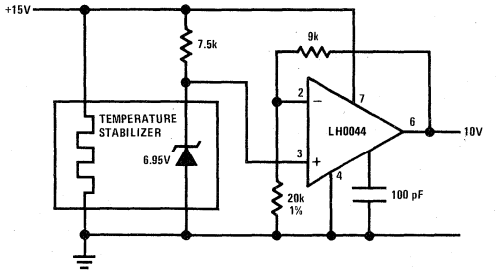



**FIGURE 10. Buffered 10V Reference**

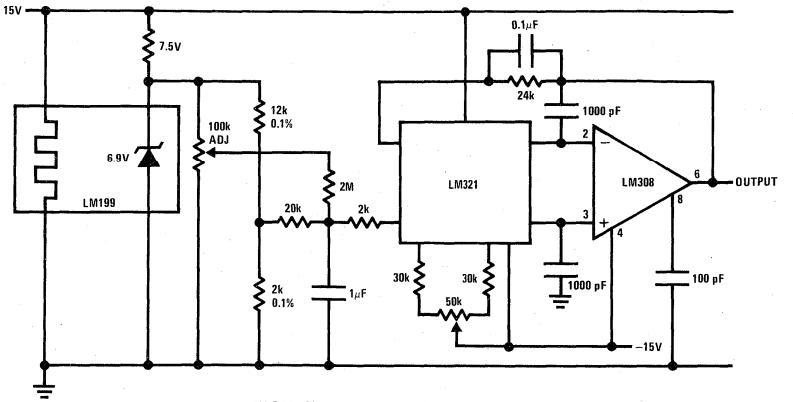



**FIGURE 11. Standard Cell Replacement**

For circuits with a wide input voltage range, the reference can be powered from the output of the buffer as is shown in *Figure 12.* The op amp supplies regulated voltage to the resistor biasing the reference minimizing changes due to input variation. There is some change due to variation of the temperature stabilizer voltage so extremely wide range operation is not recommended for highest precision. An additional resistor (shown 80 kΩ) is added to the unregulated input to insure the circuit starts up properly at the application of power.

A precision power supply is shown in *Figure 13.* The output of the op amp is buffered by an IC power transistor the LM395. The LM395 operates as an NPN power device but requires only 5μA base current. Full overload protection inherent in the LM395 includes current limit, safe-area protection, and thermal limit.

A reference which can supply either a positive or a negative continuously variable output is shown in *Figure 14.* The reference is biased from the ±15V input supplies as was shown earlier. A ten-turn pot will adjust the output from $+V_Z$ to $-V_Z$ continuously. For negative output the op amp operates as an inverter while for positive outputs it operates as a non-inverting connection.

Op amp choice is important for this circuit. A low drift device such as the LM108A or a LM108-LM121 combination will provide excellent performance. The pot should be a precision wire wound 10 turn type. It should be noted that the output of this circuit is not linear.

## CONCLUSIONS

A new monolithic reference which exceeds the performance of conventional zeners has been developed. In fact, the LM199 performance is limited more by external components than by reference drift itself. Further, many of the problems associated with conventional zeners such as hysteresis, stress sensitivity and temperature gradient sensitivity have also been eliminated. Finally, long-term stability and noise are equal of the drift performance of the new device.

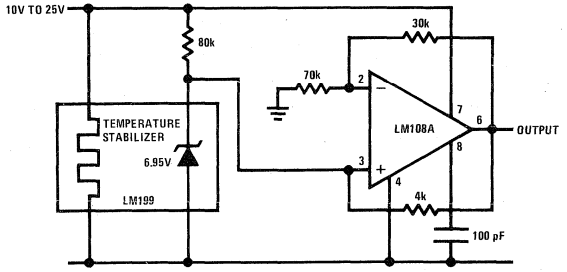



**FIGURE 12. Wide Range Input Voltage Reference**

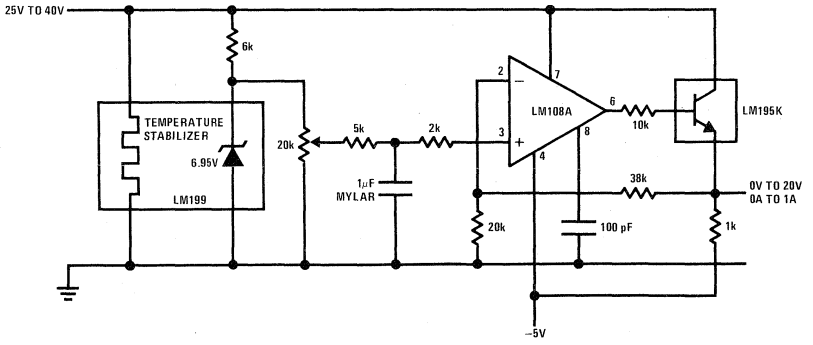



**FIGURE 13. Precision Power Supply**

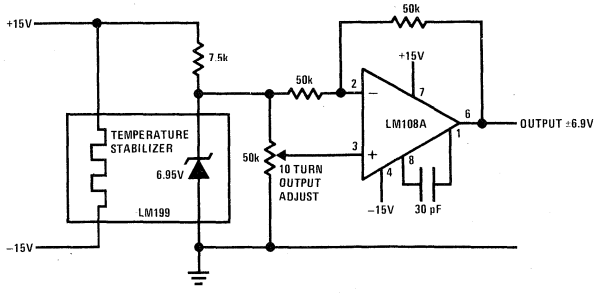



**FIGURE 14. Bipolar Output Reference**

Dave Long
JUNE 1976

# LM2907, LM2917 TACHOMETER/SPEED SWITCH BUILDING BLOCK APPLICATIONS

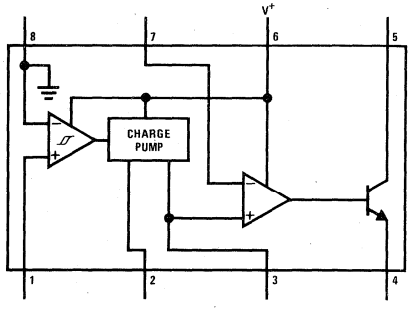
## INTRODUCTION

Frequency to voltage converters are available in a number of forms from a number of sources, but invariably require significant additional components before they can be put to use in a given situation. The LM2907, LM2917 series of devices was developed to overcome these objections. Both input and output interface circuitry is included on chip so that a minimum number of additional components is required to complete the function. In keeping with the systems building block concept, these devices provide an output voltage which is proportional to input frequency and provide zero output at zero frequency. In addition, the input may be referred to ground. The devices are designed to operate from a single supply voltage, which makes them particularly suitable for battery operation.

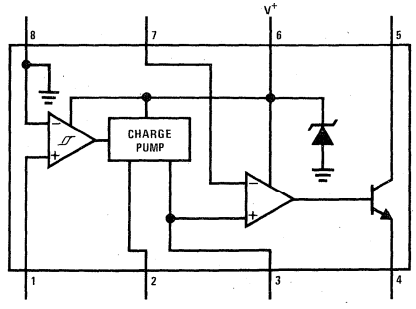
## PART I — GENERAL OPERATION PRINCIPLES

### Circuit Description

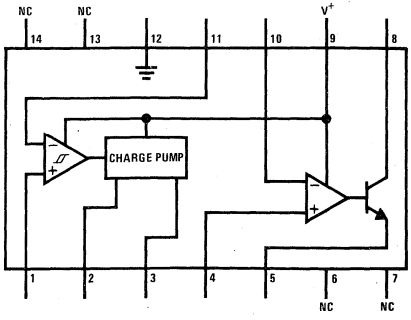
Referring to *Figure 1,* the family of devices all include three basic components: an input amplifier with built-in hysteresis; a charge pump frequency to voltage converter; and a versatile op amp/comparator with an uncommitted output transistor. LM2917 incorporates an active zener regulator on-chip. LM2907 deletes this option. Both versions are obtainable in 14-pin and in 8-pin dual-in-line molded packages, and to special order in other packages.



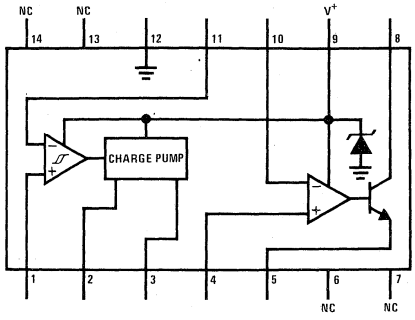

LM2907N-8




LM2917N-8




LM2907N




LM2917N

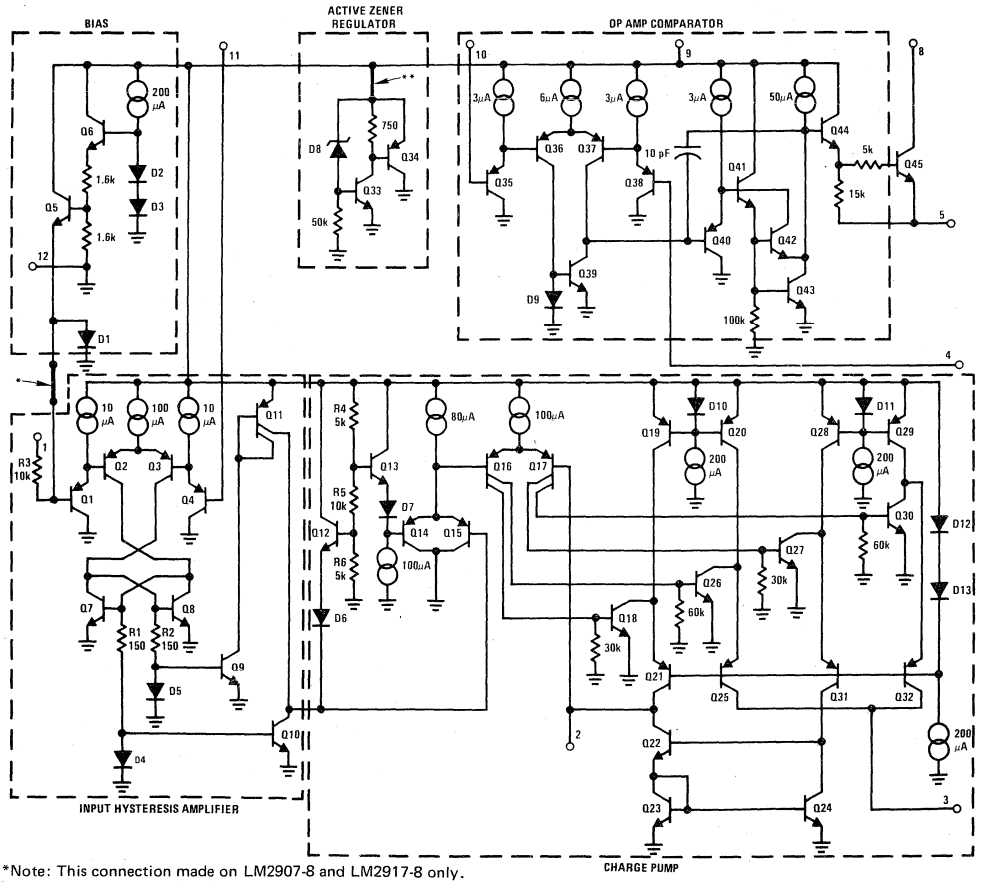
**FIGURE 1. Block Diagrams**

### Input Hysteresis Amplifier

The equivalent schematic diagram is shown in *Figure 2.* Q1 through Q11 comprise the input hysteresis amplifier. Q1 through Q4 comprise an input differential amplifier which, by virtue of PNP level shifting, enables the circuit to operate with signals referenced to ground. Q7, Q8, D4, and D5 comprise an active load with positive feedback. This load behaves as a bi-stable flip-flop which may be set or reset depending upon the currents supplied from Q2 and Q3. Consider the situation where Q2 and Q3 are conducting equally, i.e. the input differential voltage is zero. Assuming Q7 to be conducting, it will be noted that the current from Q3 will be drawn by Q7 and Q8 will be in the "OFF" state. This allows the current from Q2 to drive Q7 in parallel with D4 and a small resistor. D4 and Q7 are identical geometry devices, so that the resistor causes Q7 to be biased at a higher level than D4. Thus Q7 will be able to conduct more current than Q3 provides. In order to reverse the state of Q7 and Q8, it will be necessary to reduce the current from Q2 below that provided by Q3 by an amount which is established by R1. It can be shown that this requires a differential input to Q1 and Q4, of approximately 15 mV. Since the circuit is symmetrical, the threshold voltage to reverse the state is 15 mV in the other direction. Thus the input amplifier has built-in hysteresis at ±15 mV. This provides clean switching where noise may be present on the input signal, and allows total rejection of noise below this amplitude where there is no input signal.

### Charge Pump

The charge pump is composed of Q12 through Q32. R4, R5, and R6 provide reference voltages equal to 1/4 and 3/4 of supply voltage to Q12 and Q13. When Q10 turns "ON" or "OFF," the base voltage at Q16 changes by an amount equal to the voltage across R5, that is 1/2 $V_{CC}$. A capacitor connected between Pin 2 and ground is either charged by Q21 or discharged by Q22 until its voltage matches that on the base of Q16. When the voltage on Q16 base goes low, Q16 turns "ON," which results in Q18 and Q26 turning on, which causes the current, sourced by Q19 and Q20, to be shunted to ground. Thus Q21 is unable to charge pin 2. Meanwhile, Q27 and Q30 are turned off permitting the 200μA sourced by Q28 and Q29 to enter the emitters of Q31 and Q32 respectively. The current from Q31 is mirrored by Q22 through Q24 resulting in a 200μA discharge current through pin 2. The external capacitor on pin 2 is thus




*Note: This connection made on LM2907-8 and LM2917-8 only.
**Note: This connection made on LM2917 and LM2917-8 only.
Note: Pin numbers refer to 14-pin package.

**FIGURE 2. Equivalent Schematic Diagram**

discharged at a constant rate until it reaches the new base voltage on Q16. The time taken for this discharge to occur is given by:

$$t = \frac{CV}{I} \quad (1)$$

where C = capacitor on pin 2
V = change in voltage on Q16 base
I = current in Q22

During this time, Q32 sources an identical current into pin 3. A capacitor connected to pin 3 will thus be charged by the same current for the same amount of time as pin 2. When the base voltage on Q16 goes high, Q18 and Q26 are turned off while Q27 and Q3 are turned "ON." In these conditions, Q21 and Q25 provide the currents to charge the capacitors on pins 2 and 3 respectively. Thus the charge required to return the capacitor on pin 2 to the high level voltage is duplicated and used to charge the capacitor connected to pin 3. Thus in one cycle of input the capacitor on pin 3 gets charged twice with a charge of CV.

Thus the total charge pumped into the capacitor on pin 3 per cycle is:

$$Q = 2\,CV \quad (2)$$

Now, since $V = V_{CC}/2$

then $$Q = CV_{CC} \quad (3)$$

A resistor connected between pin 3 and ground causes a discharge of the capacitor on pin 3, where the total charge drained per cycle of input signal is equal to:

$$Q1 = \frac{V3 \cdot T}{R}$$

where V3 = the average voltage on pin 3
T = period of input signal
R = resistor connected to pin 3

In equilibrium Q = Q1

$$\text{i.e., } CV_{CC} = \frac{V3 \cdot T}{R} \quad (4)$$

and $$V3 = V_{CC} \cdot \frac{RC}{T} \quad (5)$$

or $$V3 = V_{CC} \cdot R \cdot C \cdot f \quad (6)$$

where f = input frequency

**Op Amp/Comparator**

Again referring to *Figure 2,* the op amp/comparator includes Q35 through Q45. A PNP input stage again provides input common-mode voltages down to zero, and if pin 8 is connected to $V_{CC}$ and the output taken from pin 5, the circuit behaves as a conventional, unity-gain-compensated operational amplifier. However, by allowing alternate connections of Q45 the circuit may be used as a comparator in which loads to either $V_{CC}$ or ground may be switched. Q45 is capable of sinking 50 mA. Input bias current is typically 50 nA, and voltage gain is typically 200V/mV. Unity gain slew rate is 0.2V/$\mu$s. When operated as a comparator Q45 emitter will switch at the slew rate, or the collector of Q45 will switch at that rate multiplied by the voltage gain of Q45, which is user selectable.

**Active Zener Regulator**

The optional active zener regulator is also shown in *Figure 2.* D8 provides the voltage reference in conjunction with Q33. As the supply voltage rises, D8 conducts and the base voltage on Q33 starts to rise. When Q33 has sufficient base voltage to be turned "ON," it in turn causes Q34 to conduct current from the power source. This reduces the current available for D8 and the negative feedback loop is thereby completed. The reference voltage is therefore the zener voltage on D8 plus the emitter base voltage of Q33. This results in a low temperature coefficient reference voltage.

**Input Levels and Protection**

In 8-pin versions of the LM2907, LM2917, the non-inverting input of the op amp/comparator is connected to the output of the charge pump. Also, one input to the input hysteresis amplifier is connected to ground. The other input (pin 1) is then protected from transients by, first a 10 k$\Omega$ series resistor, R3 *(Figure 2)* which is located in a floating isolation pocket, and secondly by clamp diode D1. Since the voltage swing on the base of Q1 is thus restricted, the only restriction on the allowable voltage on pin 1 is the breakdown voltage of the 10 k$\Omega$ resistor. This allows input swings to ±28V. In 14-pin versions the link to D1 is opened in order to allow the base of Q1 to be biased at some higher voltage.

Q5 clamps the negative swing on the base of Q1 to about 300 mV. This prevents substrate injection in the region of Q1 which might otherwise cause false switching or erroneous discharge of one of the timing capacitors.

The differential input options (LM2907-14, LM2917-14), give the user the option of setting his own input switching level and still having the hysteresis around that level for excellent noise rejection in any application.

**HOW TO USE IT**

**Basic f to V Converter**

The operation of the LM2907, LM2917 series is best understood by observing the basic converter shown in *Figure 3.* In this configuration, a frequency signal is applied to the input of the charge pump at pin 1. The voltage appearing at pin 2 will swing between two values which are approximately 1/4 ($V_{CC}$) $-V_{BE}$ and 3/4 ($V_{CC}$) $- V_{BE}$. The voltage at pin 3 will have a value equal to $V_{CC} \cdot f_{IN} \cdot C1 \cdot R1 \cdot K$, where K is the gain constant (normally 1.0).

The emitter output (pin 4) is connected to the inverting input of the op amp so that pin 4 will follow pin 3 and provide a low impedance output voltage proportional to input frequency. The linearity of this voltage is typically better than 0.3% of full scale.

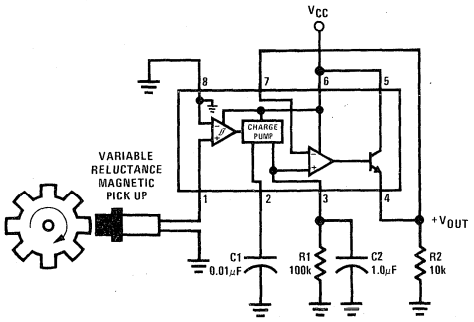



**FIGURE 3. Basic f to V Converter**

### Choosing R1, C1 and C2

There are some limitations on the choice of R1, C1 and C2 *(Figure 3)* which should be considered for optimum performance. C1 also provides internal compensation for the charge pump and should be kept larger than 100 pF. Smaller values can cause an error current on R1, especially at low temperatures. Three considerations must be met when choosing R1.

First, the output current at pin 3 is internally fixed and therefore V3 max, divided by R1, must be less than or equal to this value.

$$\therefore \quad R1 \geq \frac{V3\ max}{I_{3MIN}}$$

where V3 max is the full scale output voltage required
$I_{3MIN}$ is determined from the data sheet (150μA)

Second, if R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Finally, ripple voltage must be considered, and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1, C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \cdot \frac{C1}{C2} \left(1 - \frac{V_{CC} \cdot f_{IN} \cdot C1}{I_2}\right) \text{ p-p}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes $V_{OUT}$ to stabilize at a new frequency increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be chosen carefully. R1 should be selected according to the following relationship:

C1 is selected according to:

$$C1 = \frac{V3\ Full\ Scale}{R1 \cdot V_{CC} \cdot f_{FULL\ SCALE}}$$

Next decide on the maximum ripple which can be accepted and plug into the following equation to determine C2:

$$C2 = \frac{V_{CC}}{2} \cdot \frac{C1}{V_{RIPPLE}} \left(1 - \frac{V_3}{2}\right)$$

The kind of capacitor used for timing capacitor C1 will determine the accuracy of the unit over the temperature range. *Figure 15* illustrates the tachometer output as a function of temperature for the two devices. Note that the LM2907 operating from a fixed external supply has a negative temperature coefficient which enables the device to be used with capacitors which have a positive temperature coefficient and thus obtain overall stability. In the case of the LM2917 the internal zener supply voltage has a positive coefficient which causes the overall tachometer output to have a very low temperature coefficient and requires that the capacitor temperature coefficient be balanced by the temperature coefficient of R1.

### Using Zener Regulated Options (LM2917)

For those applications where an output voltage or current must be obtained independently of the supply voltage variations, the LM2917 is offered. The reference typically has an 11Ω source resistance. In choosing a dropping resistor from the unregulated supply to the device note that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages, there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9V to 16V, a resistance of 470Ω will minimize these zener voltage variations to 160 mV. If the resistor goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation. Take care also that the power dissipation of the IC is not exceeded at higher supply voltages. *Figure 4* shows suitable dropping resistor values.

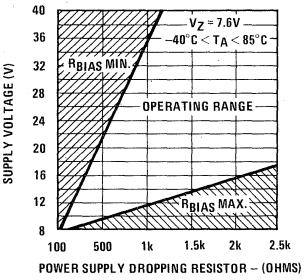



**FIGURE 4. Zener Regular Bias Resistor Range**

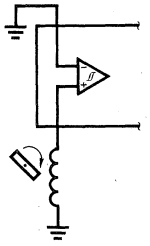
### Input Interface Circuits

The ground referenced input capability of the LM2907-8 allows direct coupling to transformer inputs, or variable reluctance pickups. *Figure 5(a)* illustrates this connection. In many cases, the frequency signal must be obtained from another circuit whose output may not go below ground. This may be remedied by using ac coupling to the input of the LM2907 as illustrated in *Figure 5(b)*. This approach is very suitable for use with phototransistors for optical pickups. Noisy signal sources may be coupled as shown in *Figure 5*(c). The signal is bandpass filtered. This can be used, for example, for tachometers operating from breakerpoints on a conventional Kettering

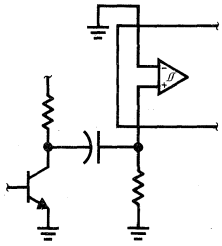
ignition system. Remember that the minimum input signal required by the LM2907 is only 30 mVp-p, but this signal must be able to swing at least 15 mV on either side of the inverting input. The maximum signal which can be applied to the LM2907 input, is ±28V. The input bias current is a typically 100 nA. A path to ground must be provided for this current through the source or by other means as illustrated. With 14-pin package versions of LM2907, LM2917, it is possible to bias the inverting input to the tachometer as illustrated in *Figure 5(d)*. This enables the circuit to operate with input signals that do not go to ground, but are referenced at higher voltages. Alternatively, this method increases the noise immunity where large signal levels are available but large noise signals on ground are also present. To take full advantage of the common-mode rejection of the input differential stage, a balanced bias configuration must be provided. One such circuit is illustrated in *Figure 5(e)*. With this arrangement, the effective common-mode rejection may be virtually infinite, owing to the input hysteresis.

**Output Configurations**

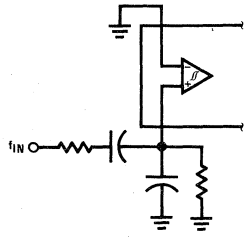
LM2907, LM2917 series devices incorporate an unusually flexible op amp/comparator device on-chip for interfacing with a wide variety of loads. This flexibility results from the availability of both the collector and emitter of the output transistor which is capable of driving up to 50 mA of load current. When the non-inverting input is higher than the inverting input, this output transistor is turned "ON." It may be used to drive loads to either the positive or the negative supply with the emitter or collector respectively connected to the other supply. For example, *Figure 6(a)*, a simple speed switch can be constructed in which the speed signal derived from the frequency to voltage converter is compared to a reference derived simply by a resistive divider from the power supply. When the speed signal exceeds the reference, the output transistor turns on the light emitting diode in the load. A small current limiting resistor should be placed in series with the output to protect the LED and the output transistor.



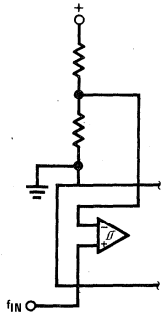
(a) Ground Referenced Inputs



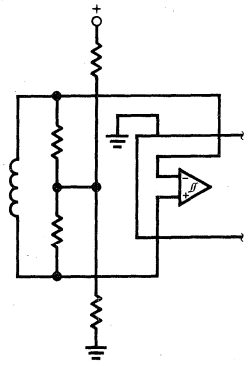
(b) AC Coupled Input




(c) Bandpass Filtered Input Reduces Noise

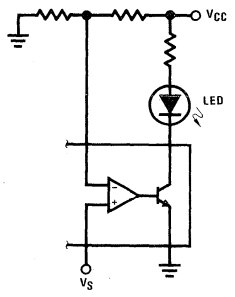



(d) Above Ground Sensing

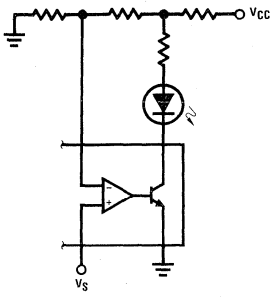



(e) High Common-Mode Rejection Input Circuit

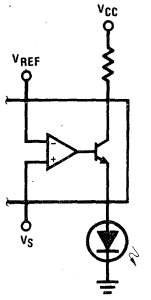
**FIGURE 5. Tachometer Input Configurations**



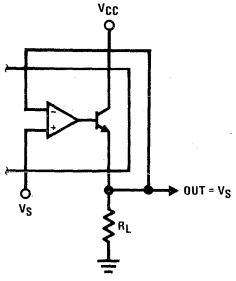

(a) Switching an LED



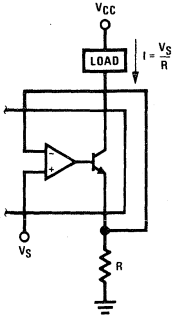

(b) Adding Hysteresis to LED Switch



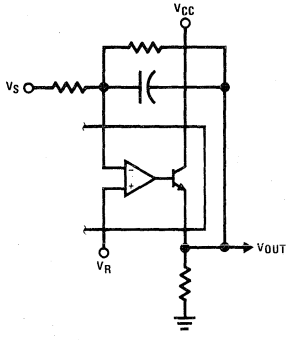

(c) Switching a Grounded Load




(d) Voltage Follower




(e) Voltage to Current Converter




(f) Integrator

**FIGURE 6. Output Configurations**

This circuit has no hysteresis in it, i.e., the turn "ON" and turn "OFF" speed voltages are essentially equal. In cases where speed may be fluctuating at a high rate and a flashing LED would be objectionable, it is possible to incorporate hysteresis so that the switch-on speed is above the switch-off speed by a controlled amount. Such a configuration is illustrated in *Figure 6(b)*. *Figure 6(c)* shows how a grounded load can also be switched by the circuit. In this case, the current limiting resistor is placed in the collector of the power transistor. The base current of the output transistor (Q45) is limited by a 5 kΩ base resistor (see *Figure 2*). This raises the output resistance so that the output swing will be reduced at full load.

The op amp/comparator is internally compensated for unity gain feedback configurations as in *Figure 6(d)*. By directly connecting the emitter output to the non-inverting input, the op amp may be operated as a voltage follower. Note that a load resistor is required externally. The op amp can also be operated, of course, as an amplifier, integrator, active filter, or in any other normal operational amplifier configuration.

One unique configuration which is not available with standard operational amplifiers, is shown in *Figure 6(e)*. Here the collector of the output transistor is used to drive a load with a current which is proportional to the input voltage. In other words, the circuit is operating as a voltage to current converter. This is ideal for driving remote signal sensors and moving coil galvanometers. *Figure 6(f)* shows how an active integrator can be used to provide an output which falls with increasing speed.

These are the basic configurations obtainable with the op amp/comparator. Further combinations can be seen in the applications shown in Part II of this application note.

### Transient Protection

Many application areas use unregulated power supplies which tend to expose the electronics to potentially damaging transients on the power supply line. This is particularly true in the case of automotive applications where two such transients are common.[1] First is the load dump transient. This occurs when a dead battery is being charged at a high current and the battery cable comes loose, so that the current in the alternator inductance produces a positive transient on the line in the order of 60V to 120V. The second transient is called field decay. This occurs when the ignition is turned "OFF" and the energy stored in the field winding of the alternator causes a negative 75V transient on the ignition line.

*Figure 7* illustrates methods for protecting against these and other transients. *Figure 7(a)* shows a typical situation in which the power supply to the LM2907 can be provided through a dropping resistor and regulated by an external zener diode Z1, but the output drive is required to operate from the full available supply voltage. In this case, a separate protection zener Z2 must be provided if the voltage on the power supply line is expected to exceed the maximum rated voltage of the LM2907.

In *Figure 7(b)* and *7(c)*, the output transistor is required only to drive a simple resistive load and no secondary protection circuits are required. (Note that the dropping resistor to the zener also has to supply current to the output circuit). With the foregoing circuits, reverse supply protection is supplied by the forward biased zener diode. This device should be a low forward resistance unit in order to limit the maximum reverse voltage applied to the integrated circuit. Excessive reverse voltage on the IC can cause high currents to be conducted by the substrate diodes with consequent danger of permanent damage. Up to 1V negative can generally be tolerated. Versions with internal zeners may be self-protecting depending on the size of dropping resistor used. In applications where large negative voltage transients may be anticipated, a blocking diode may be connected in the power supply line to the IC as illustrated in *Figure 7(d)*. During these negative transients, the diode D1 will be reverse biased and prevent reverse currents flowing in the IC. If these transients are short and the capacitor C1 is large enough, then the power to the IC can be sustained. This is useful to prevent change of state or change of charge in systems connected to it.

**Temperature Ranges and Packaging Considerations**

The LM2907, LM2917 series devices are specified for operation over the temperature range −40°C to +85°C.

The devices are normally packaged in molded epoxy, dual-in-line packages. Other temperature ranges and other packages are available to special order. For reliability requirements beyond those of normal commercial application where the cost of military qualification is not bearable, other programs are available such as B+.

## PART II – APPLICATIONS

### INTRODUCTION

The LM2907, LM2917 series devices were designed not only to perform the basic frequency to voltage function required in many systems, but also to provide the input and output interface so often needed, so that low cost implementations of complete functions are available.

The concept of building blocks requires that a function be performed in the same way as it can be mathematically defined. In other words, a frequency to voltage converter will provide an output voltage proportional to frequency which is independent of the input voltage or other input parameters, except the frequency. In the same way, the output voltage will be zero when the input frequency is zero. These features are built into the LM2907.

Applications for the device range from simple speed switch for anti-pollution control device functions in automobiles, to motor speed controls in industrial

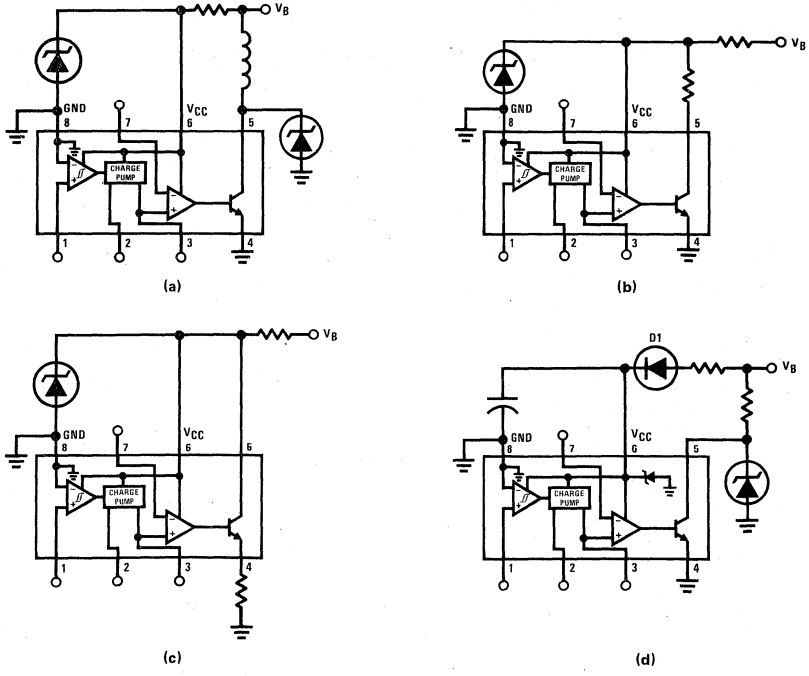



**FIGURE 7. Transient Protection Schemes**

applications. The applications circuits which follow are designed to illustrate some of the capabilities of the LM2907. In most cases, alternative input or output configurations can be mixed and matched at will and other variations can be determined from the description in Part I of this application note. For complete specifications, refer to the data sheet.

**Speed Switches**

Perhaps the most natural application of the LM2907 is in interfacing with magnetic pickups, such as the one illustrated in *Figure 8* to perform speed switching functions. As an example, New York taxies are required to change the intensity of the warning horn above and below 45 mph. Other examples include an over-speed warning, where a driver may set the desired maximum speed and have an audible or visual warning of speeds in excess of that level. Many anti-pollution devices included on several recent automobile models have included a speed switch to disable the vacuum advance function until a certain speed is attained[2]. A circuit which will perform these kind of functions is shown in *Figure 9*. A typical magnetic pickup for automotive applications will provide a thousand pulses per mile so that at 60 mph the incoming frequency will be 16.6 Hz. If the reference level on the comparator is set by two equal resistors R1 and R2 then the desired value of C1 and R1 can be determined from the simple relationship:

$$\frac{V_{CC}}{2} = V_{CC} \cdot C1 \cdot R1 \cdot f.$$

or $$C1R1f = 0.5$$

and hence $$C1\,R1 = 0.03$$

From the RC selection chart in *Figure 10* we can choose suitable values for R1 and C1. Examples are 100 kΩ and 0.3μF. The circuit will then switch at approximately 60 mph with the stated input frequency relationship to speed. To determine the ripple voltage refer back to the equation for ripple voltage (under "Choosing R1, C1 and C2"). From this we can determine that there will be about 10 mV of ripple at the switching level. To prevent this from causing chattering of the load a certain amount of hysteresis is added by including R3. This will provide typically 1% of supply as a hysteresis or 1.2 mph in the example. Note that since the reference to the comparator is a function of supply voltage as is the output from the charge pump there is no need to regulate the power supply. The frequency at which switching occurs is independent of supply voltage.

In some industrial applications it is useful to have an indication of past speed excesses, for example in notifying the need for checking of bearings. The LM2907 can be made to latch until the power supply is turned "OFF" in the case where the frequency exceeds a certain limit,

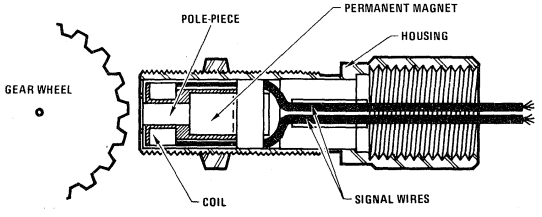



**FIGURE 8. Typical Magnetic Pickup**

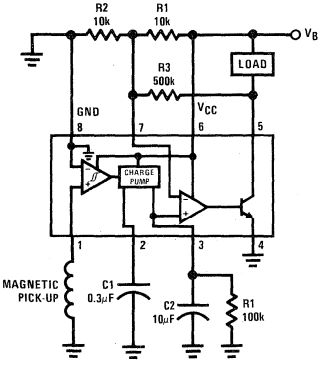



**FIGURE 9. Simple Speed Switch Load is Energized when $f_{IN} > \frac{1}{2C1\,R1}$**

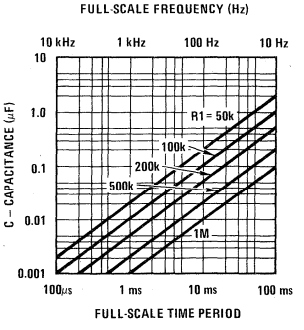
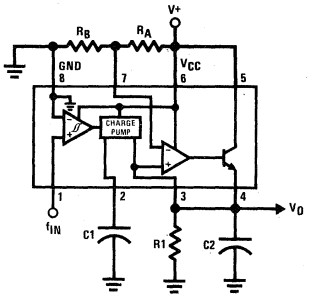
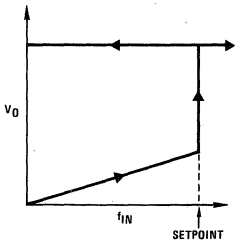



**FIGURE 10. RC Selection Chart**

by simply connecting the output transistor emitter back to the non-inverting input of the comparator as shown in *Figure 11.* It can also serve to shut off a tape recorder or editing machine at the end of a rewind cycle. When the speed suddenly increases, the device will sense the condition and shut down the motor.




$$V_O = F_{IN}\ V+\ R1\ C1$$

$$\text{SETPOINT} = V+ \frac{RB}{RB + RA}$$

Latchup occurs when

$$F_{IN} = \frac{RB}{RA + RB} \frac{1}{R1\,C1}$$

Independent of V+!

**FIGURE 11. Overspeed Latch**

### Analog Displays

The LM2907, LM2917 series devices are particularly useful for analog display of frequency inputs. In situations where the display device is a moving coil instrument the advantages of the uncommitted output transistor can be realized by providing a current drive to the meter. This avoids temperature tracking problems with the varying meter resistance and enables high resistance instruments to be driven accurately with relatively large voltages as illustrated in *Figure 12.* The LM2917 version is employed here to provide a regulated current to the instrument. The onboard 7.6V zener is compatible with car and boat batteries and enables the moving coil instrument to employ the full battery voltage for its deflection. This enables high torque meters to be used. This is particularly useful in high vibration environments such as boats and motorcycles. In the case of boats, the most common speed pickup for the knot meter employs a rotating propeller driving a magnetic pickup device. Meteorologists employ a large number of anemometers for measuring wind velocities and these are frequently coupled by a magnetic pickup. In examples like these, where there is frequently a large distance between the display device and the sensor, the configuration of *Figure 13* can be usefully employed to cut down on the number of wires needed. Here the output current is conducted along the supply line so that a local current sensing device in the supply line can be used to get a direct reading of the frequency at the remote location where the electronics may also be situated. The small zero speed offset due to the device quiescent current may be compensated by offsetting the zero on the display device. This also permits one display device to be shared between several inputs.

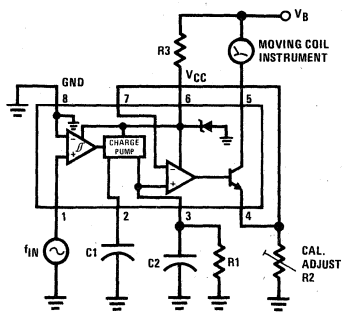
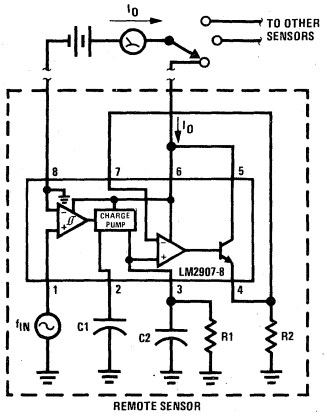



**FIGURE 12. Analog Display of Frequency**



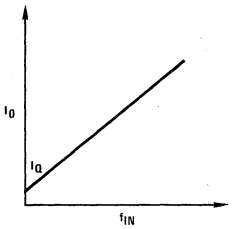




**FIGURE 13. Two Wire Remote Speed Sensor**

### Automotive Tachometer

Not all inputs are derived from variable reluctance magnetic pickups; for example, in spark ignition engines the tachometer is generally driven from the spark coil. An interface circuit for this situation is shown in

*Figure 14*. This tachometer can be set up for any number of cylinders by linking the appropriate timing resistor as illustrated. A 500Ω trim resistor can be used to set up final calibration. A protection circuit composed of a 10Ω resistor and a zener diode is also shown as a safety precaution against the transients which are to be found in automobiles.

### Motor Speed Controls

DC motors with or without brushes can be purchased with ac tachometer outputs already provided by the manufacturer.[3] With these motors in combination with the LM2907, a very low cost speed control can be constructed. In *Figure 16* the most simple version is illustrated where the tachometer drives the non-inverting input of the comparator up towards the preset reference level. When that level is reached, the output is turned off and the power is removed from the motor. As the motor slows down, the voltage from the charge pump output falls and power is restored. Thus speed is maintained by operating the motor in a switching mode. Hysteresis can be provided to control the rate of switching. An alternative approach which gives proportional control is shown in *Figure 17*. Here the charge pump integrator is shown in a feedback connection around the operational amplifier. The output voltage for zero speed is equal to the reference voltage set up on the potentiometer on the non-inverting input. As speed increases,

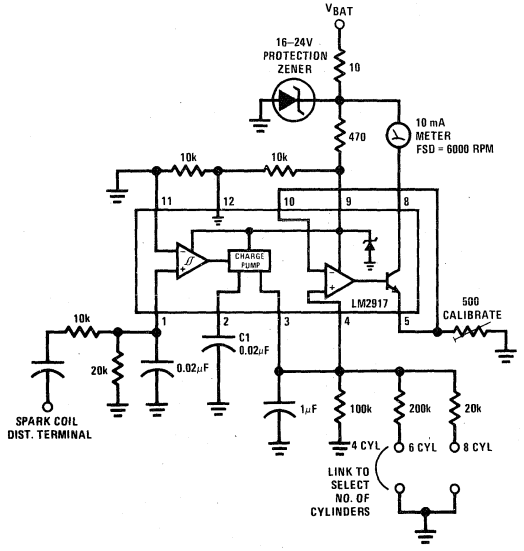



**FIGURE 14. Gasoline Engine Tachometer**

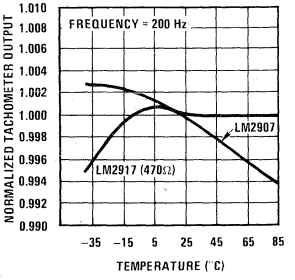



**FIGURE 15. Normalized Tachometer Output vs Temperature**

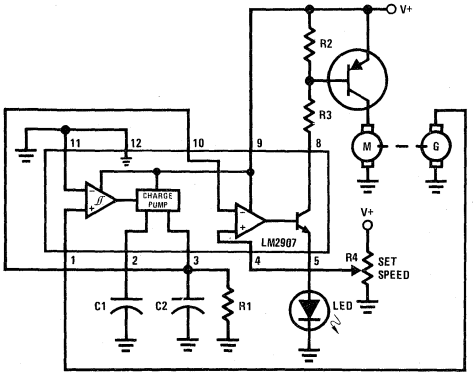



**FIGURE 16. Motor Speed Control**

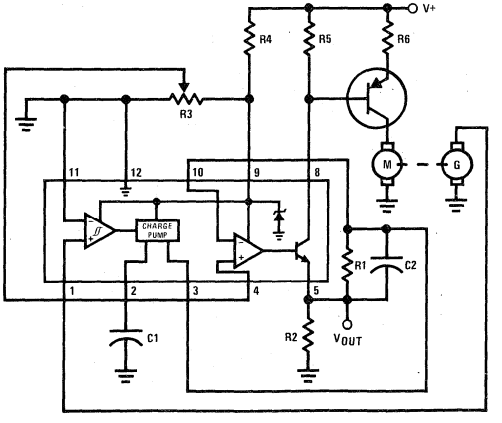



**FIGURE 17. Motor Speed Control with Proportional Drive**

the charge pump puts charge into capacitor C2 and causes the output $V_{OUT}$ to fall in proportion to speed. The output current of the op amp transistor is used to provide an analog drive to the motor. Thus as the motor speed approaches the reference level, the current is proportionately reduced to the motor so that the motor gradually comes up to speed and is maintained without operating the motor in a switching mode. This is particularly useful in situations where the electrical noise generated by the switching mode operation is objectionable. This circuit has one primary disadvantage in that it has poor load regulation. A third configuration is shown in *Figure 18.* This employs an LM2907-8 acting as a shunt mode regulator. It also features an LED to indicate when the device is in regulation.

**Position Sensing**

In addition to their use to complete tachometer feedback loops, used in position transducer circuits, the LM2907, LM2917 devices can also be used as position transducers. For example, the timing resistor can be removed from pin 3 so that the output current produces a staircase instead of a fixed dc level. If the magnetic pickup senses passing notches or items, a staircase signal is generated which can then be compared with a reference to initiate a switching action when a specified count is reached. For example, *Figure 19* shows a circuit which will count up a hundred input pulses and then switch on the output stage. Examples of this application can be found in automated packaging operations or in line printers.

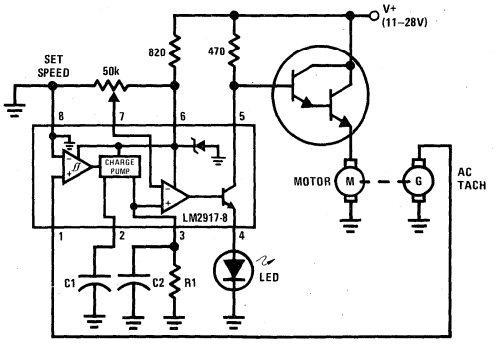



**FIGURE 18. Motor Speed Control**

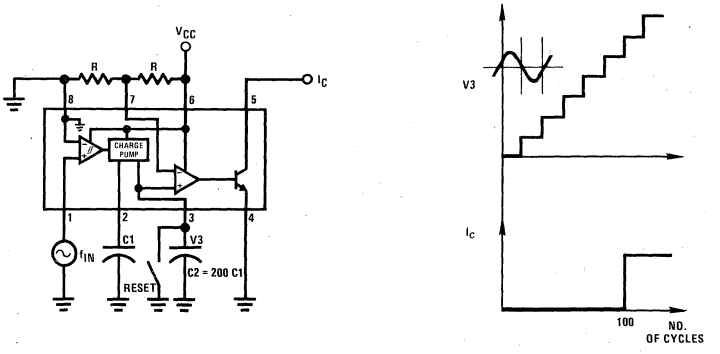



**FIGURE 19. Staircase Counter**

The output of the tachometer is proportional to the product of supply voltage, input frequency, a capacitor and a resistor. Any one of these may be used as the input variable or they may be used in combination to produce multiplication. An example of a capacitive transducer is illustrated in *Figure 20,* where a fixed input frequency is employed either from the 60 Hz line as a convenient source or from a stable oscillator. The capacitor is a variable element mechanically coupled to the system whose position is to be sensed. The output is proportional to the capacitance value, which can be arranged to have any desired relationship to the mechanical input by suitable shaping of the capacitor electrodes.

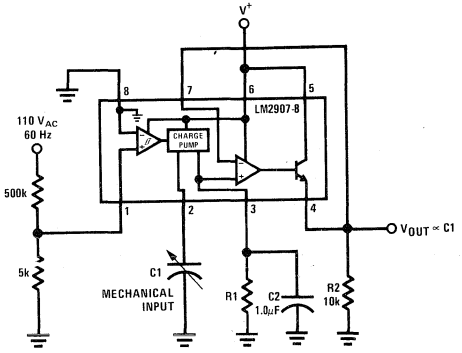



**FIGURE 20. Capacitive Transducer**

## Analog Systems Building Block

The LM2907, LM2917 series characterize systems building block applications by the feature that the output from the device is proportional only to externally programmed inputs. Any or all of these inputs may be controlled inputs to provide the desired output. For example, in *Figure 20* the capacitance transducer can be operated as a multiplier. In flow measurement indicators, the input frequency can be a variable depending on the flow rate, such as a signal generated from a paddle wheel, propeller or vortex sensor[4]. The capacitor can be an indication of orifice size or aperture size, such as in a throttle body. The product of these two will indicate volume flow. A thermistor could be added to R1 to convert the volume flow to mass flow. So a combination of these inputs, including control voltage on the supply, can be used to provide complex multiplicative analog functions with independent control of the variables.

Phase-locked loops (PLL) are popular today now that low cost monolithic implementations are available off the shelf. One of their limitations is the narrow capture range and hold-in range. The LM2907 can be employed as a PLL helper. The configuration is shown in *Figure 21*. The LM2907 here serves the function of a frequency-to-voltage converter which puts the VCO initially at approximately the right frequency to match the input frequency. The phase detector is then used to close the gap between VCO and input frequency by exerting a control on the summing point. In this way, given proper

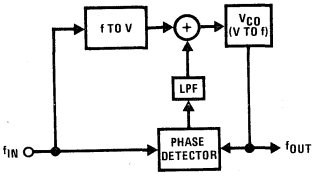



**FIGURE 21. Phase-Locked Loop Helper Added f to V Greatly Increases Capture and Hold Range**

tracking between the frequency-to-voltage converter and the VCO, (which is a voltage-to-frequency converter), a wide-range phase loop can be developed.

The linearity of voltage controlled oscillators can be improved by employing the LM2907 as a feedback control element converting the frequency back to voltage and comparing with the input voltage. This can often be a lower cost solution to linearizing the VCO than by working directly on the VCO itself in the open loop mode. The arrangement is illustrated in *Figure 22.*

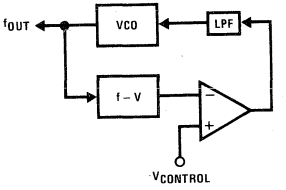
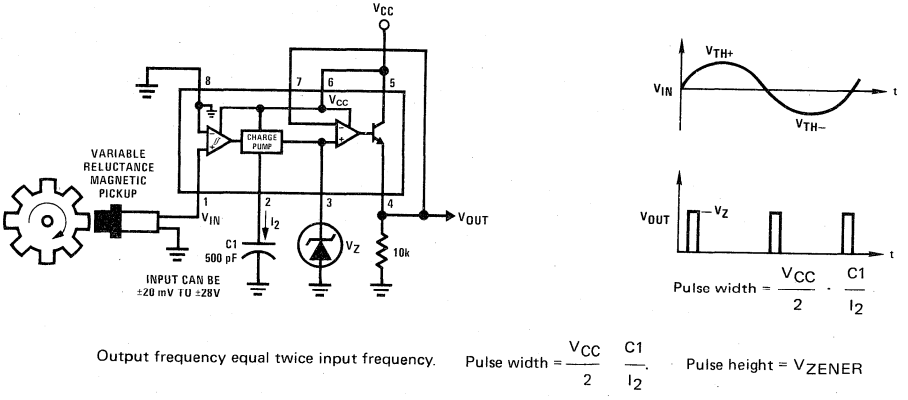



**FIGURE 22. Feedback Controlled VCO**

## Digital Interface

A growing proportion of the complex control systems today are being controlled by microprocessors and other digital devices. Frequently they require inputs to indicate position or time from some mechanical input. The LM2907 can be used to provide zero crossing datum to a digital system using the circuits illustrated in *Figure 23.* At each zero crossing of the input signal the charge pump changes the state of capacitor C1 and provides a one-shot pulse into the zener diode at pin 3. The width of this pulse is controlled by the internal current of pin 2 and the size of capacitor C1 as well as by the supply voltage. Since a pulse is generated by each zero crossing of the input signal we call this a "two-shot" instead of a "one-shot" device and this can be used for doubling the frequency that is presented to the microprocessor control system. If frequency doubling is not required and a square wave output is preferred, the circuit of *Figure 24* can be employed. In this case, the output swing is the same as the swing on pin 2 which is a swing of half supply voltage starting at 1 $V_{BE}$ below one quarter of supply and going to 1 $V_{BE}$ below three-quarters of supply. This can be increased up to the full output swing capability by reducing or removing the negative feedback around the op amp.

The staircase generator shown in *Figure 19* can be used as an A-D converter. A suitable configuration is shown in *Figure 25*. To start a convert cycle the processor generates a reset pulse to discharge the integrating capacitor C2. Each complete clock cycle generates a charge and discharge cycle on C1. This results in two steps per cycle being added to C2. As the voltage on C2 increases, clock pulses are returned to the processor. When the voltage on C2 steps above the analog input voltage the data line is clamped and C2 ceases to charge. The processor, by counting the number of clock pulses received after the reset pulse, is thus loaded with a digital measure of the input voltage. By making C2/C1 = 1024 an 8-bit A-D is obtained.




Output frequency equal twice input frequency. Pulse width = $\frac{V_{CC}}{2} \cdot \frac{C1}{I_2}$. Pulse height = $V_{ZENER}$

**FIGURE 23. "Two-Shot" Zero Crossing Detector**

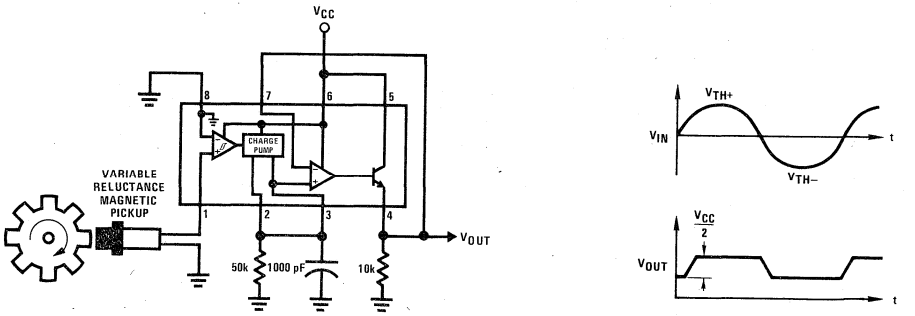



**FIGURE 24. Zero Crossing Detector and Line Drivers**

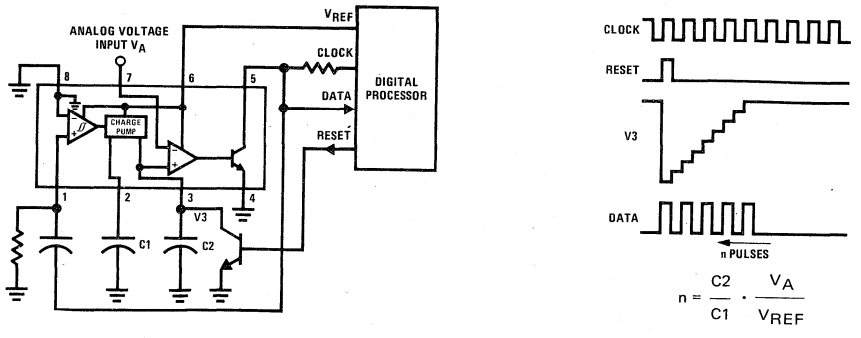
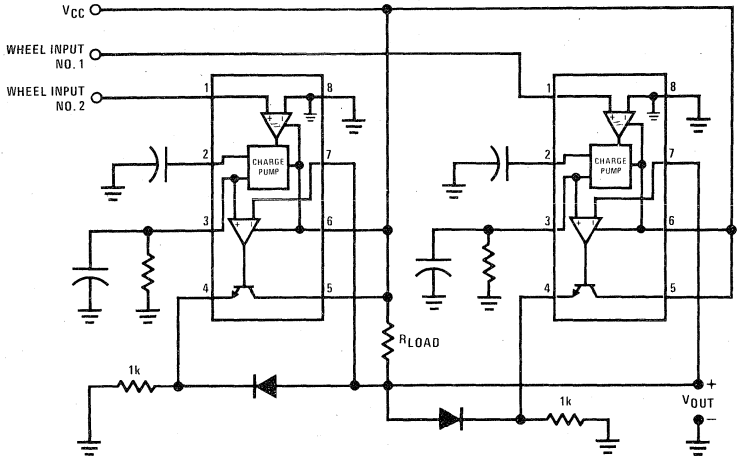
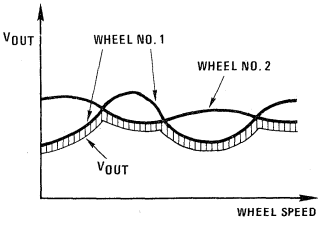



**FIGURE 25. A-D Converter**

### Anti-Skid Circuit Functions

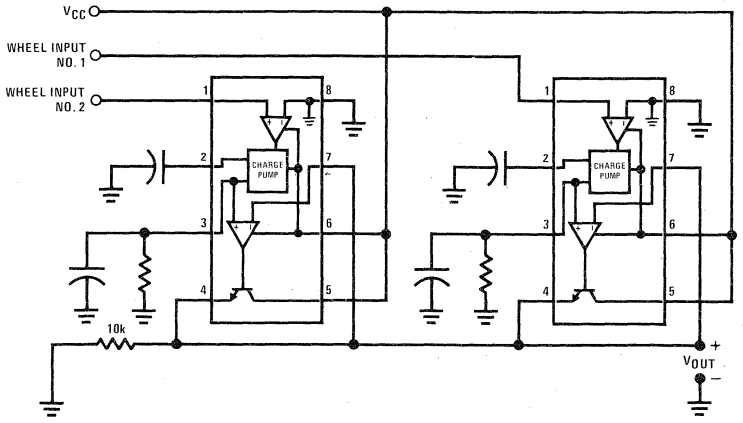
Motor Vehicle Standards 121 place certain stopping requirements on heavy vehicles which require the use of electronic anti-skid control devices.[5] These devices generally use variable reluctance magnetic pickup sensors on the wheels to provide inputs to a control module. One of the questions which the systems designer must answer is whether to use the average from each of the two wheels on a given axle or to use the lower of the two speeds or to use the higher of the two speeds. Each of the three functions can be generated by a single pair of LM2907-8 as illustrated in *Figures 26–28.* In *Figure 26* the input frequency from each wheel sensor is converted to a voltage in the normal manner. The op amp/comparator is connected with negative feedback with a diode in the loop so that the amplifier can only pull down on the load and not pull up. In this way, the outputs from the two devices can be joined together and the output will be the lower of the two input speeds. In *Figure 27* the output emitter of the onboard op amp provides the pullup required to provide a select-high situation where the output is equal to the higher of two speeds. The select average circuit in *Figure 28* saves components by allowing the two charge pumps to operate into a single RC network. One of the amplifiers is needed then to buffer the output and provide a low impedance output which is the average of the two input frequencies. The second amplifier is available for other applications.

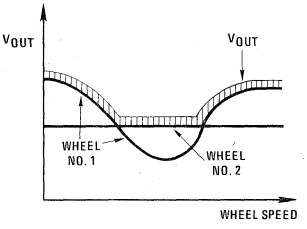



$V_{OUT}$ is proportional to the lower of the two input wheel speeds

**FIGURE 26. "Select-Low" Circuit**




$V_{OUT}$ is proportional to the higher of the two input wheel speeds

**FIGURE 27. "Select-High" Circuit**

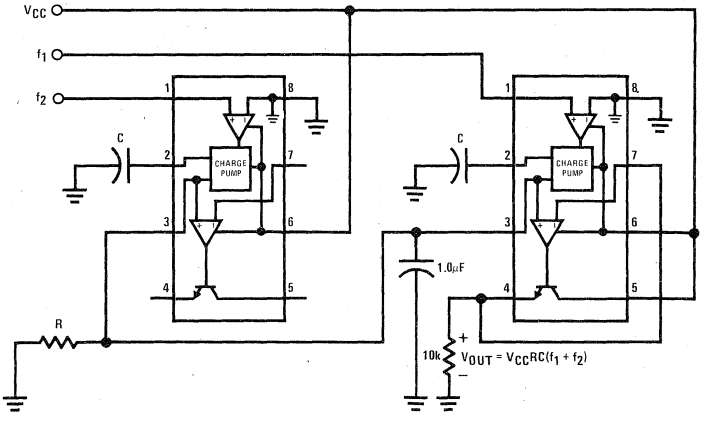



**FIGURE 28. "Select-Average" Circuit**

### Transmission and Clutch Control Functions

Electric clutches can be added to automotive transmissions to eliminate the 6% slip which typically occurs during cruise and which results in a 6% loss in fuel economy. These devices could be operated by a pair of LM2907's as illustrated in *Figure 29*. Magnetic pickups are connected to input and output shafts of the transmission respectively and provide frequency inputs $f_1$ and $f_2$ to the circuit. Frequency, $f_2$, being the output shaft speed, is also a measure of vehicle road speed. Thus the LM2907-8 No. 2 provides a voltage proportional to road speed at pin 3. This is buffered by the op amp in LM2907-8 No. 1 to provide a speed output $V_{OUT1}$ on pin 4. The input shaft provides charge pulses at the rate of $2f_1$ into the inverting node of op amp 2. This node has the integrating network R1, C3 going back to the output of the op amp so that the charge pulses are integrated and provide an inverted output voltage proportional to the input speed. Thus the output $V_{OUT2}$ is proportional to the difference between the two input frequencies. With these two signals— the road speed and the difference between road speed and input shaft speed—it is possible to develop a number of control functions including the electronic clutch and a complete electronic transmission control. (In the configuration shown, it is not possible for $V_{OUT2}$ to go below zero so that there is a limitation to the output swing in this direction. This may be overcome by returning R3 to a negative bias supply instead of to ground.)

## CONCLUSION

The applications presented in this note indicate that the LM2907, LM2917 series devices offer a wide variety of uses ranging from very simple low cost frequency to voltage conversion to complex systems building blocks. It is hoped that the ideas contained here have given suggestions which may help provide new solutions to old problems. Additional applications ideas are included in the data sheet, which should be referred to for all specifications and characteristics.

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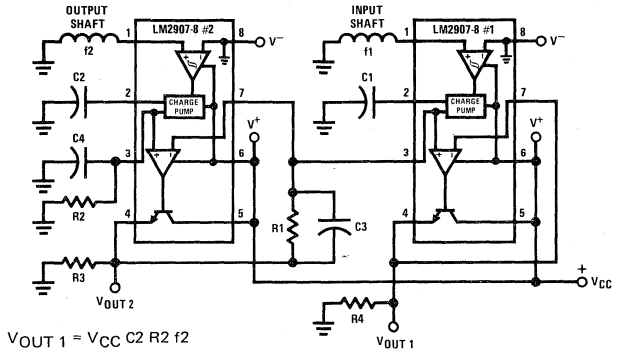
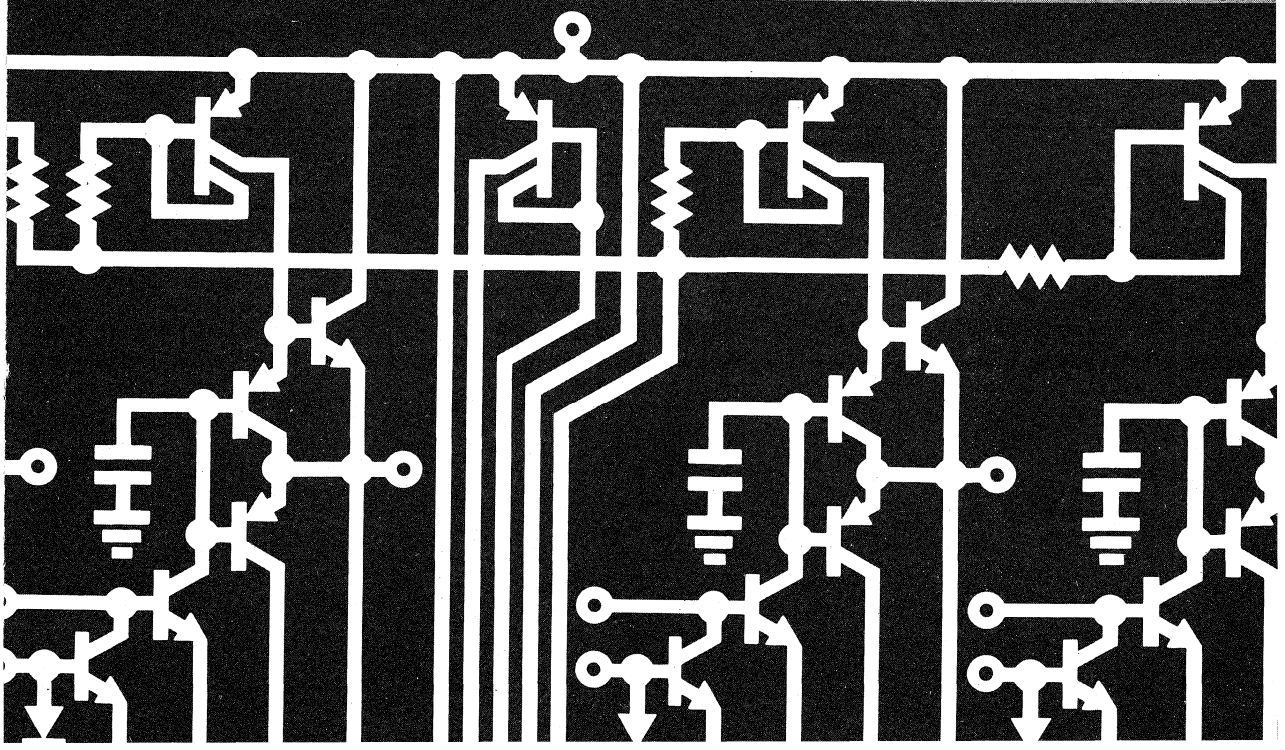



$V_{OUT\,1} = V_{CC}\ C2\ R2\ f2$

$V_{OUT\,2} = V_{CC}\ (C2\ R2\ f2 - C1\ R1\ f1)$

**FIGURE 29. Transmission or Clutch Control Functions**

# National Semiconductor
# LINEAR BRIEFS



Robert C. Dobkin
JUNE 1973

LINEAR BRIEF-21

# INSTRUMENTATIONAL AMPLIFIERS

## INTRODUCTION

One of the most useful analog subsystems is the true instrumentation amplifier. It can faithfully amplify low level signals in the presence of high common mode noise. This aspect of its performance makes it especially useful as the input amplifier of a signal processing system. Other features of the instrumentation amplifier are high input impedance, low input current, and good linearity.

It has never been easy to design a high performance instrumentation amplifier; however, the availability of high performance IC's considerably simplify the problem. IC op amps are available today that can give very low drifts as well as low bias currents; however, most of the circuits have some drawback.

The most commonly used instrumentation amplifier designs utilize either 2 or 3 op amps and several precision resistors. These are capable of excellent performance; however, for high performance they require very precisely matched resistors. The common mode rejection of these designs depends on resistor matching and overall gain. Since op amps are now available with exceedingly high CMRR this is no longer a problem. The CMRR of the instrumentation amplifier is approximately equal to half resistor mismatch plus the gain. For a 1% resistor mismatch the CMRR is limited to 46 dB plus the gain—referred to the input.

Referred to the output, the common mode error is independent of gain and fixed by the resistor mismatch. For 1% match the error is 0.5%, and for 0.1% match the error is 0.05%. These errors are not trivial in high precision systems.

An instrumentation amplifier is shown here that compares favorably with multiple op amp designs, yet does not require precisely matched resistors. Further, the design allows a single resistor to adjust the gain. In comparing this instrumentation amp to multiple op amp types there are of course some drawbacks. The gain linearity and accuracy are not as good as the multiple op amp circuits.

The errors appearing in multiple op amp circuits are independent of the output signal level. For example, a common mode error at the output of 0.5% of full scale is a 33% error if the desired output signal is only 1.5% of full scale. With the new circuit maximum errors at full scale output and the percentage of output error decreases at lower output levels.

Figure 1 shows a general purpose instrumentation amplifier optimized for wide bandwidth. It can provide gains from under 1 to over 1000 with a single resistor adjustment. Gain linearity is worst for unity-gain at 0.4%, and gain stability is better than 1.5% from −55°C to +125°C. Typically over a 0°C to +70°C range gain stability is 0.2%. Common mode rejection ratio is about 100 dB—independent of gain.

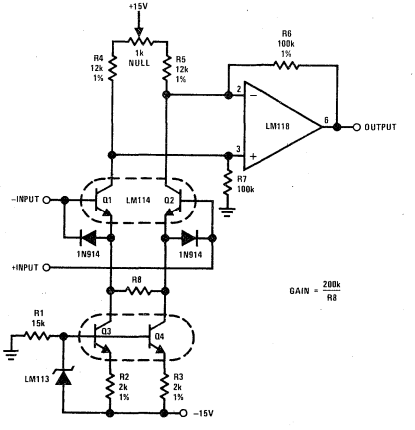



**FIGURE 1. Instrumentation Amplifier**

Transistor pair, Q1 and Q2, are operated open-loop as the input stage to give a floating, fully differential input. Current sources, Q3 and Q4, set the operating current of the input pair. To obtain good linearity the output current of Q3 and Q4 are set at about twice the current in R8 at full differential voltage. The temperature sensitivity of the transconductance of Q1 and Q2 is compensated by making their operating current directly proportional to absolute temperature. It has been shown that by biasing the base of transistor current sources at 1.22V, the output current varies as absolute temperature. The LM113 diode provide a constant 1.22V to the current sources. Both the compensated gm of Q1 and Q2 and the large degeneration from R8 give the amplifier stable gain over a wide temperature range.

In operation transistors Q1 and Q2 convert a differential input voltage to a differential output current at their collectors. This is fed into a standard differential amplifier to obtain a single ended output voltage. Since the diff amp does not see the common mode input voltage, 1% resistors are adequate. Gain is set by the ratio of R8 (plus the $r_e$ of Q1 and Q2) to the sum of R6 and R7.

As mentioned previously this circuit is optimized for wide bandwidth: however, it is easily modified for other applications. If low bias current is needed all resistors can be increased by a factor of 100 and an LM108 substituted for the LM318. Other possible improvements are cascoded current sources and a modified Darlington input stage.

Robert C. Dobkin
JUNE 1973

LINEAR BRIEF-22

# LOW DRIFT AMPLIFIERS

## INTRODUCTION

Since the introduction of the monolithic IC amplifier, there has been a continued improvement in dc accuracy. Bias currents have been decreased by five orders of magnitude over the past five years, Low offset voltage drift is also necessary in high-accuracy circuits. This is evidenced by the popularity of low-drift amplifier types as well as requests for selected low-drift op amps. However, little has been written about the problems associated with handling microvolt signals with a minimum of errors.

A very low-drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted. In many cases, the low drift of the op amp is completely swamped by external effects while the amplifier is blamed for the high drift.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Whenever dissimilar metals are joined, a thermocouple results. The voltage generated by the thermocouple is proportional to the temperature difference between the junction and the measurement end of the metal. This voltage can range between essentially zero and hundreds of microvolts per degree, depending on the metals used. In any system using integrated circuits, a minimum of three metals are found: copper, solder, and kovar (lead material of the IC).

Nominally, most parts of the circuit are at the same temperature. However, a small temperature gradient can exist across even a few inches—and this is a big problem with low level signals. Only a few degrees gradient can cause hundreds of microvolts of error. Two places where this shows up, generally, are the package-to-printed-circuit-board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

For example, a very low-drift amplifier was constructed and the output monitored over a 1-minute period. During the 1 minute it appeared to have input referred offset variations of ±5.0μV. Shielding the circuit from air currents reduced this to ±0.5μV. The 10μV error was due to thermal gradients across the circuit from air currents.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film, and some metal-film resistors can cause large thermocouple errors. Wirewound resistors of evenohm or managanin are best since they only generate about 2.0μV/°C referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low-drift stage electrically and thermally yields good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature, a gain error will result. For example, a gain-of-1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50μV error. Most precision resistors use different material for different ranges of resistor values. It is not unexpected that a resistor differing by a factor of 1000 does not track perfectly with temperature. For best results, ensure that the gain fixing resistors are of the same material or have tracking temperature coefficients.

It is appropriate to mention offset balancing as this can have a large effect on drift. Theoretically, the drift of a transistor differential amplifier depends on the offset voltage. For every millivolt of offset voltage the drift is 3.6μV/°C. Therefore, if the offset is nulled, the drift should be zero. When working with IC op amps, this is not the case. Other effects, such as second-stage drift and internal resistor TC, make the drift nontheoretical.

Certain types of amplifiers are optimized to have lower drift with offset balancing such as the LM121 and LM725. With this type of device offset, nulling improves the drift, and offset nulling should be used. Other types of devices, such as selected LM741's or LM308's, are selected for drift without offset nulling connected to the device. The addition of a balancing network changes the internal currents and thus changes the drift—probably for worse—so any offset balancing should be done at the input.

No matter which null network is applied highly stable resistors must be used. They should have low TC and track. Wirewound pots are usually a good choice. Finally, when the null network reduces a drift, the balancing of the amplifier as close to zero offset as possible minimizes the drift.

Testing low-drift amplifiers is also difficult. Standard drift testing techniques such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signal through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal. The circuit in Figure 1 will yield good results if well constructed.

## CONCLUSION

Low-drift amplifiers need extreme care to achieve reproducable low drift. Thermal and electrical shielding minimize thermocouple effects. Resistor choice is also important as they can introduce large errors. Careful attention to circuit layout offset balancing circuitry is also necessary.

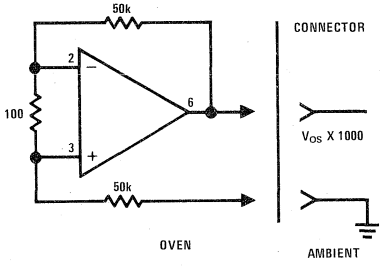



**FIGURE 1. Drift Measurement Circuit**

Robert C. Dobkin
JUNE 1973

LINEAR BRIEF-23

# PRECISE TRI-WAVE GENERATION

## INTRODUCTION

The simple Tri-wave generator has become an often used analog circuit. Tri-wave oscillators are more easily designed, require less circuitry, and are more easily stabilized than sine wave oscillators. Further, the highly linear output of todays Tri-wave generators make them useful in many "sweep" circuits and test equipment.

This article describes a triangle wave generator with an easily controlled peak-to-peak amplitude. The positive and negative peak amplitude is controllable to an accuracy of about ±0.01V by a dc input. Also, the output frequency and symmetry are easily adjustable.

## CIRCUIT DESCRIPTION

The Tri-wave oscillator consist of an integrator and two comparators—one comparator sets the positive peak and the other the negative peak of the Tri-wave. To understand the operation, assume that the output of the comparator is low (−5V). Then −5.0V is applied through R1 to the input of the integrator. The LM118 will integrate positive until its output is equal to the positive reference on pin 9 of the LM119. Since the comparator outputs are low, D1 is reverse biased and the full output of the integrator is applied to the non-inverting input of comparator A. As the integrator output crosses the positive reference, comparator A switches "plus" and latches "plus" from positive feedback through D1 and R4. Now the polarity of the current to the integrator has changed and the integrator starts ramping negative. When the output reaches the negative reference voltage, comparator B swings negative. This forces the output of comparator A negative, also, and stops the positive feedback through D1 from holding the comparators' outputs positive. Once the positive feedback loop is broken, the outputs of the comparators stay low. With the comparators outputs low the integrator ramps positive again.

The frequency of operation is dependent upon R1, C1 and the reference voltages. Frequency is given by:

$$F = \frac{5.0V}{2R1\ C1\ (V_{REF}{}^{+} - V_{REF}{}^{-})}$$

The maximum frequency of operation is limited by circuit delay to about 200 kHz. Also, the maximum difference in reference voltages is 5.0V.

## APPLICATIONS

Regulator or op amp testing is made easier with precise triangle waves. For example, IC voltage regulators are usually specified to operate over a certain input voltage range such as 7.0V to 25V. The Tri-wave generator can be set to deliver a 0.7V to 2.5V output. This output is then amplified by a factor of 10 by an op amp and used to sweep the regulator input over its operating range. With op amps, the generator can be used to sweep common mode voltages, power supply voltages, or even to test output swing. The output of the device can be displayed on an oscilloscope and performance monitored over the entire operating range.

Another application is a voltage controlled oscillator. Since the frequency depends on the input reference voltage, varying the reference varies the frequency. The useful VCO range is about 2

decades. The output is then taken from the comparators as the Tri-wave changes in amplitude.

Many sine wave oscillators use a non-linear network to convert triangle wave to sines. It is usually necessary to set triangle amplitude precisely for minimum distortion. If R1 is replaced by a pot, frequency can be varied over at least 10 to 1 range without affecting amplitude.

Symmetry is also easily adjustable. Current can be injected into the inverting input of the LM118 to change ramp time. The easiest way to achieve is to connect a 50 kΩ resistor from the inverting input of the LM118 to the arm of a 1 kΩ pot. The ends of the pot are connected across the supplies. Current from the resistor either adds or subtracts from the current through R1, changing the ramp time.

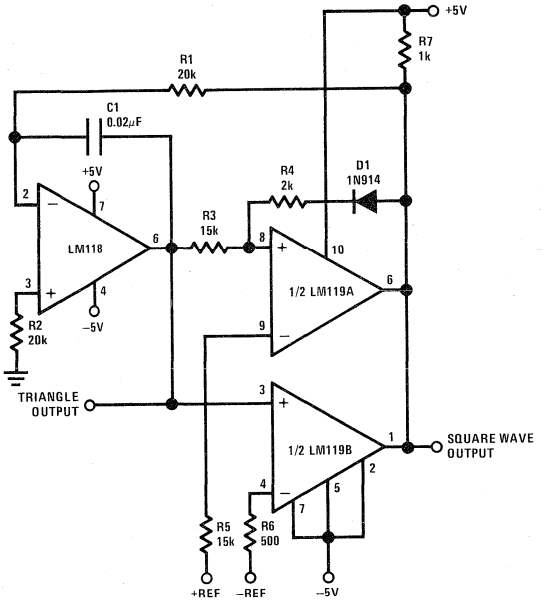



**FIGURE 1. Precision Tri-Wave Generator**

Robert C. Dobkin
JUNE 1973

LINEAR BRIEF-24

# VERSATILE IC PREAMP MAKES THERMOCOUPLE AMPLIFIER WITH COLD JUNCTION COMPENSATION

## INTRODUCTION

Accurate electronic temperature measurements are not simple. There exists a large array of temperature sensors; each with its own peculiarities. The major sensors are thermistors, resistance sensors, and thermocouples. (Diodes and transistors have been used but they are not normally sold for this purpose.) Thermistors are highly non-linear, making wide range measurements difficult. Resistance sensors are large, require a bridge, and tend to be relatively costly. Thermocouples are small, relatively linear, inexpensive, but require reference junction temperature compensation.

Thermocouples are made when wires of different metals are joined. A voltage is produced proportional to the temperature *difference* between the junction and the output ends of the wire. This voltage is the Seebeck coefficient and is usually specified in volts (or microvolts) per degree. Depending on the material, it can range from nearly zero to volts—for some semiconductors. Commercially available thermocouples produce an output of between 10$\mu$/°C and 50$\mu$V/°C.

Since the output voltage of thermocouples is proportional to temperature difference, the ambient temperature or measurement end of the thermocouple must be known. Alternatively, compensation can be applied for temperature changes. This is done either by terminating the thermocouple in a temperature controlled environment or with electrical compensation circuitry. The amplifier shown here provides a direct reading output of 10 mV/°C and automatically compensates for reference junction temperature changes. Further, calibration is relatively simple.

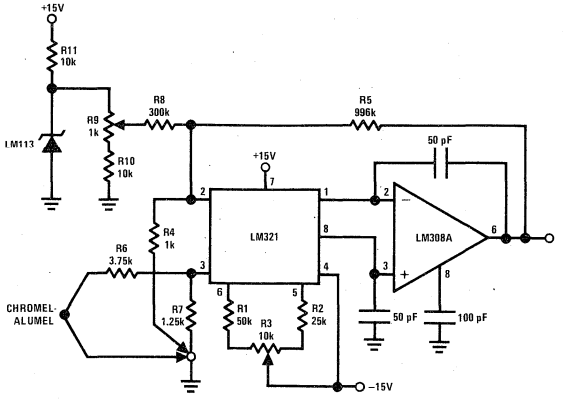
## CIRCUIT DESCRIPTION

An LM321 preamp is used in conjunction with an LM308A op amp to form a precision, low-drift, operational amplifier. The LM321 is specifically designed for use with general purpose op amps to obtain drifts of 1$\mu$V/°C. When the offset voltage is nulled, the drift is also nulled. There is a theoretical relationship between the offset voltage and drift when the offset is not nulled to zero. The drift of the amplifier is then used to compensate the thermocouple for ambient temperature variations. Drift given by:

$$\frac{d\,V_{os}}{dT} = \frac{V_{os}}{T}$$

where T is in degrees Kelvin.

Resistors R1, R2, and R3 set the operating current of the preamp, and R3 is used to adjust the offset. The offset and drift are amplified by the ratio of the feedback resistors R4 and R5 and appears at the output. R6 and R7 attenuate the thermocouple's output to 10$\mu$V/°C to match the amplifier drift and set the scale factor at 10 mV/°C. The LM113 provides a temperature stable reference for offsetting the output to read directly in degrees centigrade.



## CALIBRATION

Calibration is independent of thermocouple type; however, circuit values are for chromel alumel. R6 and R7 must be changed for different thermocouples. First, the thermocouple is replaced by a short of copper wire and the LM113 is shorted to ground. Then the offset is adjusted so the output reads the ambient temperature at 10 mV/°k—for 25°C this is 2.98V. The short across the LM113 is removed and R9 is adjusted for the correct output in degrees centigrade. Connect the thermocouple, and it's ready to go.

## PERFORMANCE

It should be mentioned that for stable performance, good construction techniques are necessary. Resistor R4, R6, and R7 should be wirewound so they contribute a minimum of error due to thermocouple effects from temperature gradients across the circuit. The entire circuit should be enclosed in a box with the end of the thermocouple terminated in the box near the LM321. This will minimize temperature gradients across the circuit and insure close thermal coupling between the LM321 and the reference end of the thermocouple.

Typically, the LM321 will track temperature changes with less than 0.03°C error per degree change. Self-heating of the LM321 will change its temperature by about 2°C; this is calibrated out initially. Reference and resistor drift can be expected to contribute about 0.02°C/°C. Of course, no compensation is made for nonlinearities of the thermocouple output voltage as a function of temperature. Over a wide measurement range with relatively stable ambient temperature, thermocouple error will be the major inaccuracy.

Robert C. Dobkin
JUNE 1973

LINEAR BRIEF-25

# TRUE RMS DETECTOR

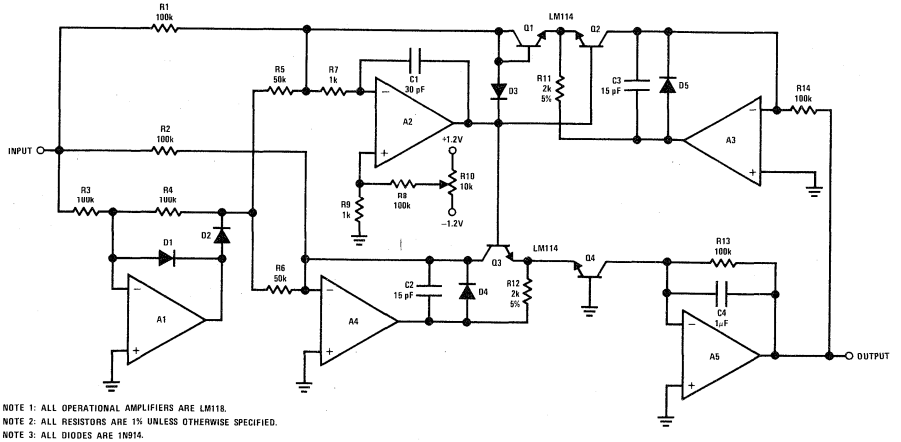
## INTRODUCTION

The op amp precision rectifier circuits have greatly eased the problems of ac to dc conversion. It is possible to measure millivolt ac signal with a dc meter with better than 1% accuracy. Inaccuracy due to diode turn-on and nonlinearity is eliminated, and precise rectification of low level signals is obtained.

Once the signal is rectified, it is normally filtered to obtain a smooth dc output. The output is proportional to the average value of the ac input signal, rather than the root mean square. With known input waveforms such as a sine, triangle, or square; this is adequate since there is a known proportionality between rms and average values. However, when the waveform is complex or unknown, a direct readout of the rms value is desirable.

The circuit shown will provide a dc output equal to the rms value of the input. Accuracy is typically 2% for a 20 $V_{P-P}$ input signal from 50 Hz to 100 kHz, although it's usable to about 500 kHz. The lower frequency is limited by the size of the filter capacitor. Further, since the input is dc coupled, it can provide the true rms equivalent of a dc and ac signal.

Basically, the circuit is a precision absolute value circuit connected to a one-quadrent multiplier/divider. Amplifier A1 is the absolute value amplifier and provides a positive input current to amplifiers A2 and A4 independent of signal polarity. If the input signal is positive, A1's output is clamped at −0.6V, D2 is reverse biased, and no signal flows through R5 and R6. Positive signal current flows through R1 and R2 into the summing junctions of A2 and A4. When the input is negative, an inverted signal appears at the output of A1 (output is taken from D2). This is summed through R5 and R6 with the input signal from R1 and R2. Twice the current flows through R5 and R6 and the net input to A2 and A4 is positive.




NOTE 1: ALL OPERATIONAL AMPLIFIERS ARE LM118.
NOTE 2: ALL RESISTORS ARE 1% UNLESS OTHERWISE SPECIFIED.
NOTE 3: ALL DIODES ARE 1N914.
NOTE 4: SUPPLY VOLTAGE ±15V.

Amplifiers A2 through A5 with transistors Q1 through Q4 form a log multiplier/divider. Since the currents into the op amps are negligible, all the input currents flow through the logging transistors. Assuming the transistors to be matched, the $V_{be}$ of Q4 is:

$$V_{be}\,(Q4) = V_{be}\,(Q1) + V_{be}\,(Q3) - V_{be}\,(Q2)$$

The $V_{be}$'s of these transistors are logarithmically proportional to their collector currents so

$$\log\,(I_{C4}) = \log\,(I_{C1}) + \log\,(I_{C3}) - \log\,(I_{C2})$$

$$\text{or} \quad I_{C4} = \frac{I_{C1}\,I_{C3}}{I_{C2}}$$

where $I_{C1}$, $I_{C2}$, $I_{C3}$, and $I_{C4}$ are the collector currents of transistors Q1 – Q4.

Since $I_{C1}$ equals $I_{C3}$ and is proportional to the input, the square of the input signal is generated. The square of the input appears as the collector current of Q4. Averaging is done by C4, giving a mean square output. The filtered output of Q4 is fed back to Q2 to perform continuous division where the divisor is proportional to the output signal for a true root mean square output.

Due to mismatches in transistors, it is necessary to calibrate the circuit. This is accomplished by feeding a small offset into amplifier A2. A 10V dc input signal is applied, and R10 is adjusted for a 10V dc output. The adjustment of R10 changes the gain of the multiplier by adding or subtracting voltage from the log voltages generated by the transistors. Therefore, both the resistor inaccuracies and $V_{be}$ mismatches are corrected.

For best results, transistors Q1 through Q4 should be matched, have high beta, and be at the same temperature. Since dual transistors are common, good results can be obtained if Q1, Q2 and Q3, Q4 are paired. They should be mounted in close proximity or on a common heat sink, if possible. As a final note, it is necessary to bypass all op amps with 0.1$\mu$F disc capacitors.

Robert C. Dobkin
OCTOBER 1973

LINEAR BRIEF-26

# SPECIFYING SELECTED OP AMPS AND COMPARATORS

It is not infrequent that commercially available standard IC components do not fit a particular application as they are specified. Often, however, a standard device selected to tighter limits will work. Thereupon, the IC manufacturer may be requested to supply a specially tested device.

The usual chain of events for a selected part is as follows: A specification is sent to the manufacturer with a request for quote. It is evaluated at the manufacturer for feasability, yield, and testing requirements. Then price and delivery are quoted to the customer. (Sometimes this route is shortened by calling the manufacturer—but this does not always work.)

Some insight into the IC design and IC testing can help both the manufacturer and IC user with special selection. Proper specification helps the manufacturer test as well as reduce IC costs. Ambiguous or impossible specs will usually result in the return of the specification to the customer for clarification and delay the delivery of the required parts.

The manufacturer is usually familiar with the product and production spread of devices. Further, test equipment is available for measuring parameters specified by the data sheet. In general, tighting selected data sheet parameters causes no problems. Further, no additional test equipment is needed for these tests—only the limits need be changed.

Perhaps one of the largest problems is over-specification. Each tightened specification reduces the number of parts available to the specification. For example, tighting several specifications at once could result in a 1% or 0.1% yield; to supply 100 parts at this yield, between 10,000 and 100,000 parts might have to be tested, and that gets expensive.

Of course, spec limits cannot be tightened to any desired value. This is due to limitations on the IC design. For example, bias current, which depends on transistor $H_{fe}$; can not be tightened by a factor of 10. This would require beta's 10 times higher than normal. Also, some specifications are not independent; such as op amp bandwidth and slew-rate.

## OP AMP AND COMPARATORS

These are the two most popular linear IC components requiring selection. Since many of the same specifications apply to both types of devices, they will be covered together. Table I shows the most common parameters tested on these devices and the relative difficulty of testing on high speed equipment.

Selected offset voltage and drift are very commonly specified parameters. Offset voltage and drift depends on component matching. In general, drift is not usually tested on general purpose devices; although, it may be guaranteed. Offset voltage can be correlated to drift, and the offset limits are set to guarantee the standard drift specification. Of course, very low drift devices must be 100% tested for drift, making them relatively expensive. Drift testing requires measuring the offset voltage at three or more temperatures; then subtracting

**TABLE I**

| PARAMETER | OP AMP | COMPARATOR | COST |
|---|---|---|---|
| Offset Voltage | Easy | Easy | Low |
| Offset Current | Easy | Easy | Low |
| Bias Current | Easy | Easy | Low |
| Supply Current | Easy | Easy | Low |
| Common Mode/Supply Rejection | Easy | Easy | Low |
| Gain | Moderate | Moderate | Low |
| Input Resistance | Guaranteed by Bias Current Measurement | Guaranteed by Bias Current Measurement | Not Tested |
| Slew Rate | Moderate | Moderate | Relatively Low |
| Band Width/Response Time | Difficult | Difficult | Moderate |
| Offset Voltage Drift | Very Difficult | Very Difficult | High |
| Offset Current Drift | Very Difficult | Very Difficult | High |

and dividing by the temperature change to obtain the drift—a long and tedious measurement.

In some cases tightened offset voltage specifications over the operating temperature range offer the same performance as a drift tested device, but are less expensive. This is because offset voltage measurement can be a go/no-go measurement. For example, 15$\mu$V/°C can be guaranteed over a 100°C range by limiting the maximum offset voltage to ±0.75 mV or a 1.5 mV band. If the application has an error budget of ± "X" volts, it may be better to tighten the offset voltage rather than have the manufacturer to drift test. Drift testing a comparator is virtually impossible since they are not designed to operate closed loop.

Other parameters dependent upon matching are: offset current, common mode rejection, and supply rejections. These can be greatly tightened at the expense of yield.

Bias current, supply current, gain, slew rate, and response time are dependent upon both device design and processing. The limits for tighter parameters on these specifications are more restrictive. Table II gives reasonable special selection limits. This is only a guideline and, of course, depends on the device.

Noise testing is in a class by itself. Op amp noise will vary between manufacturers of the same device. Further, noise will vary between different types of devices from the same manufacturer. Since noise on a particular device is mostly process dependent, it will be relatively consistant from a single IC producer.

Noise can be broken into two categories: white noise, and popcorn noise. Both of these noise sources can be either voltage or current noise. It is possible with advanced processing to make IC transistors as good as the best discrete low noise transistors. With good processing only a very small percentage of op amps will have any popcorn noise.

Noise measurements are time consuming and costly. Popcorn noise testing may take as much as 30 seconds per unit which limits production to about 100 devices per hour. This low production rate will increase costs. If not absolutely necessary—do not specify noise.

As a final note, some mention should be made of other special testing. Anything reasonable can be done; however, it should be kept in mind that accurate specification in terms of the IC parameters is necessary. It is unlikely a positive result will come from a specification showing a system schematic, system output, and stating "select devices to produce desired outputs." Although this is an exaggeration, it points out the type of specification to be avoided. Performance specification should apply to the IC not to a circuit using the IC. Many manufacturers have circuits available showing the various electrical tests and the way they are done.

**TABLE II. Guideline to Tightened Specifications**

| PARAMETERS | LIMIT | COMMENTS |
|---|---|---|
| Offset Voltage | 0.1 mV | Matching |
| Offset Current | −50% of Nominal | Matching |
| Bias Current | −50% of Nominal | Depends on $H_{fe}$ |
| Supply Current | −25% of Nominal | Depends on Various Process Parameters |
| Gain | +100% of Nominal | Set by Design |
| Common Mode/Supply Rejection | +200% of Nominal | Matching |
| Slew Rate | +30% of Nominal | Set by Design |
| Bandwidth | +30% of Nominal | Set by Design |
| Response Time | −30% of Nominal | Set by Design and Processing |
| Offset Voltage Drift | 0.2$\mu$V/°C − 5$\mu$V/°C | Lower Limit May Not Apply to Many Op Amps |
| Offset Current Drift | Guarantee by Offset Current Limit | |

Robert C. Dobkin
JANUARY 1974

LINEAR BRIEF-27

# MICROPOWER THERMOMETER

## INTRODUCTION

The introduction of a monolithic temperature transducer for the −55°C to +125°C temperature range can considerably simplify the problems encountered in temperature measurement. The three most common sensors—thermistors, resistance sensors, and thermocouples—require a reasonable amount of circuitry for use. Thermistors are highly nonlinear, resistance sensors and thermistors require a stable excitation voltage, and thermocouples have low output. Further, none of these sensors provide an output directly calibrated in a known temperature scale.

The new monolithic temperature transducer provides an output directly proportional to absolute temperature at 10 mV/°K. The chip includes a temperature stable voltage reference and op amp. These allow the output to be offset and scaled to provide any desired temperature scale factor and zero output temperature.

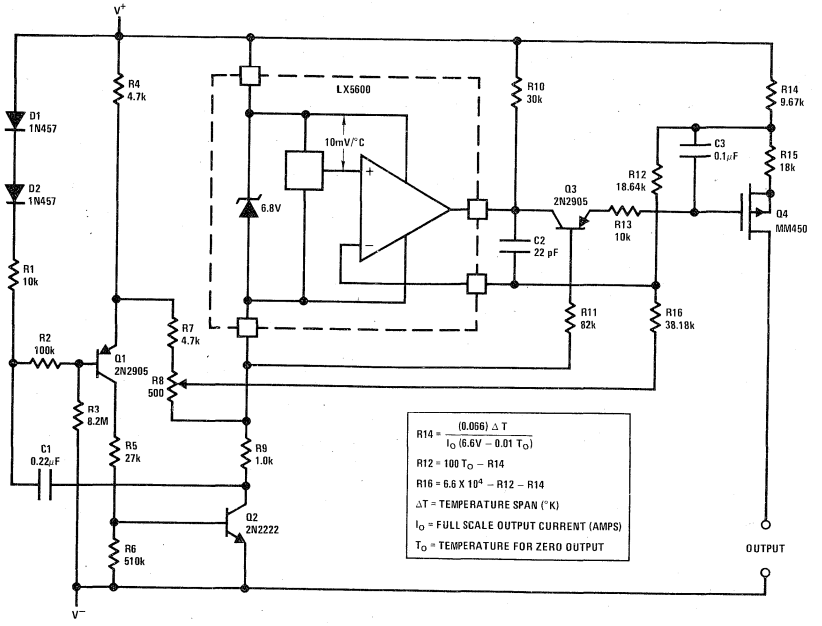
## THERMOMETER DESIGN

The circuit shown will provide a temperature sensitive output with both zero and scale factor independently selectable. Since the temperature transducer requires about 1.0 mA for normal operation, the thermometer is pulsed at a low duty cycle to reduce power consumption. A continuous output is obtained between pulses by a sample and hold. Since temperature does not usually change rapidly, the pulsed operation of the thermometer does not detract from its usefulness.

With the components shown, duty cycle is about 0.2% with a one second sample rate. This gives an average current drain of about 25μA plus the output current. It is designed to operate over a supply voltage of 8.0V to 12V with good results. A small 8.4V mercury battery can give an operational life in excess of one year.

The output of the thermometer is a current proportional to temperature which can be used to drive a meter for a direct readout. Alternatively, a resistor or op amp can be used to obtain a voltage output.

A complementary astable multivibrator, made of Q1 and Q2, drives the LX5600 through R9. The timing is set by several components. C1 and R3




**Micropower Thermometer Circuit Diagram**

control the off-time and C1, R1, R4 and R7 control the on-time. R9 sets the operating current of the transducer to 1.0 mA at the lowest supply voltage.

When the transducer is "on," sample transistor Q3 is also on. The output of the op amp drives the sample capacitor, C3, and MOSFET, Q4. Feedback is obtained from R12, R14 and R16 which set both the zero and scale factor of the thermometer. When the transducer is turned off, a continuous output is provided by C3 and Q4. Resistor R15 decreases the circuit's sensitivity to MOSFET gm, allowing almost any MOSFET to be used. About 2.0V should be dropped across R15 at full scale output. R8 is used to trim the thermometer, correcting for zener tolerance, temperature error in the sensor and resistor tolerance. With the values shown, a 0 to 50μA output is obtained for a +50°F to +100°F temperature change. Other ranges can be selected by using the formulas shown in the box on the circuit diagram.

The low power consumption makes this thermometer especially attractive for battery operated equipment. Further, the current source output allows long lines to be driven with no loss of accuracy. Finally, the circuit is easy to set up for almost any desired temperature range.

Robert C. Dobkin
JUNE 1974

LINEAR BRIEF-28

# GENERAL PURPOSE POWER SUPPLY

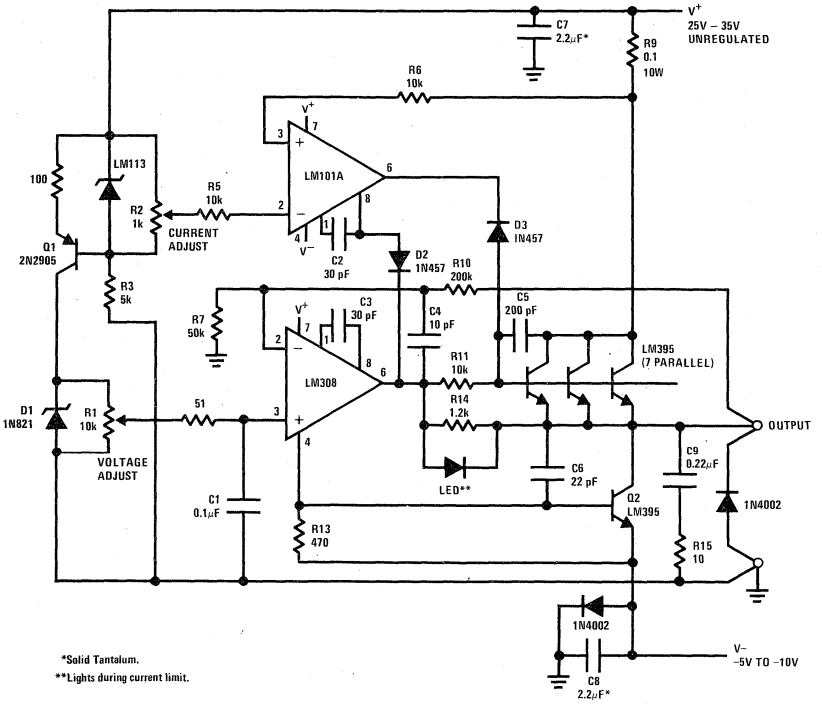
## INTRODUCTION

A general purpose lab type constant voltage/constant current power supply is easily made using standard integrated circuits. The circuit shown will provide up to 25V at up to 10A output with both the output voltage and current adjustable down to zero. Although relatively simple, very high performance is obtained.

Lab supplies must withstand considerable abuse. Good control of maximum output current is mandatory both to protect the supply and the powered circuitry. One of the short comings of many commercial supplies is the use of a large output capacitor to help frequency compensate the regulator loop. This output capacitor can discharge many times the peak output current of the supply into the load as well as degrade the ac output impedance when the supply is used as a constant current source. (Of course, the output capacitor helps keep the ac output impedance low when the supply is used as a constant voltage source.) The circuit shown has good response both as a constant voltage or constant current source.

The use of the LM395 monolithic power transistor as the pass element considerably simplifies the design power. The LM395 acts as a 2A current limited, thermally limited, high gain power transistor. Since only a maximum of 10μA is needed to drive the pass elements and complete overload protection is included on the chip, external biasing and protection circuitry is minimized. Only two control op amps are needed—one for voltage control and one for current control.

In constant voltage operation, a reference voltage is fed from voltage control pot, R1, through a high frequency filter into the non-inverting input of an LM308 op amp. The output of the LM308 drives seven paralleled LM395's as emitter followers to obtain a 10A capability.



Feedback is taken through R10 directly from the output with the overall gain set at 5 by the ratio of R10 to R7. An additional LM395 is driven from the negative power supply lead of the LM308 to provide some output current sink capability (2A) so the supply can be quickly programmed even with large capacitive loads. Frequency compensation is achieved with C3 for the LM308 and C4 for the overall loop. Resistor R11, capacitors C5 and C6 and network R15 — C9 suppress parasitic high frequency oscillations.

When the circuit is used in the constant current mode, the LM101A overcomes the constant voltage loop to control the output. Output current is sensed in R9 and compared with the voltage between $V^+$ and the arm of R2. R2 is connected across an LM113 low voltage reference diode to provide a 0V to 1.2V reference for 0A to 12A output. When the output current is below the set level, the LM101A output is positive, reverse biasing D3 and the LM308 control the output. When the current increases to the control point the output of the LM101A swings negative and decreases the drive to the output pass devices through D3, limiting the current. (Note that no separate positive supply is needed since the common mode operative range of the LM101A is equal to the positive supply.) Diode, D2, clamps the output of the LM101A when it is not regulating, decreasing the switchover time from voltage to current mode operation.

A few special precautions are needed in construction for proper operation. All LM395's should be mounted on the same heat sink to insure good current sharing. Also, a large heat sink is necessary since 300W will be dissipated under worst case conditions. Since the LM395's are high devices, the supply bypasses should be near the power transistors.

Elias S. Papanicolaou
Helge H. Mortensen
FEBRUARY 1975

LINEAR BRIEF-29

# LOW-COST AM RADIO SYSTEM USING LM1820 AND LM386

## INTRODUCTION

The majority of linear integrated circuits being produced today is in the field of op amps, comparators and regulators. This has come about for the reason that these types of devices can take advantage of the well matched characteristics of monolithic components. However, in recent years the monolithic integrated circuit has found its place in communication systems such as radios and televisions. The basic philosophy in this area, and the consumer industry as a whole, has mainly been cost reduction over discrete counterparts, improved performance and higher reliability.

An integrated circuit which meets the above criteria is the LM1820 AM-RADIO SYSTEM, designed primarily for superheterodyne AM receiver applications utilizing an RF-amplifier stage ahead of the mixer-oscillator. However, this linear brief describes how the LM1820 and LM386 can be incorporated in the design of a conventional low cost AM-radio without an RF-amplifier stage.

## RADIO DESCRIPTION

The block diagram of the radio is depicted in *Figure 1*. A complete schematic is shown in *Figure 2*. The building blocks for the Mixer-Oscillator, the two IF stages, and the AGC section, are contributed by the LM1820. Power output of 1/4W into an 8Ω speaker is obtained by the LM386, the gain of which is externally set to 200. The LM1820 is operated from a 6V supply, that is, below the voltage of zener diode D6, see *Figure 3*.

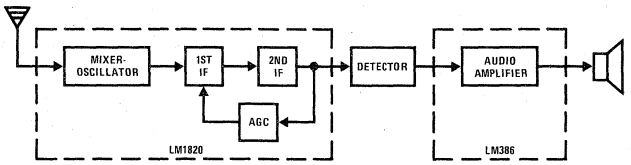



FIGURE 1. Radio Block Diagram

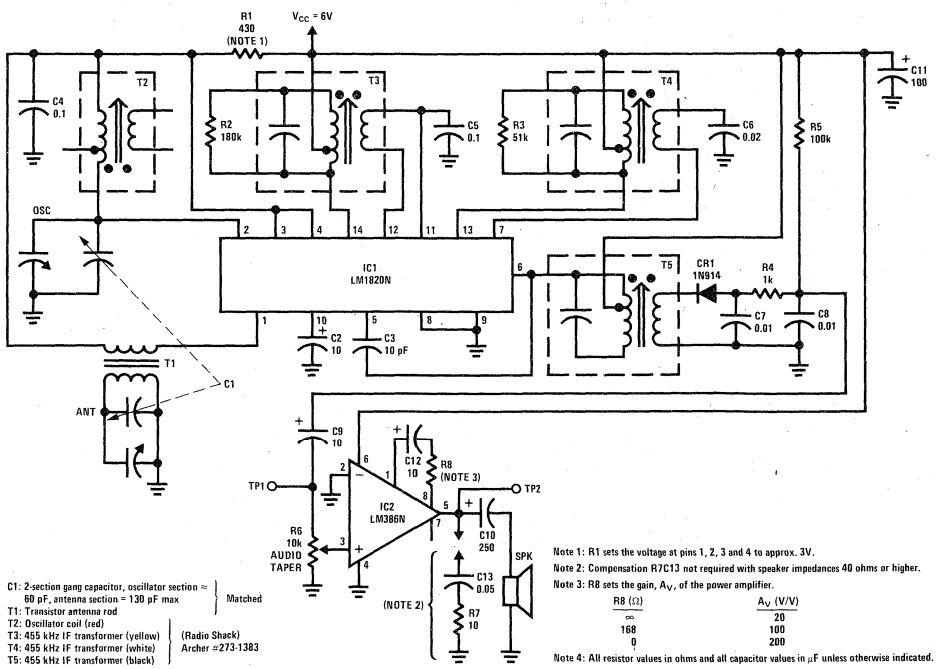



FIGURE 2. Radio Schematic

Pins 1, 2, 3 and 4 are biased from the same supply through a 430Ω dropping resistor. This reduces the total current consumption to approximately 10 mA making the operation from a 6V battery feasible. The dc return of pin 1 and 4 to pin 3 improves component count and prevents transistor Q4 in the oscillator section from saturating. Large swings are preserved by returning the collectors at pins 14, 13 and 6 to $V_{CC}$ via the primary windings of transformers T3, T4 and T5 respectively. For better linearity, detector diode 1N914 is biased slightly in the forward direction. Radio performance concerning distortion, AGC, sensitivity and signal-to-noise is shown in *Figure 4*. These data are taken with the radio laid out as shown in *Figure 5*.

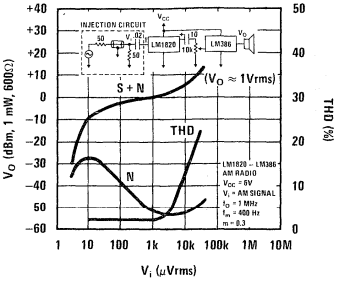



**FIGURE 4. Radio Performance Plots**

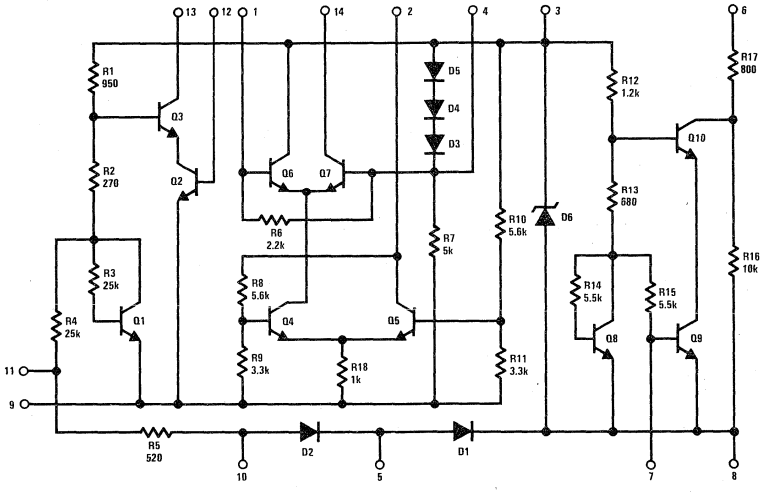



**FIGURE 3. LM1820 Schematic**

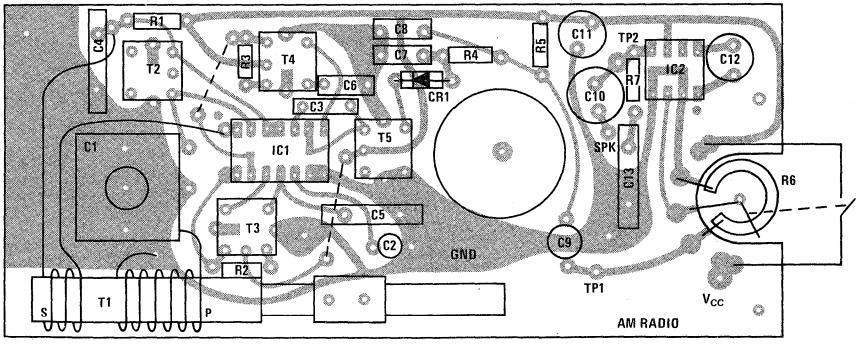



**FIGURE 5. Typical Printed Circuit Board Radio Layout (Bottom View)**
**(Not Shown Full Size)**

Wade Tuma
JULY 1975

LINEAR BRIEF-30

# LOW COST LED THERMOMETER

The circuit shown in Figure 1 is a Fahrenheit and centigrade digital thermometer using LED display. The use of a ±1 digit along with an unusual code conversion technique allows a display of -40 to +100 in the centigrade mode, and -40 to +199 in the Fahrenheit mode. Only one supply is required and critical voltages in the analog subsection are referenced to the zener contained in the LM5700 sensor making additional regulation unnecessary.

## CIRCUIT OPERATION

The LM5700, LM555 and MM74C04 integrated circuits are the basic components of a linear voltage to frequency converter which uses the 10 mV/°Kelvin sensor voltage as its input. Linearity is achieved through the use of an MM74C04 operating with the reference voltage in the LM5700 as its supply potential. The pulse width at the input to the MM74C04 is held constant by the Rand C used with the LM555. The repetition rate of these pulses, however, is determined by the current in the 2N4403 which is controlled by the LM5700. The voltage amplitude of these constant width pulses at the output of the CMOS inverters is equal to the zener voltage of the LM5700. The filtered voltage returned to the summing junction of the LM5700 is

$$\text{frequency} \times V_{REF} \times T$$

where T is the pulse width. As the constraints of the feedback loop force this voltage to equal the sensor voltage, any frequency rate may be obtained by choosing the LM555 pulse width, where

$$\frac{\text{temperature in } ^\circ K \times .01}{V_{REF} \times T} = \text{frequency.}$$

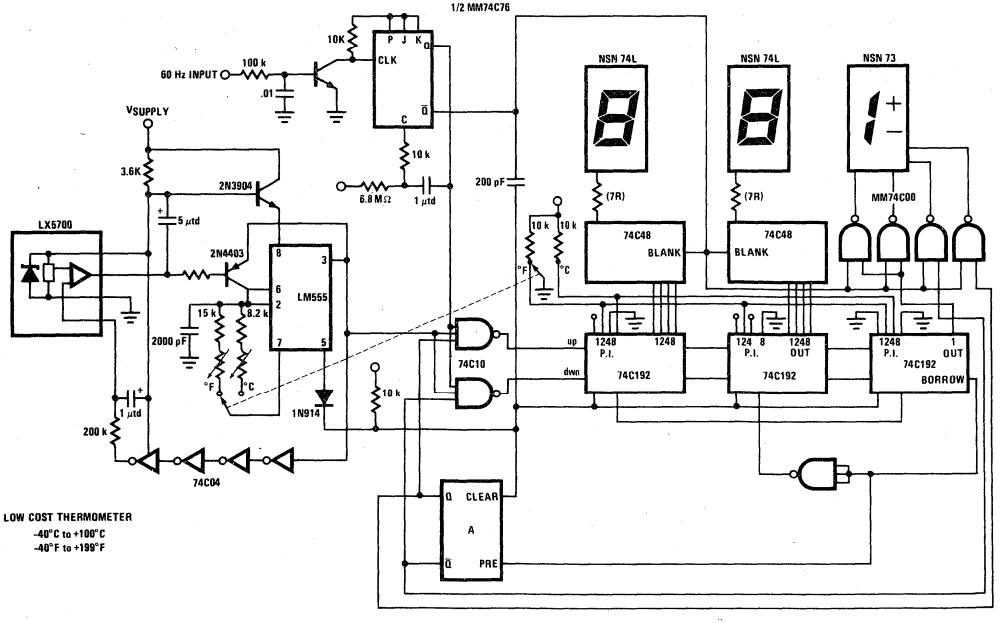



FIGURE 1

Thus the frequency output of the LM555 is proportional to the temperature in degrees Kelvin. In order to convert this to display in degrees centigrade or Fahrenheit, a digital code converter is used. The operation of this converter is represented by the bar graphs in Figure 2. The first three bars show the conversion between degrees Kelvin, centigrade, and Fahrenheit. Graphs 4 and 5 show the actual frequencies the LM555 is calibrated to produce at various temperatures. By gating these frequencies with a 16.66 ms pulse developed from the 60 Hz line, the counts which are fed to the counters are developed. These counts are depicted in Graphs 6 and 7.

Note that these counts are equal to temperature in degrees Kelvin and Rankin. By presetting the three decade counters to 273 in the centigrade mode and 459 in the Fahrenheit mode these counts are converted from Kelvin to centigrade and Rankin to Fahrenheit. The counters count down during each gate time. If the temperature and therefore the frequency is low and the gate closes before zero is detected a minus temperature is displayed. For higher temperatures, a borrow will be detected at zero degrees before gate closure and the counters will begin to count up. Thus the flip flop which controls the down or up state of the counters also controls the plus or minus sign. This final display is shown in Graphs 8 and 9.

The number of updates/second is controlled by the 6.8 MΩ resistor and 1 μF capacitor in the gate generating flip flop and may be adjusted for various applications.

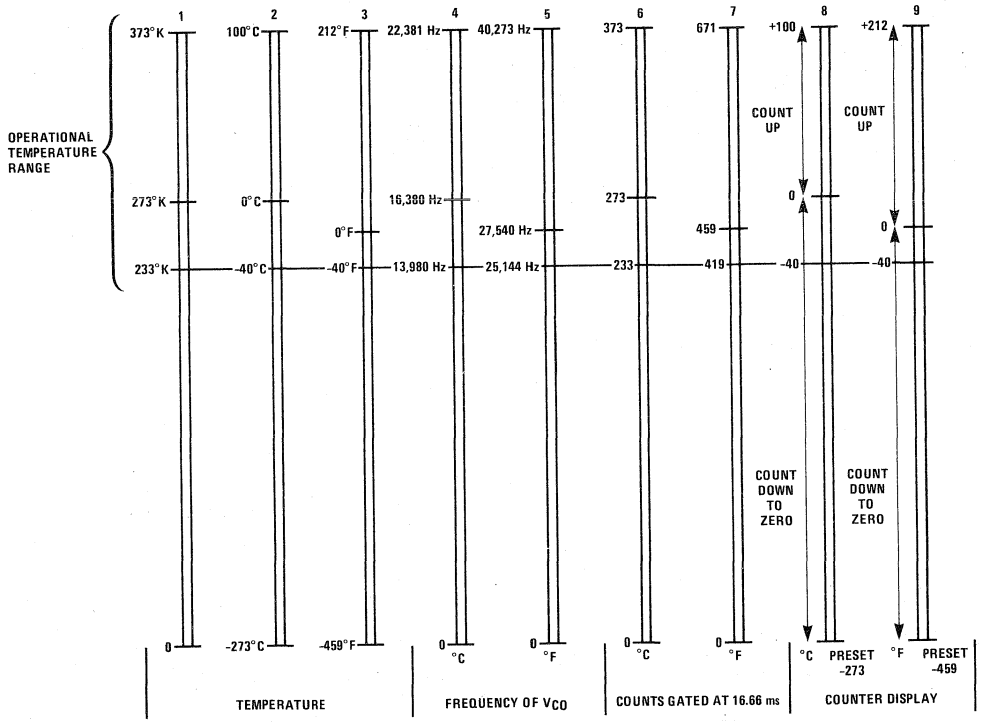



FIGURE 2

Forrest Sass
Brent Welling
JUNE 1976

LINEAR BRIEF-31

# CRYSTAL OVEN CONTROLLER AND PRECISION VOLTAGE REFERENCE

## INTRODUCTION

Small ovens have long been used to temperature stabilize critical circuits or components such as oscillators or VCO's. Usually, the circuitry requiring a crystal oven will also require a very stable voltage reference or power supply for the circuitry. This brief describes the use of an LM199 temperature stabilized reference zener both as a low cost, accurate oven temperature controller and as a voltage reference. The temperature controller will regulate oven temperature at 82°C to 84°C depending on oven configuration and thermal resistance, with long term stability accurate to ±0.1°C. The voltage reference portion is a 6.95V active zener capable of supplying up to 10 mA of current, a reverse dynamic impedance better than 1.0Ω, long term stability better than 20 ppm/1000 hr. and a temperature coefficient of 1 ppm/°C max*. The circuit can be designed for use over a wide range of supply voltages, from 9V to 40V.

## CIRCUIT DESCRIPTION

The oven controller consists of R1, Q1 and the temperature stabilizer portion of the LM199 integrated circuit *(Figure 1)*. Control of oven temperature is achieved using the stabilizers' ability to sense die temperature.

The stabilizer of the LM199 is a temperature-dependent current source which ordinarily has the sole function of maintaining a constant 85°C die temperature by dissipating power. Heater current vs die temperature for various supply voltages are shown in *Figure 2*. The LM199 comes packaged in a plastic thermal shield which is removed for this application. The TO-46 can inside is coupled to the oven ambient via a heat sink attached to the copper-clad surface of a P.C. board within the oven. The LM199 die, including the stabilizer, will now closely track ambient oven temperature in spite of the stabilizer's power dissipation.

The oven heater, R1, is a length of nichrome wire wrapped around the oven core. The value of R1 depends on the supply voltage and the amount of power to be dissipated. For an oven with a core mass (including circuitry) of 12 oz., an uninsulated surface area of 10 $in^2$ and 3/4 inch of insulation, a 10 watt (at full power) heater is adequate.

The heater is controlled by Q1, a PNP power transistor such as an NSP4919.

Initially the oven and circuitry are at ambient (room) temperature. When power is applied, the stabilizer turns on attempting to heat the die. This initial stabilizer current is enough to saturate Q1 and run the oven heater R1 at full power. As the temperature approaches 85°C, the stabilizer draws less and less current, which in turn reduces current delivered to R1 via Q1.

The oven reaches equilibrium when the LM199 die temperature is very close to 85°C, the oven temperature is 82°C to 84°C, and the heat generated by the stabilizer, R1, and Q1 equals the heat lost through the walls of the oven. These temperatures will now remain constant to within ±0.1°C. The time taken to reach 1% of final temperature is about 12 to 15 minutes, as shown in *Figure 3*.

Resistor R2 is used to set the zener current and the load current of the voltage reference. The zener current

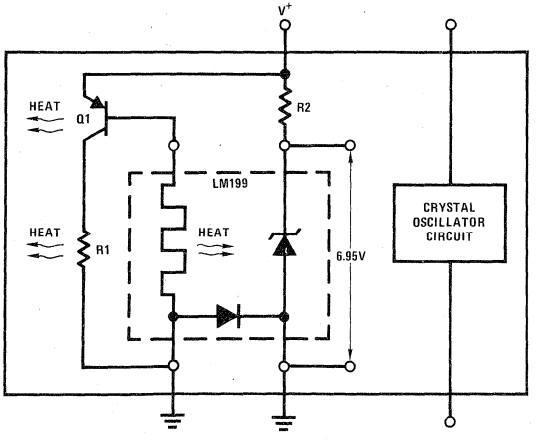



FIGURE 1. Schematic of Oven Temperature Controller

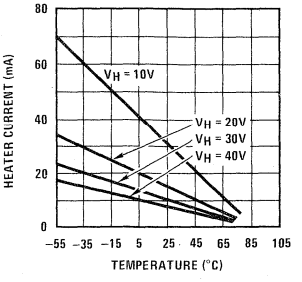



FIGURE 2. Heater Current vs Die Temperature

*See LM199/LM299/LM399 Precision Reference Data Sheet.

should be set at about 1 mA. Care should be taken to keep the zener and stabilizer ground leads separate. IR drops in a common ground lead can cause apparent variation in reference voltage. Also, care must be taken not to forward bias the LM199 substrate diode if the "negative" leads are not used as grounds.

## CONSTRUCTION HINTS

Practically any type of commercially available crystal oven enclosure may be used, or an oven may be constructed. A few points are worth mentioning. First, all components including Q1 may be mounted on a P.C. board (*Figure 4*). At equilibrium, however, Q1 will dissipate one or two watts or power and care must be taken to keep it as far away as possible from the rest of the circuit components to prevent large temperature gradients. If Q1 is mounted on the copper-clad surface of the P.C. board, etch a 1/8" line across the copper to further thermally isolate Q1. (Copper interconnects from Q1 to the rest of the circuit will not significantly increase temperature gradients.)

Second, best results are obtained when the LM199 is firmly attached to the copper-clad surface via a heat sink. Thermal bonding may be further increased by using a good thermal grease. Poor temperature regulation or regulation at a lower-than-normal oven temperature may be due to poor attachment, or operation of the LM199 without a heat sink.

For applications requiring a crystal oven and precision voltage reference, the LM199 is an extremely cost-effective solution for both requirements, with no sacrifice of precision or performance.

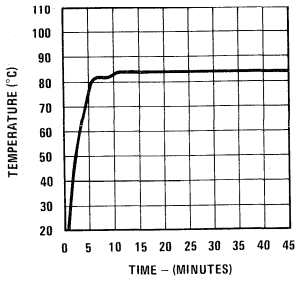



FIGURE 3. Typical Oven Warm-Up Time

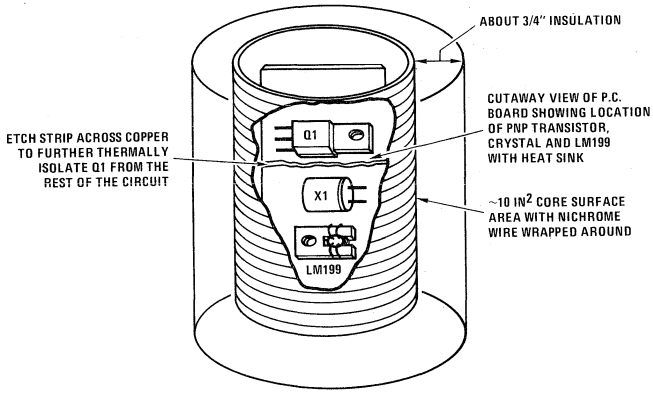



FIGURE 4. Detail of Typical Oven Construction

Peter Lefferts
JUNE 1976

LINEAR BRIEF-32

# MICROVOLT COMPARATOR

## INTRODUCTION

Comparison of dc signal levels within microvolts of each other can be made by using an LM121A pre-amp and an LM111 comparator IC. Implementing this with two separate IC's decreases noise, eliminates troublesome thermal effects, and achieves a maximum offset drift of 0.22$\mu$V/°C *(Figure 1)*.

Designing a practical comparator with a voltage gain of 10 million involves protecting the *input* stage from temperature changes or gradients, and avoiding problems of including the noise filter within the positive feedback loop. The circuit as shown has a 5$\mu$V hysteresis which can be trimmed to 1$\mu$V under certain conditions. Further, delays *decrease* with increasing overdrive (see chart) due to elimination of input stage thermal effects, saturating stages, and dielectric soak or polarization effects on signal filter capacitors (Table I).

## DESIGNING WITH A PRE-AMP

With the bias network shown, the LM121A input stage has an open-loop temperature stable voltage gain of close to 100. The 100k output impedance of the LM121A is shunted by $C_S$ to filter out pickup and internally generated noise. No feedback to the inputs of the pre-amp is employed to avoid degrading common-mode rejection of the system.

The separate pre-amp with a gain of 100 provides two major advantages over single comparator designs. First, $V_{OS}$ and other small errors attributed to the LM111 are reduced by the 100 gain factor. More important, temperature gradient changes which occur within the LM111 when switching any output load, are completely isolated by the separate packages and do not affect the pre-amp. If the entire microvolt comparator were on a single silicon chip, a temperature variation of as little

**TABLE 1. Typical Overdrive Delays**

| HYST. SET | $R_H$ | $R_S$ | $C_S$ | DELAYS WITH VARIOUS OVERDRIVES | | | |
|---|---|---|---|---|---|---|---|
| | | | | 25% | 100% | 1000% | 100 mV |
| 5$\mu$V | 75 k$\Omega$ | 10 k$\Omega$ Max. | 6800 pF | 2 ms | 1.8 ms | 600$\mu$s | 560$\mu$s |

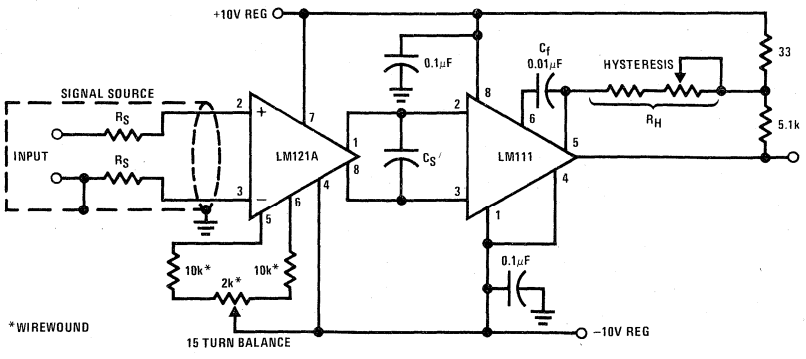



**FIGURE 1. Schematic Diagram**

as 1/1000°C across the input stage could have a significant effect.

This effect is a major reason for designing circuits sensitive and stable to microvolt dc signals with a *separate* pre-amplifier. Further, the special 4-transistor input stage, when adjusted to zero offset with the "balance" control between pins 5 and 6, automatically reduces $V_{OS}$ change with temperature to almost zero.

## FILTERING

The pre-amp/comparator system generates a continuous stream of very fast pulses if assembled without a filter, even with positive feedback for hysteresis. This is caused by both stray output-input feedback, and noise. The noise is both thermal and pickup from the environment, including power switching transients and fluorescent light hash. To cure this, shunt filter capacitor $C_S$ is used.

Placing this capacitor outside the positive feedback loop has two advantages. It eliminates a tendency for the comparator to oscillate during slow transitions. Also, response time to small signals is halved since the positive hysteresis feedback signal is not stored on the filter capacitor.

A higher frequency filter ($C_f$) is needed to provide a low impedance shunt to any high frequency noise and stray feedback that may be picked up between LM111 terminals 5 and 6. These two terminals have almost the same voltage sensitivity as the normal input terminals. The positive feedback to terminal 5, as described below, is only delayed slightly by this filter.

## FEEDBACK

The positive feedback provided by the 5.1k/33Ω voltage divider with $R_H$ is needed to insure clean, rapid changes of state. It is applied to one of the "balance" terminals (pin 5) of the LM111 to simplify the circuit over a balanced feedback network, and to minimize signal stored on $C_S$ as previously described. The current fed back to terminal 5 is single ended with respect to the balance adjust network between these terminals, and hence injects a dc offset of the desired polarity and amplitude for a few microvolts of latching.

## PERFORMANCE

A tabulation is shown for one of the many possible combinations of input circuits, filters, etc. For large amplitude signals, $C_S$ can be decreased and hysteresis increased for greater speed. Conversely, to obtain hysteresis as low as 1μV, trim $R_H$ (to about 300k) use a $C_S$ of 0.01μF to 0.1μF and have a low impedance source of signals.

For reduced ambient range and drift specifications, an LM321 can be paired with the LM311 for a cost saving while maintaining the same comparison sensitivity.

## DESIGN TIPS FOR MICROVOLT SIGNALS

Even with high performance devices such as the LM121, microvolts of error can occur from thermocouple effects, common-mode signals, "microphonics," or unbalances in the input or nulling circuits. As pointed out in application note AN-79, Kovar lead to copper circuit board thermocouple effects can cause a 3.5μV offset voltage for only 0.1°C difference across the input leads. A compact layout of input connections and shielding from air currents will minimize this problem.

Although the LM121A has excellent common-mode rejection (> 120 dB), a 1V change in common-mode voltage can induce up to 1μV of error voltage. For this reason common-mode voltage changes should be kept to a minimum. Also, common-mode voltages allow mechanical vibrations in the probe cable to induce "microphonic" noise signals. Short, stiff, low capacitance and symmetrical input shielded wires are recommended.

If it is possible to have a signal source balanced with regard to ground, it will help decrease errors due to bias currents, and noise due to common-mode and microphonic effects. Matched, low temperature coefficient parts should be used in the balance network, and care should be exercised in shielding input circuits and eliminating ground-loops.

## APPLICATIONS

The microvolt comparator is particularly well suited to controllers or test equipment having thermocouples or strain gauges as inputs. This includes wind speed indicators, RMS to dc converters, vacuum gauges, gas analysis equipment, conductivity gauges, and hot wire controls. The strain gauges can be used in materials testing, electronic weighing, pressure transducers, and load limiting sensors for cranes, hoists, and rolling mills.

As a temperature controller, 1/8 degree or less on-off differential can be obtained using thermocouple types E, J, T or K. Other microvolt signals used for control may come from Hall effect sensors, Bolometers, slidewires, and heat-flow thermopiles. A microvolt comparator will be useful in "Go/No-Go" testing of low resistances such as switch and relay contacts, RTDs, coil and fuse resistances, and pressure-sensitive-plastic conductors.

Dave Long
JUNE 1976

LINEAR BRIEF-33

# HIGH SPEED WARNING DEVICE FOR AUTOMOBILES

Conventional speed warning devices require the addition of a multipole electromagnetic transducer in the transmission or the speedometer cable as a source for the speed signal. The proposed circuit uses the engine speed signal available at the primary of the spark coil and a switch in the transmission which is closed only in high gear. Lowest cost display would be a light emitting diode driven directly from the integrated circuit. Add a durawatt transistor, and an incandescent lamp can be driven. Two NSN71 1/3 inch high 7-segment numeric displays can be hard wired to display the speed at which the limit is set. For best effect, the visual warning should be accompanied by an audible alarm such as a buzzer. A more elegant solution which sounds better and costs little more uses a tone generator to drive a miniature moving coil loudspeaker.

The circuit shown in *Figure 1* employs an LM2900 quad Norton op amp to perform all the above functions. Specifically, A1 amplifies and regulates the signal from the spark coil. A2 converts frequency to voltage so that its output is a voltage proportional to engine RPM. This signal could be used to directly drive a tachometer if desired. A3 compares the tachometer voltage with the reference voltage and turns on the output transistor at the set speed. A small amount (2%) of positive feedback is provided to prevent annoying intermittent operation. Amplifier A4 is used to generate an audible tone whenever the set speed is exceeded. R1 is adjusted in the factory according to the gear and axle ratios, number of cylinders, wheel and tire size, etc. Note that the 2900 is capable of directly driving the loudspeaker.

In operation, the circuit is powered up so that the tachometer drive is always available. When the transmission moves to top gear, switch S1 closes and connects the output light and speaker displays to the power source. When the vehicle speed exceeds the set value (56 mph U.S. or 82 km/hr South American) the light and tone will be energized. To extinguish these warnings, the driver will have to slow the vehicle to below the value set by the hysteresis (say 55 mph or 80 km/hr). The integrating 10$\mu$F capacitor on the frequency to voltage converter, A2, could be increased so that the alarm is not sounded during momentary excursions above the set speed.

**TABLE I. Component Distribution**

| | PRE-AMP & FILTER | FREQ TO VOLTAGE (TACH) | COMP & OUTPUT | TONE GEN | PROT & REG | TOTAL |
|---|---|---|---|---|---|---|
| Resistors | 4 | 2 | 5 | 4 | 1 | 16 |
| Capacitors | 1 | 2 | | 1 | 1 | 5 |
| Diodes | 1 | 1 | | 1 | | 3 |
| Transistors | | | 1* | | 1 | 2 |
| IC's | 1/4 | 1/4 | 1/4 | 1/4 | | 1 |
| Other | | | LED | Speaker | | 2 |
| | | | | | | 29 |

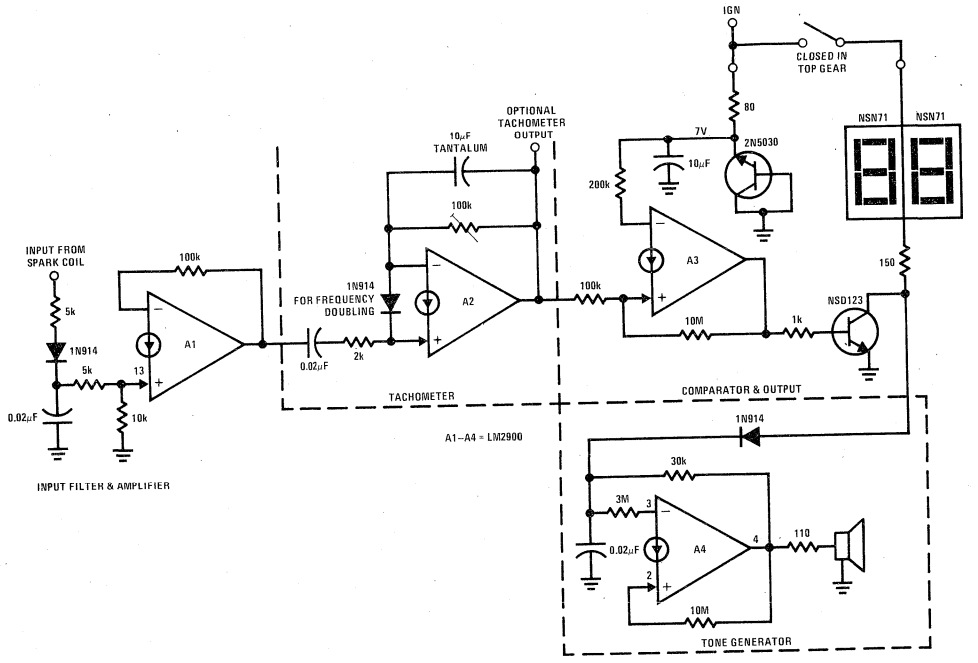



**FIGURE 1. High Speed Warning Device**

Note: Since this linear brief was written, the LM2907, LM2917 Frequency to Voltage Converter was developed which performs the same function as described here. See Application Note AN-162.

Nello Sevastopoulos
JUNE 1976

LINEAR BRIEF-34

# A MICROPOWER VOLTAGE REFERENCE

A low-drift voltage reference can be easily made by converting a zero temperature coefficient current to a voltage. JFETs biased slightly below pinch-off exhibit a zero temperature coefficient drain current ($I_D$) as shown in *Figure 1*. With the above property and a micropower operational amplifier, used to convert the drain current to a voltage, a low power consumption voltage reference can be built as shown in *Figure 2*. The consumption of LM4250 op amp is programmed through resistor $R_{SET}$. Potentiometer P1 should be adjusted for low output ($V_{REF}$) temperature coefficient. Actually, it can be trimmed for positive, negative or zero temperature coefficient. The output voltage is trimmed through P2 and it is expressed by:

$$V_{REF} = I_{D1}(P_2' + R1 + R2),$$

$$R2 = R3,\ I_{D1} \simeq I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]2$$

With the values shown in *Figure 2*, the temperature coefficient of the output is 0.002%/°C and the overall standby current less than 100μA. The characteristics of the LM4250 are a function of its supply current, which depends on $R_{SET}$, and $V^+$. $V^+$ can be provided by $V_{REF}$ through the addition of a second FET, J2, shown in *Figure 3*. This way the parameters of the op amp will be independent of the unregulated input. The reference voltage output can be taken from the wiper of the potentiometer P2 ($V_{REF} = V^+$) or from the source of J2 ($V_{REF} > V^+$). In the first case, the output impedance of the circuit is quite high and buffering may be required according to the application. The output impedance in the second case is low, essentially the 1/gm of (J2) divided by the loop gain of the circuit. In this case, a small temperature coefficient due to the supply current of the LM4250 is going to be added and be compensated for by an additional trimming of P1. $V_{REF}$ is computed by:

$$V_{REF} \simeq I_{D1}\,[P2 + R1 + R2] + P_2''\,[I_S + I_{D1}],$$

$$R2 = R3,\ I_S \simeq \frac{6(V^+ - V_{BE})}{R_{SET}}$$

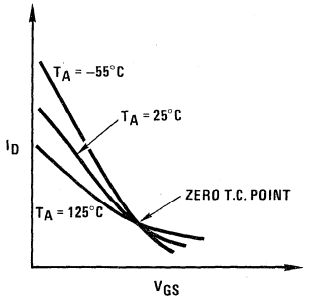



**FIGURE 1. FET Transfer Characteristics**

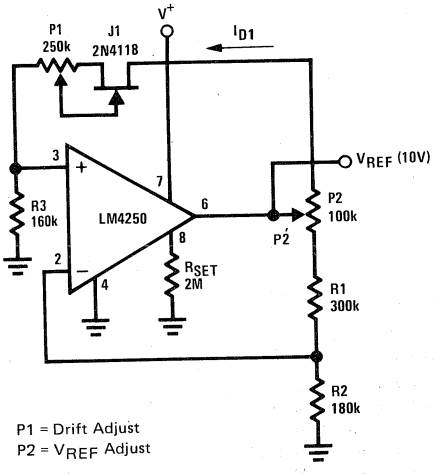



FIGURE 2. Basic Voltage Reference

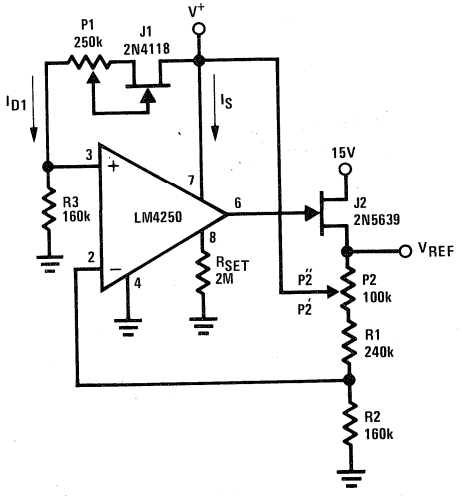
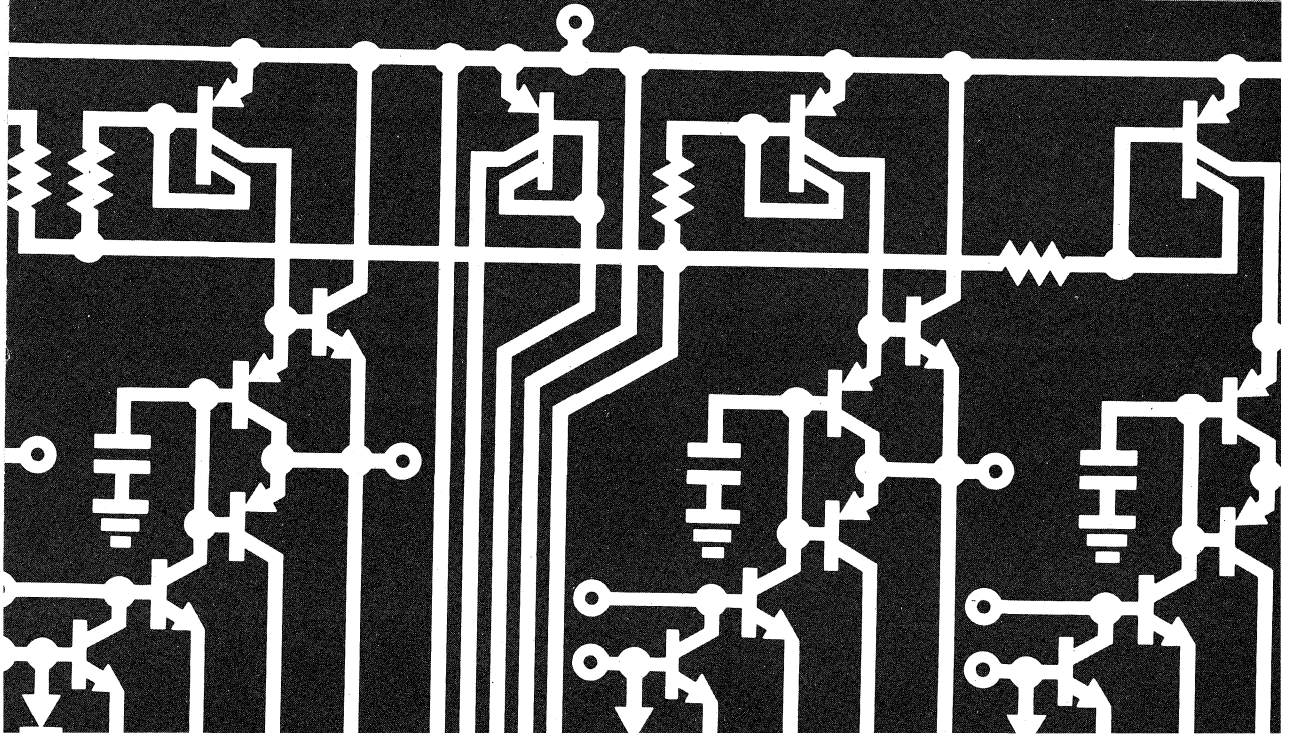



FIGURE 3. Improved Voltage Reference

# National Semiconductor
# APPENDICES



James E. Solomon
DECEMBER 1974

# THE MONOLITHIC OP AMP: A TUTORIAL STUDY

*Invited Paper—*
*IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6*

***Abstract*—A study is made of the integrated circuit operational amplifier (IC op amp) to explain details of its behavior in a simplified and understandable manner. Included are analyses of thermal feedback effects on gain, basic relationships for bandwidth and slew rate, and a discussion of pole-splitting frequency compensation. Sources of second-order bandlimiting in the amplifier are also identified and some approaches to speed and bandwidth improvement are developed. Brief sections are included on new JFET-bipolar circuitry and die area reduction techniques using transconductance reduction.**

## I. Introduction

THE integrated circuit operational amplifier (IC op amp) is the most widely used of all linear circuits in production today. Over one hundred million of the devices will be sold in 1974 alone, and production costs are falling low enough so that op amps find applications in virtually every analog area. Despite this wide usage, however, many of the basic performance characteristics of the op amp are poorly understood.

It is the intent of this study to develop an understanding for op amp behavior in as direct and intuitive a manner as possible. This is done by using a variety of simplified circuit models which can be analyzed in some cases by inspection, or in others by writing just a few equations. These simplified models are generally developed from the single representative op amp configuration shown in Figs. 1 and 2.

The rationale for starting with the particular circuit of Fig. 1 is based on the following: this circuit contains, in simplified form, all of the important elements of the most commonly used integrated op amps. It consists essentially of two voltage gain stages, an input differential amp and a common emitter second stage, followed by a class-AB output emitter follower which provides low impedance drive to the load. The two interstages are frequency compensated by a single small "pole-splitting" capacitor (see below) which is usually included on the op amp chip. In most respects this circuit is directly equivalent to the general purpose LM101 [1], $\mu$A 741 [2], and the newer dual and quad op amps [3], so the results of our study relate directly to these devices. Even for more exotic designs, such as wide-band amps using feedforward [4], [5], or the new FET input circuits [6], the basic analysis approaches still apply, and performance details can be accurately predicted. It has also been found that a good understanding of the limitations of the circuit in Fig. 1 provides a reasonable starting point from which higher performance amplifiers can be developed.

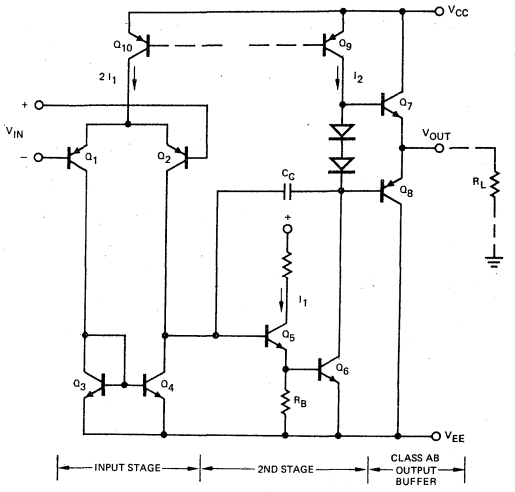



Fig. 1. Basic two-stage IC op amp used for study. Minimal modifications used in actual IC are shown in Fig. 2.

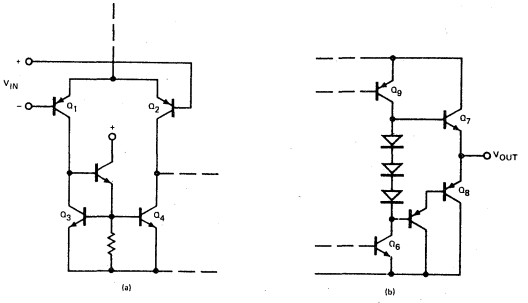



Fig. 2. (a) Modified current mirror used to reduce dc offset caused by base currents in $Q3$ and $Q4$ in Fig. 1. (b) Darlington p-n-p output stage needed to minimize gain fall-off when sinking large output currents. This is needed to offset the rapid $\beta$ drop which occurs in IC p-n-p's.

The study begins in Section II, with an analysis of dc and low frequency gain. It is shown that the gain is typically limited by thermal feedback rather than elec-

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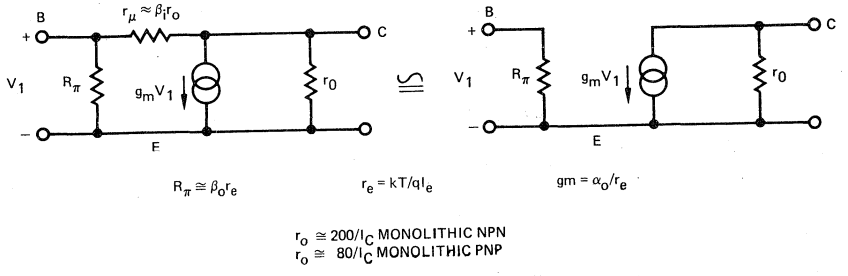
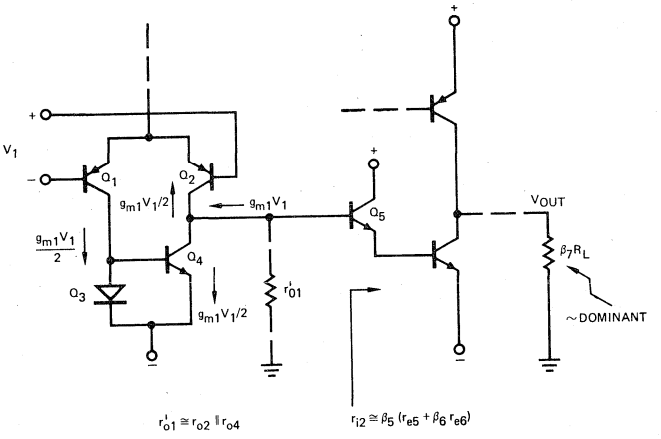



(a)




(b)

Fig. 3. (a) Approximate $\pi$ model for CE transistor at dc. Feedback element $r_\mu \cong \beta_i r_o$ is ignored since this greatly simplifies hand calculations. The error caused is usually less than 10 percent because $\beta_i$, the intrinsic $\beta$ under the emitter, is quite large. Base resistance $r_x$ is also ignored for simplicity. (b) Circuit illustrating calculation of electronic gain for op amp of Fig. 1. Consideration is given only to the fully loaded condition ($R_L \cong 2$ kΩ) where $\beta_7$ is falling (to about 50) due to high current density. Under this condition, the output resistance of $Q6$ and $Q9$ are nondominant.

trical characteristics. A highly simplified thermal analysis is made, resulting in a gain equation containing only the maximum output current of the op amp and a thermal feedback constant.

The next three sections apply first-order models to the calculation of small-signal high frequency and large-signal slewing characteristics. Results obtained include an accurate equation for gain-bandwidth product, a general expression for slew rate, some important relationships between slew rate and bandwidth, and a solution for voltage follower behavior in a slewing mode. Due to the simplicity of the results in these sections, they are very useful to designers in the development of new amplifier circuits.

Section VI applies more accurate models to the calculation of important second-order effects. An effort is made in this section to isolate all of the major contributors to bandlimiting in the modern amp.

In the final section, some techniques for reduction of op amp die size are considered. Transconductance reduction and layout techniques are discussed which lead to fabrication of an extremely compact op amp cell. An example yielding 8000 possible op amps per 3-in wafer is given.

## II. Gain at DC and Low Frequencies

### A. The Electronic Gain

The electronic voltage gain will first be calculated at dc using the circuit of Fig. 1. This calculation becomes straightforward if we employ the simplified transistor model shown in Fig. 3(a). The resulting gain from Fig. 3(b) is

$$A_V(0) = \frac{v_{out}}{v_{in}} \cong \frac{g_{m1}\beta_5\beta_6\beta_7 R_L}{1 + r_{i2}/r_{01}'} \qquad (1)$$

where

$$r_{i2} \cong \beta_5(r_{e5} + \beta_6 r_{e6})$$

$$r_{01}' \cong r_{04}//r_{02}.$$

It has been assumed that

$$\beta_7 R_L < r_{06}//r_{09},\ g_{m1} = g_{m2},\ \beta_7 = \beta_8.$$

The numerical subscripts relate parameters to transistor $Q$ numbers (i.e., $r_{e5}$ is $r_e$ of $Q_5$, $\beta_6$ is $\beta_0$ of $Q_6$, etc.). It has also been assumed that the current mirror transistors $Q_3$ and $Q_4$ have $\alpha$'s of unity, and the usually small loading of $R_B$ has been ignored. Despite the several assumptions made in obtaining this simple form for (1), its accuracy is quite adequate for our needs.

An examination of (1) confirms the way in which the amplifier operates: the input pair and current mirror convert the input voltage to a current $g_{m1}v_{in}$ which drives the base of the second stage. Transistors $Q_5$, $Q_6$, and $Q_7$ simply multiply this current by $\beta^3$ and supply it to the load $R_L$. The finite output resistance of the first stage causes some loss when compared with second stage input resistance, as indicated by the term $1/(1 + r_{i2}/r_{01}')$. A numerical example will help our perspective: for the LM101A, $I_1 \cong 10\ \mu A$, $I_2 \cong 300\ \mu A$, $\beta_5 = \beta_6 \cong 150$, and $\beta_7 \cong 50$. From (1) and dc voltage gain with $R_L = 2\ k\Omega$ is

$$A_V(0) \cong 625\ 000. \tag{2}$$

The number predicted by (2) agrees well with that measured on a discrete breadboard of the LM101A, but is much higher than that observed on the integrated circuit. The reason for this is explained in the next section.

### *B. Thermal Feedback Effects on Gain*

The typical IC op amp is capable of delivering powers of 50–100 mW to a load. In the process of delivering this power, the output stage of the amp internally dissipates similar power levels, which causes the temperature of the IC chip to rise in proportion to the output dissipated power. The silicon chip and the package to which it is bonded are good thermal conductors, so the whole chip tends to rise to the same temperature as the output stage. Despite this, small temperature gradients from a few tenths to a few degrees centigrade develop across the chip with the output section being hotter than the rest. As illustrated in Fig. 4, these temperature gradients appear across the input components of the op amp and induce an input voltage which is proportional to the output dissipated power.

To a first order, it can be assumed that the temperature difference $(T_2\text{-}T_1)$ across a pair of matched and closely spaced components is given simply by

$$(T_2 - T_1) \cong \pm K_T P_d \quad °C \tag{3}$$

where

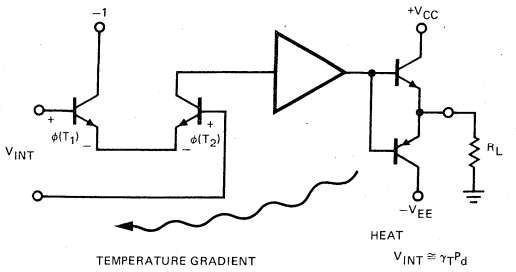



Fig. 4. Simple model illustrating thermal feedback in an IC op amp having a single dominant source of self-heat, the output stage. The constant $\gamma_T \cong 0.6$ mV/W and $P_d$ is power dissipated in the output. For simplicity, we ignore input drift due to uniform heating of the package. This effect can be significant if the input stage drift is not low, see [7].

$P_d$ power dissipated in the output circuit,
$K_T$ a constant with dimensions of °C/W.

The plus/minus sign is needed because the direction of the thermal gradient is unknown. In fact, the sign may reverse polarity during the output swing as the dominant source of heat shifts from one transistor to another. If the dominant input components consist of the differential transistor pair of Fig. 4, the thermally induced input voltage $V_{int}$ can be calculated as

$$V_{int} \cong \pm K_T P_d (2 \times 10^{-3})$$

$$\cong \pm \gamma_T P_d \tag{4}$$

where $\gamma_T = K_T(2 \times 10^{-3})$ V/W, since the transistor emitter-base drops change about $-2$ mV/°C.

For a thermally well designed IC op amp, in which the power output devices are made to approximate either a point or a line source and the input components are placed on the resulting isothermal lines (see below and Fig. 8), typical values measured for $K_T$ are

$$K_T \approx 0.3\ °C/W \tag{5}$$

in a TO-5 package.

The dissipated power in the class-AB output stage $P_d$ is written by inspection of Fig. 4:

$$P_d = \frac{V_0 V_s - V_0^2}{R_L} \tag{6}$$

where

$$V_s = +V_{cc} \quad \text{when } V_0 > 0$$

$$V_s = -V_{ee} \quad \text{when } V_0 < 0.$$

A plot of (6) in Fig. 5 resembles the well-known class-AB dissipation characteristics, with zero dissipation occurring for $V_0 = 0$, $+V_{cc}$, $-V_{ee}$. Dissipation peaks occur for $V_0 = +V_{cc}/2$ and $-V_{ee}/2$. Note also from (4) that the thermally induced input voltage $V_{int}$ has this same double-humped shape since it is just equal to a constant times $P_d$ at dc.

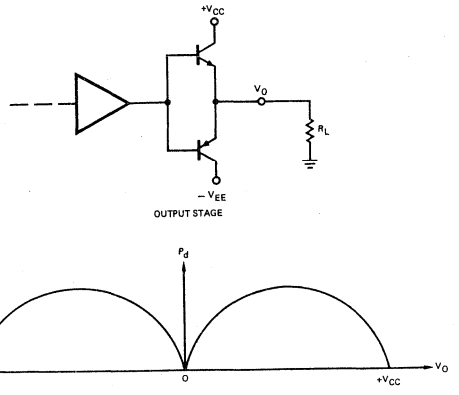



Fig. 5. Simple class-B output stage and plot of power dissipated in the stage, $P_d$, assuming device can swing to the power supplies. Equation (6) gives an expression for the plot.

Now examine Figs. 6(a) and (b) which are curves of open-loop $V_0$ versus $V_{in}$ for the IC op amp. Note first that the overall curve can be visualized to be made up of two components: a) a normal straight line electrical gain curve of the sort expected from (1) and b) a double-humped curve similar to that of Fig. 5. Further, note that the gain characteristic has either positive or negative slope depending on the value of output voltage. This means that the thermal feedback causes the open-loop gain of the feedback amplifier to change phase by 180°, apparently causing negative feedback to become positive feedback. If this is really true, the question arises: which input should be used as the inverting one for feedback? Further, is there any way to close the amplifier and be sure it will not find an unstable operating point and latch to one of the power supplies?

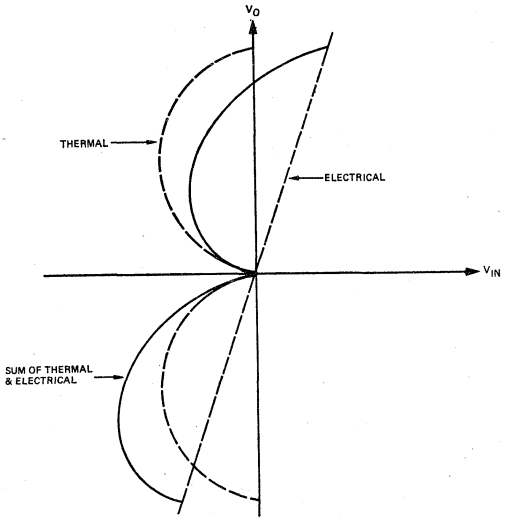
The answers to these questions can be found by studying a simple model of the op amp under closed-loop conditions, including the effects of thermal coupling. As shown in Fig. 7, the thermal coupling can be visualized as just an additional feedback path which acts in parallel with the normal electrical feedback. Noting that the electrical form of the thermal feedback factor is [see (4) and (6)]

$$\beta_T = \frac{\partial V_{\text{int}}}{\partial V_0} = \pm\frac{\gamma_T}{R_L}(V_S - 2V_0). \tag{7}$$

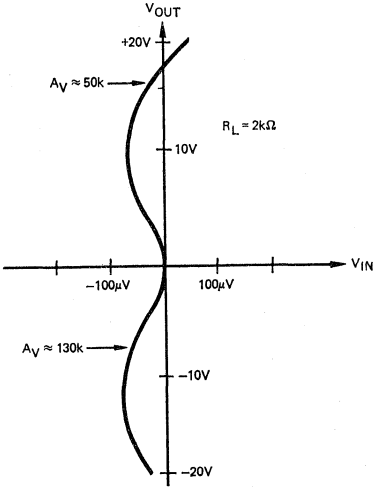
The closed-loop gain, including thermal feedback is

$$A_V(0) = \frac{\mu}{1 + \mu(\beta_e \pm \beta_T)} \tag{8}$$

where $\mu$ is the open-loop gain in the absence of thermal feedback [(1)] and $\beta_e$ is the applied electrical feedback as in Fig. 7. Inspection of (8) confirms that as long as there is sufficient electrical feedback to swamp the thermal feedback (i.e., $\beta_e > \beta_T$), the amplifier will behave as a normal closed-loop device with characteristics determined principally by the electrical feedback (i.e., $A_V(0) \cong 1/\beta_e$). On the other hand, if $\beta_e$ is small or nonexistant, the thermal term in (8) may dominate, giving an apparent open-loop gain characteristic determined by the thermal feedback factor $\beta_T$. Letting $\beta_e = 0$ and combining (7) and (8), $A_V(0)$ becomes




(a)




(b)

Fig. 6. (a) Idealized dc transfer curve for an IC op amp showing its electrical and thermal components. (b) Experimental open-loop transfer curve for a representative op amp (LM 101).

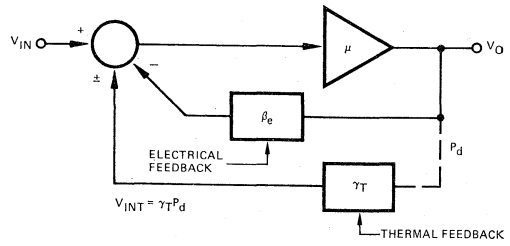



Fig. 7. Diagram used to calculate closed-loop gain with thermal feedback.

$$A_V(0) = \frac{\mu}{1 \pm \frac{\mu\gamma_T}{R_L}(V_S - 2V_0)}. \tag{9}$$

Recalling from (6) that $V_0$ ranges between 0 and $V_S$, we note that the incremental thermal feedback is greatest when $V_0 = 0$ or $V_s$, and it is at these points that the thermally limited gain is smallest. To use the amplifier in a predictable manner, one must always apply enough electrical feedback to reduce the gain below this minimum thermal gain. Thus, a *maximum usable gain* can be defined as that approximately equal to the value of (9) with $V_0 = 0$ or $V_s$ which is

$$A_V(0)|_{\max} \cong \frac{R_L}{\gamma_T V_S} \tag{10}$$

or

$$A_V(0)|_{\max} \cong \frac{1}{\gamma_T I_{\max}}. \tag{11}$$

It was assumed in (10) and (11) that thermal feedback dominates over the open-loop electrical gain, $\mu$. Finally, in (11) a maximum current was defined $I_{\max} = V_S/R_L$ as the maximum current which would flow if the amplifier output could swing all the way to the supplies.

Equation (11) is a strikingly simple and quite general result which can be used to predict the expected maximum usable gain for an amplifier if we know only the maximum output current and the thermal feedback constant $\gamma_T$.

Recall that typically $K_T \cong 0.3°C/W$ and $\gamma_T = (2 \times 10^{-3})$ $K_T \cong 0.6$ mV/W. Consider, as as example, the standard IC op amp operating with power supplies of $V_S = \pm 15$ V and a minimum load of 2 kΩ, which gives $I_{\max} = 15$ V/2 kΩ = 7.5 mA. Then, from (11), the maximum thermally limited gain is about:

$$A_V(0)|_{\max} \cong 1/(0.6 \times 10^{-3})(7.5 \times 10^{-3})$$
$$\cong 220\,000. \tag{12}$$

Comparing (2) and (12), it is apparent that the thermal characteristics dominate over the electrical ones if the minimum load resistor is used. For loads of 6 kΩ or more, the electrical characteristics should begin to dominate

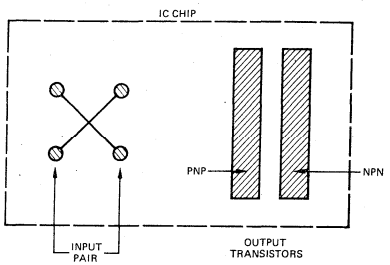



Fig. 8. One type layout in which a quad of input transistors is cross connected to reduce effect of nonuniform thermal gradients. The output transistors use distributed stripe geometries to generate predictable isothermal lines.

if thermal feedback from sources other than the output stage is negligible. It should be noted also that, in some high speed, high drain op amps, thermal feedback from the second stage dominates when there is no load.

As a second example, consider the so-called "power op amp" or high gain audio amp which suffers from the same thermal limitations just discussed. For a device which can deliver 1 W into a 16-Ω load, the peak output current and voltage are 350 mA and 5.7 V. Typically, a supply voltage of about 16 V is needed to allow for the swing loss in the IC output stage. $I_{\max}$ is then 8 V/16 Ω or 0.5 A. If the device is in a TO-5 package $\gamma_T$ is approximately 0.6 mV/W, so from (11) the maximum usable dc gain is

$$A_V(0)|_{\max} \cong \frac{1}{(0.6 \times 10^{-3})(0.5)} \cong 3300. \tag{13}$$

This is quite low compared with electrical gains of, say, 100 000 which are easily obtainable. The situation can be improved considerably by using a large die to separate the power devices from the inputs and carefully placing the inputs on constant temperature (isothermal) lines as illustrated in Fig. 8. If one also uses a power package with a heavy copper base, $\gamma_T$'s as low as 50 μV/W have been observed. For example, a well-designed 5-W amplifier driving an 8-Ω load and using a 24-V supply, would have a maximum gain of 13 000 in such a power package.

As a final comment, it should be pointed out that the most commonly observed effect of thermal feedback in high gain circuits is low frequency distortion due to the nonlinear transfer characteristic. Differential thermal coupling typically falls off at an initial rate of 6 dB/octave starting around 100–200 Hz, so higher frequencies are uneffected.

## III. Small-Signal Frequency Response

At higher frequencies where thermal effects can be ignored, the behavior of the op amp is dependent on purely electronic phenomena. Most of the important small and large signal performance characteristics of the classical IC op amp can be accurately predicted from

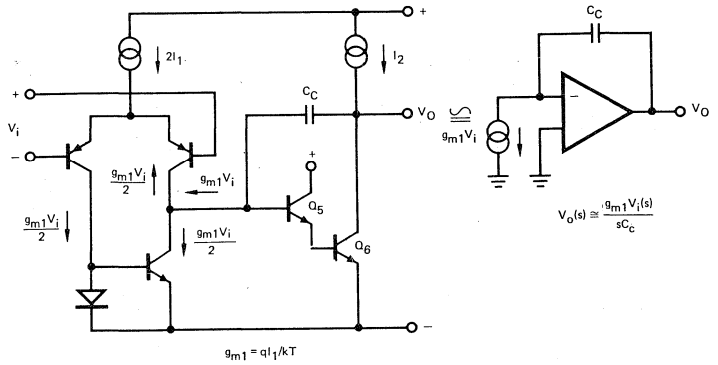



Fig. 9. First-order model of op amp used to calculate small signal high frequency gain. At frequencies of interest the input impedance of the second stage becomes low compared to first stage output impedance due to $C_c$ feedback. Because of this, first stage output impedance can be assumed infinite, with no loss in accuracy.

very simple first-order models for the amplifier in Fig. 1[8]. The small-signal model that is used assumes that the input differential amplifier and current mirror can be replaced by a frequency independent voltage controlled current source, see Fig. 9. The second stage consisting essentially of transistors $Q_5$ and $Q_6$, and the current source load, is modeled as an ideal frequency independent amplifier block with a feedback or "integrating capacitor" identical to the compensation capacitor, $C_c$. The output stage is assumed to have unity voltage gain and is ignored in our calculations. From Fig. 9, the high frequency gain is calculated by inspection:

$$A_v(\omega) = \left|\frac{v_0}{v_i}(s)\right| = \left|\frac{g_{m1}}{sC_c}\right| = \frac{g_{m1}}{\omega C_c} \tag{14}$$

where dc and low frequency behavior have not been included since this was evaluated in the last section. Fig. 10 is a plot of the gain magnitude as predicted by (14). From this figure it is a simple matter to calculate the open-loop unity gain frequency $\omega_u$, which is also the gain-bandwidth product for the op amp under closed-loop conditions:

$$\omega_u = \frac{g_{m1}}{C_c}. \tag{15}$$

In a practical amplifier, $\omega_u$ is set to a low enough frequency (by choosing a large $C_c$) so that negligible excess phase over the 90° due to $C_c$ has built up. There are numerous contributors to excess phase including low $f_t$ p-n-p's, stray capacitances, nondominant second stage poles, etc. These are discussed in more detail in a later section, but for now suffice it to say that, in the simple IC op amp, $\omega_u/2\pi$ is limited to about 1 MHz. As a simple test of (15), the LM101 or the $\mu$A741 has a first stage bias current $I_1$ of 10 $\mu$A per side, and a compensation capacitor for unity gain operation, $C_c$, of 30 pF. These amplifiers each have a first stage $g_m$ which is half that

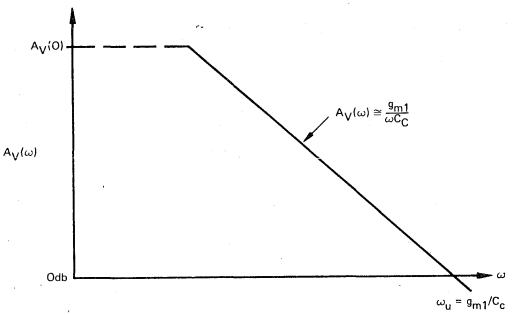



Fig. 10. Plot of open-loop gain calculated from model in Fig. 9. The dc and LF gain are given by (1), or (11) if thermal feedback dominates.

of the simple differential amplifier in Fig. 1 so $g_{m1} = qI_1/2kT$. Equation (15) then predicts a unity gain corner of

$$f_u = \frac{\omega_u}{2\pi} = \frac{g_{m1}}{2\pi C_c} = \frac{(0.192 \times 10^{-3})}{2\pi(30 \times 10^{-12})} = 1.02 \text{ MHz} \tag{16}$$

which agrees closely with the measured values.

## IV. Slew Rate and Some Special Limits

### A. A General Limit on Slew Rate

If an op amp is overdriven by a large-signal pulse or square wave having a fast enough rise time, the output does not follow the input immediately. Instead, it ramps or "slews" at some limiting rate determined by internal currents and capacitances, as illustrated in Fig. 11. The magnitude of input voltage required to make the amplifier reach its maximum slew rate varies, depending on the type of input stage used. For an op amp with a

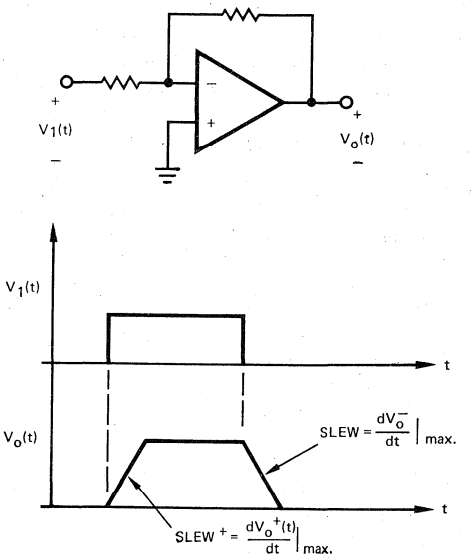



Fig. 11. Large signal "slewing" response observed if the input is overdriven.

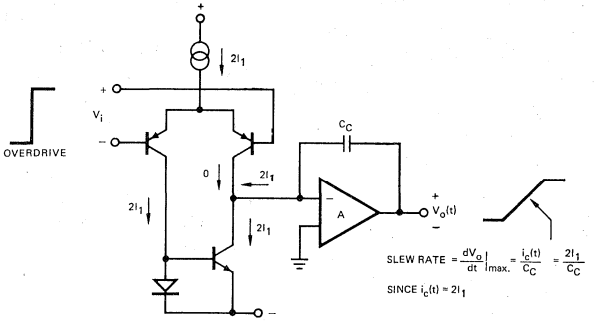



Fig. 12. Model used to calculate slew rate for the amp of Fig. 1 in the inverting mode. For simplicity, all transistor $\alpha$'s are assumed equal to unity, although results are essentially independent of $\alpha$. An identical slew rate can be calculated for a negative-going output, obtained if the applied input polarity is reversed.

simple input differential amp, an input of about 60 mV will cause the output to slew at 90 percent of its maximum rate, while a $\mu$A741, which has half the input $g_m$, requires 120 mV. High speed amplifiers such as the LM 118 or a FET-input circuit require much greater overdrive, with 1–3 V being common. The reasons for these overdrive requirements will become clear below.

An adequate model to calculate slew limits for the representative op amp in the inverting mode is shown in Fig. 12, where the only important assumption made is that $I_2 \geq 2I_1$ in Fig. 1. This condition always holds in a well-designed op amp. (If one lets $I_2$ be less than $2I_1$, the slew is limited by $I_2$ rather than $I_1$, which results in lower speed than is otherwise possible.) Fig. 12 requires some modification for noninverting operation, and we will study this later.

The limiting slew rate is now calculated from Fig. 12. Letting the input voltage be large enough to fully switch the input differential amp, we see that all of the first stage tail current $2I_1$ is simply diverted into the integrator consisting of $A$ and $C_c$. The resulting slew rate is then:

$$\text{slew rate} = \left.\frac{dv_0}{dt}\right|_{\max} = \frac{i_c(t)}{C_c}. \tag{17}$$

Noting that $i_c(t)$ is a constant $2I_1$, this becomes

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2I_1}{C_c}. \tag{18}$$

As a check of this result, recall that the $\mu$A741 has $I_1 = 10\ \mu$A and $C_1 = 30$ pF, so we calculate:

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2 \times 10^{-5}}{30 \times 10^{-12}} = 0.67\ \frac{\text{V}}{\mu\text{s}} \tag{19}$$

which agrees with measured values.

The large and small signal behavior of the op amp can be usefully related by combining (15) for $\omega_u$ with (18). The slew rate becomes

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2\omega_u I_1}{g_{m1}}. \tag{20}$$

Equation (20) is a general and very useful relationship. It shows that, for a given unity-gain frequency, $\omega_u$, the slew rate is determined entirely by just the ratio of first stage operating current to first stage transconductance, $I_1/g_{m1}$. Recall that $\omega_u$ is set at the point where excess phase begins to build up, and this point is determined largely by technology rather than circuit limitations. Thus, the only effective means available to the circuit designer for increasing op amp slew rate is to *decrease* the ratio of first stage transconductance to operating current, $g_{m1}/I_1$.

### *B. Slew Limiting for Simple Bipolar Input Stage*

The significance of (20) is best seen by considering the specific case of a simple differential bipolar input as in Fig. 1. For this circuit, the first stage transconductance (for $\alpha_1 = 1$) is[1]

$$g_{m1} = qI_1/kT \tag{21}$$

so that

$$\frac{g_{m1}}{I_1} = q/kT. \tag{22}$$

Using this in (20), the maximum bipolar slew rate is

$$\left.\frac{dv_0}{dt}\right|_{\max} = 2\omega_u \frac{kT}{q}. \tag{23}$$

This provides us with the general (and somewhat dismal) conclusion that slew rate in an op amp with a simple bipolar input stage is dependent only upon the unity gain corner and fundamental constants. Slew rate can be increased only by increasing the unity gain corner, which we have noted is generally difficult to do. As a demonstration of the severity of this limit, imagine an op amp using highly advanced technology and clever design, which might have a stable unity gain frequency of 100 MHz. Equation (23) predicts that the slew rate for this advanced device is only

$$\left.\frac{dv_0}{dt}\right|_{\max} = 33\ \frac{\text{V}}{\mu\text{s}} \tag{24}$$

which is good, but hardly impressive when compared with the difficulty of building a 100-MHz op amp.[2] But, there are some ways to get around this limit as we shall see shortly.

### *C. Power Bandwidth*

Our intuition regarding slew rate will be enhanced somewhat if we relate it to a term called "power bandwidth." Power bandwidth is defined as the maximum frequency at which full output swing (usually 10 V peak) can be obtained without distortion. For a sinusoidal output voltage $v_0(t) = V_p \sin \omega t$, the rate of change of output, or slew rate, required to reproduce the output is

$$\frac{dv_0}{dt} = \omega V_p \cos \omega t. \tag{25}$$

This has a maximum when $\cos \omega t = 1$ giving

$$\left.\frac{dv_0}{dt}\right|_{\max} = \omega V_p, \tag{26}$$

so the highest frequency that can be reproduced without slew limiting, $\omega_{\max}$ (power bandwidth) is

$$\omega_{\max} = \frac{1}{V_p}\left.\frac{dv_0}{dt}\right|_{\max}. \tag{27}$$

Thus, power bandwidth and slew rate are directly related by the inverse of the peak of the sine wave $V_p$. Fig. 13 shows the severe distortion of the output sine wave which results if one attempts to amplify a sine wave of frequency $\omega > \omega_{\max}$.

Some numbers illustrate typical op amp limits. For a $\mu$A741 or LM101 having a maximum slew rate of 0.67 V/$\mu$s, (27) gives a maximum frequency for an undistorted 10-V peak output of

$$f_{\max} = \frac{\omega_{\max}}{2\pi} = 10.7\ \text{kHz}, \tag{28}$$

which is a quite modest frequency considering the much higher frequency small signal capabilities of these devices. Even the highly advanced 100-MHz amplifier considered above has a 10-V power bandwidth of only 0.5 MHz, so it is apparent that a need exists for finding ways to improve slew rate.

### *D. Techniques for Increasing Slew Rate*

*1) Resistive Enhancement of the Bipolar Stage:* Equation (20) indicates that slew rate can be improved if we reduce first stage $g_{m1}/I_1$. One of the most effective ways

[1] Note that (21) applies only to the simple differential input stage of Fig. 12. For compound input stages as in the LM101 or $\mu$A741, $g_{m1}$ is half that in (21), and the slew rate in (23) is doubled.

[2] We assume in all of these calculations that $C_c$ is made large enough so that the amplifier has less than 180° phase lag at $\omega_u$, thus making the amplifier stable for unity closed-loop gain. For higher gains one can of course reduce $C_c$ (if the IC allows external compensation) and increase the slew rate according to (18).

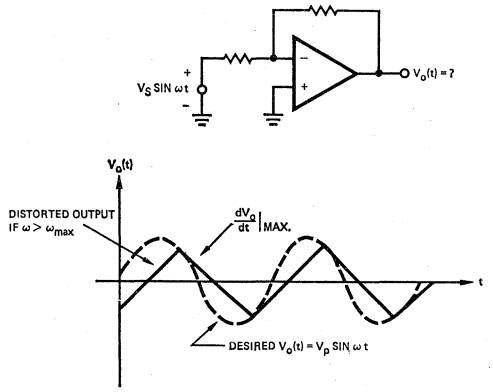



Fig. 13. Slew limiting effects on output sinewave that occur if frequency is greater than power bandwidth, $\omega_{max}$. The onset of slew limiting occurs very suddenly as $\omega$ reaches $\omega_{max}$. No distortion occurs below $\omega_{max}$, while almost complete triangularization occurs at frequencies just slightly above $\omega_{max}$.

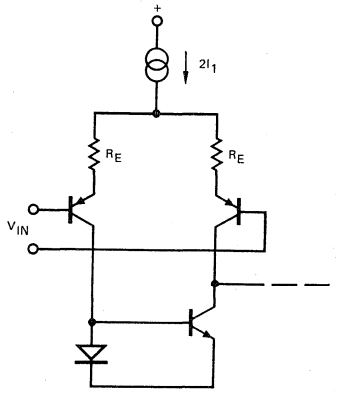



Fig. 14. Resistive degeneration used to provide slew rate enhancement according to (29).

of doing this is shown in Fig. 14, where simple resistive emitter degeneration has been added to the input differential amplifier [8]. With this change, the $g_{m1}/I_1$ drops to

$$\frac{g_{m1}}{I_1} = \frac{38.5}{1 + R_E I_1/26\text{ mV}} \tag{29}$$

at 25°C.

The quantity $g_{m1}/I_1$ is seen to decrease rapidly with added $R_E$ as soon as the voltage drop across $R_E$ exceeds 26 mV. The LM118 is a good example of a bipolar amplifier which uses emitter degeneration to enhance slew rate [4]. This device uses emitter resistors to produce $R_E I_1 = 500$ mV, and has a unity gain corner of 16 MHz. Equations (20) and (29) then predict a maximum inverting slew rate of

$$\left.\frac{dv_0}{dt}\right|_{max} = 2\omega_u \frac{I_1}{g_{m1}} = \omega_u = 100\,\frac{\text{V}}{\mu\text{s}} \tag{30}$$

which is a twenty-fold improvement over a similar amplifier without emitter resistors.

A penalty is paid in using resistive slew enhancement, however. The two added emitter resistors must match extremely well or they add voltage offset and drift to the input. In the LM118, for example, the added emitter $R$'s have values of 2.0 kΩ each and these contribute an input offset of 1 mV for each 4 Ω (0.2 percent) of mismatch. The thermal noise of the resistors also unavoidably degrades noise performance.

*2) Slew Rate in the FET Input Op Amp:* The FET (JFET or MOSFET) has a considerably lower transconductance than a bipolar device operating at the same current. While this is normally considered a drawback of the FET, we note that this "poor" behavior is in fact highly desirable in applications to fast amplifiers. To illustrate, the drain current for a JFET in the "current saturation" region can be approximated by

$$I_D \cong I_{DSS}(V_{GS}/V_T - 1)^2 \tag{31}$$

where

$I_{DSS}$ the drain current for $V_{GS} = 0$,
$V_{GS}$ the gate source voltage having positive polarity for forward gate-diode bias,
$V_T$ the threshold voltage having negative polarity for JFET's.

The small-signal transconductance is obtained from (31) as $g_m = \partial I_D/\partial V_G$. Dividing by $I_D$ and simplifying, the ratio $g_m/I_D$ for a JFET is

$$\frac{g_m}{I_D} \cong \frac{2}{(V_{GS} - V_T)} = \frac{2}{-V_T}\left[\frac{I_{DSS}}{I_D}\right]^{1/2}. \tag{32}$$

Maximum amplifier slew rate occurs for minimum $g_m/I_D$ and, from (32), this occurs when $I_D$ (or $V_{GS}$) is maximum. Normally it is impractical to forward bias the gate junction so a practical minimum occurs for (32) when $V_{GS} \cong 0$ V and $I_D \cong I_{DSS}$. Then

$$\left.\frac{g_m}{I_D}\right|_{min} \cong -\frac{2}{V_T}. \tag{33}$$

Comparing (33) with the analogous bipolar expression, (22), we find from (20) that the JFET slew rate is greater than bipolar by the factor

$$\frac{\text{JFET slew}}{\text{bipolar slew}} \approx \frac{-V_T}{2kT/q}\,\frac{\omega_{uf}}{\omega_{ub}} \tag{34}$$

where $\omega_{uf}$ and $\omega_{ub}$ are unity-gain bandwidths for JFET and bipolar amps, respectively. Typical JFET thresholds are around 2 V ($V_T = -2$ V), so for equal bandwidths (34) tells us that a JFET-input op amp is about forty times faster than a simple bipolar input. Further, if

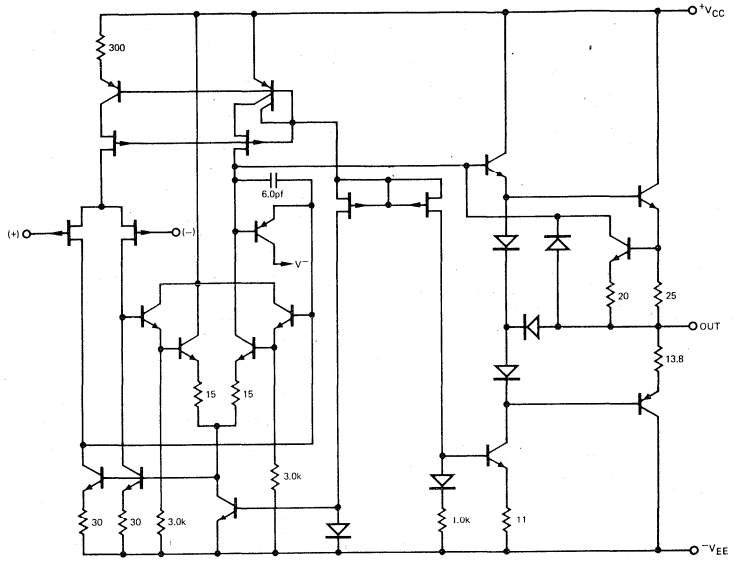



Fig. 15. Monolithic operational amplifier employing compatible p-channel JFET's on the same chip with normal bipolar components.

JFET's are properly substituted for the slow p-n-p's in a monolithic design, bandwidth improvements by at least a factor of ten are obtainable. JFET-input op amps, therefore, offer slew rate improvements by better than two orders of magnitude when compared with the conventional IC op amp. (Similar improvements are possible with MOSFET-input amplifiers.) This characteristic, coupled with picoamp input currents and reasonable offset and drift, make the JFET-input op amp a very desirable alternative to conventional bipolar designs.

As an example, Fig. 15, illustrates one design for an op amp employing compatible p-channel JFET's on the same chip with the normal bipolar components. This circuit exhibits a unity gain corner of 10 MHz, a 33 V/$\mu$s slew rate, an input current of 10 pA and an offset voltage and drift of 3 mV and 3 $\mu$V/°C [6]. Bandwidth and slew rate are thus improved over simple IC bipolar by factors of 10 and 100, respectively. At the same time input currents are smaller by about $10^3$, and offset voltages and drifts are comparable to or better than slew enhanced bipolar circuits.

## V. Second-Order Effects: Voltage Follower Slew Behavior

If the op amp is operated in the noninverting mode and driven by a large fast rising input, the output exhibits the characteristic waveform in Fig. 16. As shown, this waveform does not have the simple symmetrical slew characteristic of the inverter. In one direction, the output has a fast step (slew "enhancement") followed by a "normal" inverter slewing response. In the other direction, it suffers a slew "degradation" or reduced slope when compared with the inverter slewing response.

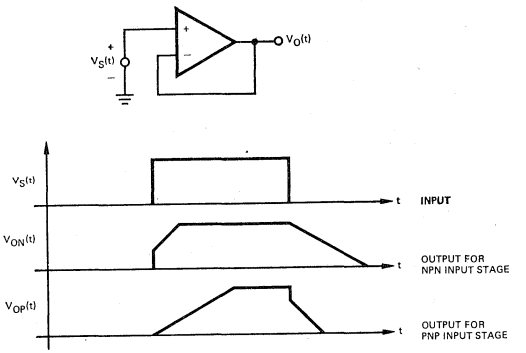



Fig. 16. Large signal response of the voltage follower. For an op amp with simple n-p-n input stage we get the waveform $v_{on}(t)$, which exhibits a step slew "enhancement" on the positive going output, and a slew "degradation" on the negative going output. For a p-n-p input stage, these effects are reversed as shown by $v_{op}(t)$.

We will first study slew degradation in the voltage follower connection, since this represents a worst case slewing condition for the op amp. A model which adequately represents the follower under large-signal conditions can be obtained from that in Fig. 12 by simply

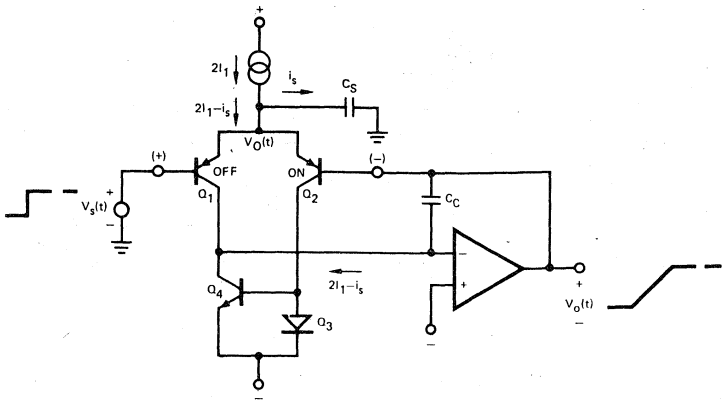



Fig. 17. Circuit used for calculation of slew "degradation" in the voltage follower. The degradation is caused by the capacitor $C_s$, which robs current from the tail, $2I_1$, thereby preventing the full $2I_1$ from slewing $C_c$.

tying the output to the inverting input, and including a capacitor $C_s$ to account for the presence of any capacitance at the output of the first stage (tail) current source, see Fig. 17. This "input tail" capacitance is important in the voltage follower because the input stage undergoes rapid large-signal excursions in this connection, and the charging currents in $C_s$ can be quite large.

Circuit behavior can be understood by analyzing Fig. 17 as follows. The large-signal input step causes $Q_1$ to turn OFF, leaving $Q_2$ to operate as an emitter follower with its emitter tracking the variational output voltage, $v_0(t)$. It is seen that $v_0(t)$ is essentially the voltage appearing across both $C_s$ and $C_c$ so we can write

$$\frac{dv_0}{dt} \cong \frac{i_c}{C_c} \cong \frac{i_s}{C_s}. \tag{35}$$

Noting that $i_c \cong 2I_1 - i_s$ (unity $\alpha$'s assumed), (35) can be solved for $i_s$:

$$i_s \cong \frac{2I_1}{1 + C_c/C_s} \tag{36}$$

which is seen to be constant with time. The degraded voltage follower slew rate is then obtained by substituting (36) into (35):

$$\left.\frac{dv_0}{dt}\right|_{\text{degr}} \cong \frac{i_s}{C_s} \cong \frac{2I_1}{C_c + C_s}. \tag{37}$$

Comparing (37) with the slew rate for the inverter, (18), it is seen that the slew rate is reduced by the simple factor $1/(1 + C_s/C_c)$. As long as the input tail capacitance $C_s$ is small compared with the compensation capacitor $C_c$, little degradation occurs. In high speed amplifiers where $C_c$ is small, degradation becomes quite noticeable, and one is encouraged to develop circuits with small $C_s$.

As an example, consider the relatively fast LM118 which has $C_c \cong 5$ pF, $C_s \cong 2$ pF, $2I_1 = 500$ $\mu$A. The calculated inverter slew rate is $2I_1/C_c \cong 100$ V/$\mu$s, and the degraded voltage follower slew rate is found to be $2I_1/(C_c + C_s) \cong 70$ V/$\mu$s. The slew degradation is seen to be about 30 percent, which is very significant. By contrast, a $\mu$A741 has $C_c \cong 30$ pF and $C_s \cong 4$ pF which results in a degradation of less than 12 percent.

The slew "enhanced" waveform can be similarly predicted from a simplified model. By reversing the polarity of the input and initially assuming a finite slope on the input step, the enhanced follower is analyzed, as shown in Fig. 18. Noting that $Q_1$ is assumed to be turned ON by the step input and $Q_2$ is OFF, the output voltage becomes

$$v_0(t) \cong -\frac{1}{C_c}\int_0^t [2I_1 + i_S(t)]\, dt. \tag{38}$$

The voltage at the emitter of $Q_1$ is essentially the same as the input voltage, $v_i(t)$, so the current in the "tail" capacitance $C_s$ is

$$i_s(t) \cong C_s \frac{dv_i}{dt} \cong \frac{C_s V_{ip}}{t_1} \qquad 0 < t < t_1. \tag{39}$$

Combining (38) and (39), $v_0(t)$ is

$$-v_0(t) \cong \frac{1}{C_c}\int_0^t 2I_1\, dt + \frac{1}{C_c}\int_0^{t_1} \frac{C_s V_{ip}}{t_1}\, dt \tag{40}$$

or

$$-v_0(t) \cong \frac{C_s}{C_c} V_{ip} + \frac{2I_1 t}{C_c}. \tag{41}$$

Equation (41) tells us that the output has an initial negative step which is the fraction $C_s/C_c$ of the input voltage. This is followed by a normal slewing response, in which the slew rate is identical to that of the inverter, see (18). This response is illustrated in Fig. 18.

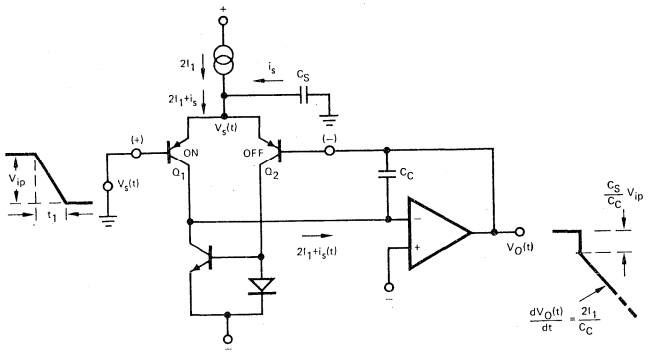



Fig. 18. Circuit used for calculation of slew "enhancement" in the voltage follower. The fast falling input causes a step output followed by a normal slew response as shown.

## VI. Limitations on Bandwidth

In earlier sections, all bandlimiting effects were ignored except that of the compensation capacitor, $C_c$. The unity-gain frequency was set at a point sufficiently low so that negligible excess phase (over the 90° from the dominant pole) due to second-order (high frequency) poles had built up. In this section the major second-order poles which contribute to bandlimiting in the op amp are identified.

### *A. The Input Stage: p-n-p's, the Mirror Pole, and the Tail Pole*

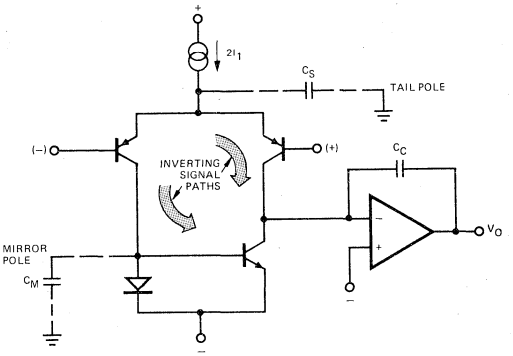
For many years it was popular to identify the lateral p-n-p's (which have $f_t$'s $\cong$ 3 MHz) as the single dominant source of bandlimiting in the IC op amp. It is quite true that the p-n-p's do contribute significant excess phase to the amplifier, but it is not true that they are the sole contributor to excess phase [9]. In the input stage, alone, there is at least one other important pole, as illustrated in Fig. 19(a). For the simple differential input stage driving a differential-to-single ended converter ("mirror" circuit), it is seen that the inverting signal (which is the feedback signal) follows two paths, one of which passes through the capacitance $C_s$, and the other through $C_m$. These capacitances combine with the dynamic resistances at their nodes to form poles designated the mirror pole at

$$p_m \cong \frac{I_1}{C_m kT/q}, \tag{42}$$

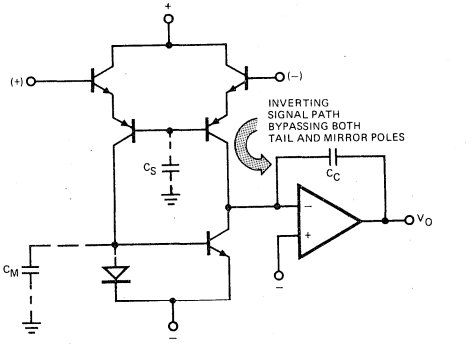
and the tail pole at

$$p_t \cong \frac{2I_1}{C_s kT/q}. \tag{43}$$

It can be seen that if one attempts to operate the first stage at too low a current, these poles will bandlimit the amplifier. If, for example, we choose $I_1 = 1$ $\mu$A, and assume $C_m \cong 7$ pF (consisting of 4-pF isolation ca-




(a)




(b)

Fig. 19. (a) Circuit showing "mirror" pole due to $C_m$ and "tail" pole due to $C_s$. One component of the signal due to an inverting input must pass through either the mirror or tail poles. (b) Alternate circuit to Fig. 19(a) (LM101, $\mu$A741) which has less excess phase. Reason is that half the inverting signal path need not pass through the mirror pole or the tail pole.

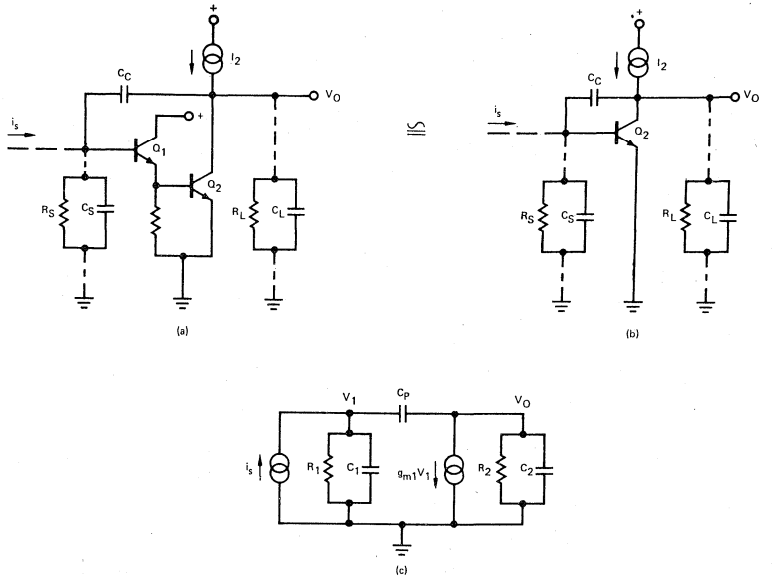



Fig. 20. Simplification of second stage used for pole-splitting analysis. (a) Complete second stage with input stage and output stage loading represented by $R_s$, $C_s$, and $R_L$, $C_L$, respectively. (b) Emitter follower ignored to simplify analysis. (c) Hybrid $\pi$ model substituted for transistor in (b). Source and load impedances are absorbed into model with the total impedances represented by $R_1$, $C_1$, and $R_2$, $C_2$. Transistor base resistance is ignored and $C_p$ includes both $C_c$ and transistor collector-base capacitance.

pacitance and 3-pF emitter transition capacitance) and $C_s \cong 4$ pF,[3] $p_m/2\pi \cong 0.9$ MHz and $p_t/2\pi \cong 3$ MHz either of which would seriously degrade the phase margin of a 1-MHz amplifier.

If a design is chosen in which either the tail pole or the mirror pole is absent (or unimportant), the remaining pole rolls off only half the signal, so the overall response contains a pole-zero pair separated by one octave. Such a pair generally has a small effect on amplifier response unless it occurs near $\omega_u$, where it can degrade phase margin by as much as 20°.

It is interesting to note that the compound input stage of the classical LM101 (and $\mu$A741) has a distinct advantage over the simple differential stage, as seen in Fig. 19(b). This circuit is noninverting across each half, thus it provides a path in which half the feedback signal bypasses both the mirror and tail poles.

[3] $C_s$ can have a wide range of values depending on circuit configuration. It is largest for n-p-n input differential amps since the current source has a collector-substrate capacitance ($C_s \cong$ 3–4 pF) at its output. For p-n-p input stages it can be as small as 1–2 pF.

*B. The Second Stage: Pole Splitting*

The assumption was made in Section III that the second stage behaved as an ideal integrator having a single dominant pole response. In practice, one must take care in designing the second stage or second-order poles can cause significant deviation from the expected response. Considerable insight into the basic way in which the second stage operates can be obtained by performing a small-signal analysis on a simplified version of the circuit as shown in Fig. 20 [10]. A straightforward two-node analysis of Fig. 20(c) produces the following expression for $v_{out}$.

$$\frac{v_{out}}{i_s} = \frac{-g_m R_1 R_2 (1 - sC_p/g_m)}{1 + s[R_1(C_1 + C_p) + R_2(C_2 + C_p) + g_m R_1 R_2 C_p] + s^2 R_1 R_2 [C_1 C_2 + C_p(C_1 + C_2)]}. \quad (44)$$

The denominator of (44) can be approximately factored under conditions that its two poles are widely separated. Fortunately, the poles are, in fact, widely separated under most normal operating conditions. Therefore, one can assume that the denominator of (44) has the form

$$D(s) = (1 + s/p_1)(1 + s/p_2)$$
$$= 1 + s(1/p_1 + 1/p_2) + s^2/p_1 p_2. \quad (45)$$

With the assumption that $p_1$ is the dominant pole and

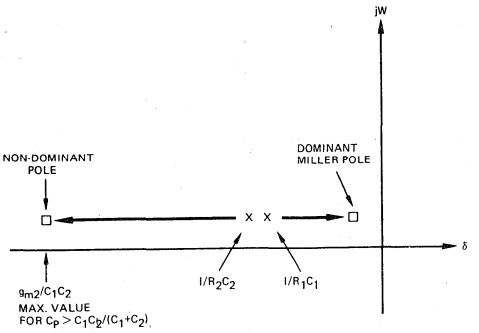



Fig. 21. Pole migration for second stage employing "pole-splitting" compensation. Plot is shown for increasing $C_p$ and it is noted that the nondominant pole reaches a maximum value for large $C_p$.

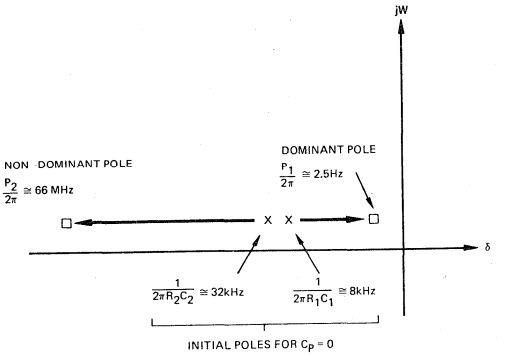



Fig. 22. Example of pole-splitting compensation in the μA741 op amp. Values used in (48) and (49) are: $g_{m2} = 1/87\ \Omega$, $C_p = 30$ pF, $C_1 \cong C_2 = 10$ pF, $R_1 = 1.7$ MΩ, $R_2 = 100$ kΩ.

$p_2$ is nondominant, i.e., $p_1 \ll p_2$, (45) becomes

$$D(s) \cong 1 + s/p_1 + s^2/p_1p_2. \tag{46}$$

Equating coefficients of $s$ in (44) and (46), the dominant pole $p_1$ is found directly:

$$p_1 \cong \frac{1}{R_1(C_1 + C_p) + R_2(C_2 + C_p) + g_mR_1R_2C_p} \tag{47}$$

$$\cong \frac{1}{g_mR_1R_2C_p}. \tag{48}$$

The latter approximation, (48), normally introduces little error, because the $g_m$ term is much larger than the other two. We note at this point that $p_1$, which represents the dominant pole of the amplifier, is due simply to the familiar Miller-multiplied feedback capacitance $g_mR_2C_p$ combined with input node resistance, $R_1$. The nondominant pole $p_2$ is found similarly by equating $s^2$ coefficients in (44) and (46) to get $p_1p_2$, and dividing by $p_1$ from (48). The result is

$$p_2 \cong \frac{g_mC_p}{C_1C_2 + C_p(C_1 + C_2)}. \tag{49}$$

Several interesting things can be seen in examining (48) and (49). First, we note that $p_1$ is inversely proportional to $g_m$ (and $C_p$), while $p_2$ is directly dependent on $g_m$ (and $C_p$). Thus, as either $C_p$ or transistor gain are increased, the dominant pole decreases and the nondominant pole increases. The poles $p_1$ and $p_2$ are being "split-apart" by the increased coupling action in a kind of inverse root locus plot.

This *pole-splitting* action is shown in Fig. 21, where pole migration is plotted for $C_p$ increasing from 0 to a large value. Fig. 22 further illustrates the action by giving specific pole positions for the μA741 op amp. It is seen that the initial poles (for $C_p = 0$) are both in the tens of kilohertz region and these are predicted to reach 2.5 Hz ($p_1/2\pi$) and 66 MHz ($p_2/2\pi$) after compensation is applied. This result is, of course, highly satisfactory since the second stage now has a single dominant pole effective over a wide frequency band.

### C. Failure of Pole Splitting

There are several situations in which the application of pole-splitting compensation may not result in a single dominant pole response. One common case occurs in very wide-band op amps where the pole-splitting capacitor is small. In this situation the nondominant pole given by (49) may not become broadbanded sufficiently so that it can be ignored. To illustrate, suppose we attempt to minimize power dissipation by running the second stage of an LM118 (which has a small-signal bandwidth of 16 MHz) at 0.1 mA. For this op amp $C_p = 5$ pF, $C_1 \cong C_2 \cong 10$ pF. From (49), the nondominant pole is

$$\frac{p_2}{2\pi} \cong 16\ \text{MHz} \tag{50}$$

which lies right at the unity-gain frequency. This pole alone would degrade phase margin by 45°, so it is clear that we need to bias the second stage with a collector current greater than 0.1 mA to obtain adequate $g_m$. Insufficient pole-splitting can therefore occur; but the cure is usually a simple increase in second stage $g_m$.

A second type of pole-splitting failure can occur, and it is often much more difficult to cope with. If, for example, one gets over-zealous in his attempt to broadband the nondominant pole, he soon discovers that other poles exist within the second stage which can cause difficulties. Consider a more exact equivalent circuit for the second stage of Fig. 20(a) as shown in Fig. 23. If the follower is biased at low currents or if $C_p$, $Q_2$ $g_m$, and/or $r_x$ are high, the circuit can contain at least four important poles rather than the two considered in simple pole splitting. Under these conditions, we no longer have a response with just negative real poles as in Fig. 21, but observe a root locus of the sort shown in Fig. 24. It is seen in this case that the circuit contains a pair of com-

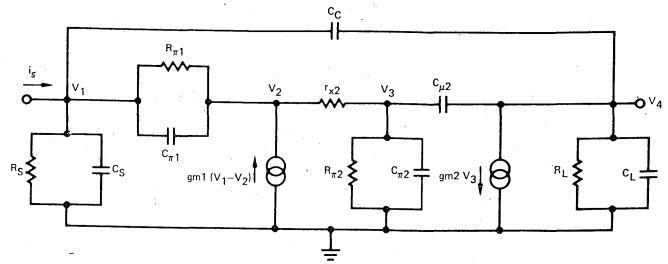



Fig. 23. More exact equivalent circuit for second stage of Fig. 20 (a) including a simplified $\pi$ model for the emitter follower ($R\pi_1$, $C\pi_1$, $g_{m1}$) and a complete $\pi$ for $Q_2$ ($r_{x2}$, $R\pi_2$, etc.).

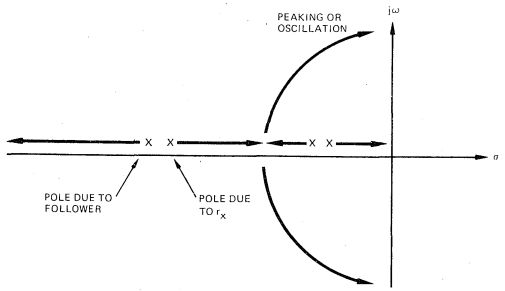



Fig. 24. Root locus for second stage illustrating failure of pole splitting due to high $g_{m2}$, $r_{x2}$, $C_p$, and/or low bias current in the emitter follower.

plex, possibly underdamped poles which, of course, can cause peaking or even oscillation. This effect occurs so commonly in the development of wide-band pole-split amplifiers that it has been (not fondly) dubbed "the second stage bump."

There are numerous ways to eliminate the "bump," but no single cure has been found which is effective in all situations. A direct hand analysis of Fig. 23 is possible, but the results are difficult to interpret. Computer analysis seems the best approach for this level of complexity, and numerous specific analyses have been made. The following is a list of circuit modifications that have been found effective in reducing the bump in the various studies: 1) reduce $g_{m2}$, $r_{x2}$, $C_{\mu 2}$, 2) add capacitance or a series $RC$ network from the stage input to ground—this reduces the high frequency local feedback due to $C_p$, 3) pad capacitance at the output for similar reasons, 4) increase operating current of the follower, 5) reduce $C_p$, 6) use a higher $f_t$ process.

### *D. Troubles in The Output Stage*

Of all the circuitry in the modern IC op amp, the class-AB output stage probably remains the most troublesome. None of the stages in use today behave as well as one might desire when stressed under worst case conditions. To illustrate, one of the most commonly used output stages is shown in Fig. 2(b). The p-n-p's in this circuit are "substrate" p-n-p's having low current $f_t$'s of around 20 MHz. Unfortunately, both $\beta_0$ and $f_t$ begin to fall off rapidly at quite low current densities, so as one begins to sink just a few milliamps in the circuit, phase margin troubles can develop. The worst effect occurs when the amplifier is operated with a large capacitive load (>100 pF) while sinking high currents. As shown in Fig. 25, the load capacitance on the output follower causes it to have negative input conductance, while the driver follower can have an inductive output impedance. These elements combine with the capacitance at the interstage to generate the equivalent of a one-port oscillator. In a carefully designed circuit, oscillation is suppressed, but peaking (the "output bump") can occur in most amplifiers under appropriate conditions.

One new type of output circuit which does not use p-n-p's is shown in Fig. 26 [6]. This circuit employs compatible JFET's (or MOSFET's, see similar circuit in [11]) in a FET/bipolar quasi-complimentary output stage, which is insensitive to load capacitance. Unfortunately, this circuit is rather complex and employs extra process steps, so it does not appear to represent the cure for the very low cost op amps.

## VII. The Gain Cell: Linear Large-Scale Integration

As the true limitations of the basic op amp are more fully understood, this knowledge can be applied to the development of more "optimum" amplifiers. There are, of course, many ways in which one might choose to optimize the device. We might, for example, attempt to maximize speed (bandwidth, slew rate, settling time) without sacrificing dc characteristics. The compatible JFET/bipolar amp of Fig. 15 represents such an effort. An alternate choice might be to design an amplifier having all of the performance features of the most widely used general purpose op amps (i.e., $\mu$A741, LM107, etc.), but having minimum possible die area. Such a pursuit is parallel to the efforts of digital large-scale integration (LSI) designers in their development of minimum area

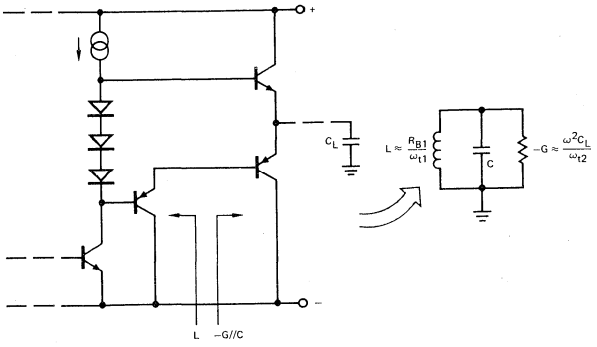



Fig. 25. Troubles in the conventional class-AB output stage of Fig. 2(b). The low $f_t$ output p-n-p's interact with load capacitance to form the equivalent of a one-port oscillator.

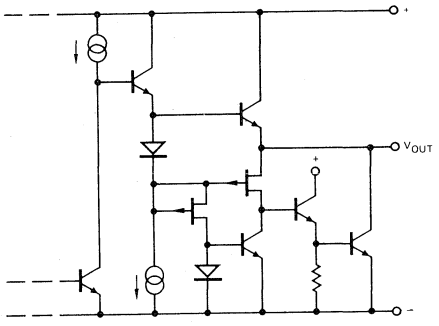



Fig. 26. The "BIFET" output stage employing JFET's and bipolar n-p-n's to eliminate sensitivity to load capacitance.

memory cells or gates. The object of such efforts, of course, is to develop lower cost devices which allow wide and highly economic usage.

In this section we briefly discuss certain aspects of the linear *gain cell*, a general purpose, internally compensated op amp having a die area which is significantly smaller than that of equivalent, present day, industry standard amplifiers.

### *A. Transconductance Reduction*

The single largest area component in the internally compensated op amp is the compensation capacitor (about 30 pF, typically). A major interest in reducing amplifier die area, therefore, centers about finding ways in which this capacitor can be reduced in size. With this in mind, we find it useful to examine (15), which relates compensation capacitor size to two other parameters, unity gain corner frequency $\omega_u$, and first stage transconductance $g_{m1}$. It is immediately apparent that for a fixed, predetermined unity gain corner (about $2\pi \times$ 1 MHz in our case), there is only one change that can be made to reduce the size of $C_c$: *the transconductance of the first stage must be reduced.* If we restrict our interest to simple bipolar input stages (for low cost), we recall the $g_{m1} = qI_1/kT$. Only by reducing $I_1$ can $g_{m1}$ be reduced, and we earlier found in Section VI–A and Fig. 19(a) and (b) that $I_1$ cannot be reduced much without causing phase margin difficulties due to the mirror pole and the tail pole.

An alternate basic approach to $g_m$ reduction is illustrated in Fig. 27 [12]. Here, a multiple collector p-n-p structure, which is easily fabricated in IC form, is used to split the collector current into two components, one component (the larger) of which is simply tied to ground, thereby "throwing away" a major portion of the transistor output current. The result is that the $g_m$ of the transistor is reduced by the ratio of $1/(1 + n)$ (see Fig. 27), and the compensation capacitance can be reduced directly by the same factor. It might appear that the mirror pole would still cause difficulties since the current mirror becomes current starved in Fig. 27, but the effect is not as severe as might be expected. The

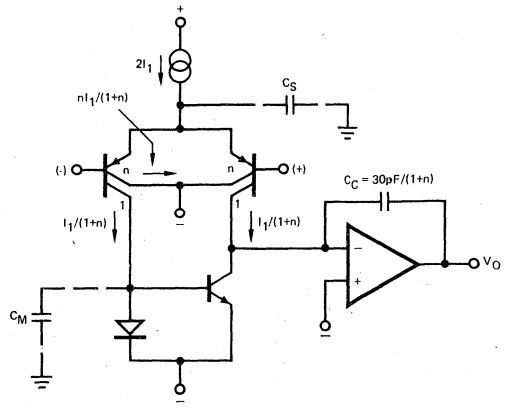



Fig. 27. Basic $g_m$ reduction obtained by using split collector p-n-p's. $C_c$ and area are reduced since $C_c = g_{m1}/\omega_u$.

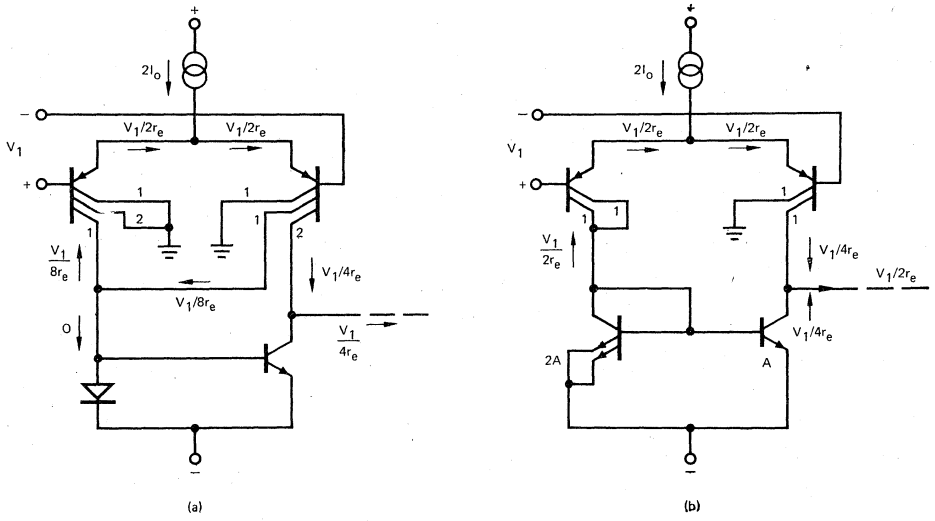



Fig. 28. Variations on $g_m$ reduction. (a) Cross-coupled connection eliminates all ac current passing through the mirror, yet maintains dc balance. (b) This approach maintains high current on the diode side of the mirror, thereby broadbanding the mirror pole.

reason is that the inverting signal can now pass through the high current wide-band path, across the differential amp emitters and into the second stage, so at least half the signal current does not become bandlimited. This partial bandlimiting can be further reduced by using one of the circuits in Fig. 28(a) or (b).[4] In (a), the p-n-p collectors are cross coupled in such a way that the ac signal is cancelled in the mirror circuit, while dc remains completely balanced. Thus the mirror pole is virtually eliminated. The circuit does have a drawback, however, in that the uncorrellated noise currents coming from the two p-n-p's add rather than subtract at the input to the mirror, thereby degrading noise performance. The circuit in Fig. 28(b) does not have this defect, but requires care in matching p-n-p collector ratios to n-p-n emitter areas. Otherwise offset and drift will degrade as one attempts to reduce $g_m$ by large factors.

### *B. A Gain Cell Example*

As one tries to make large reductions in die area for the gain cell, many factors must be considered in addition to novel circuit approaches. Of great importance are special layout/circuit techniques which combine a maximum number of components into minimum area.

[4] The circuit in Fig. 28(a) is due to R. W. Russell and the variation in Fig. 28(b) was developed by D. W. Zobel.

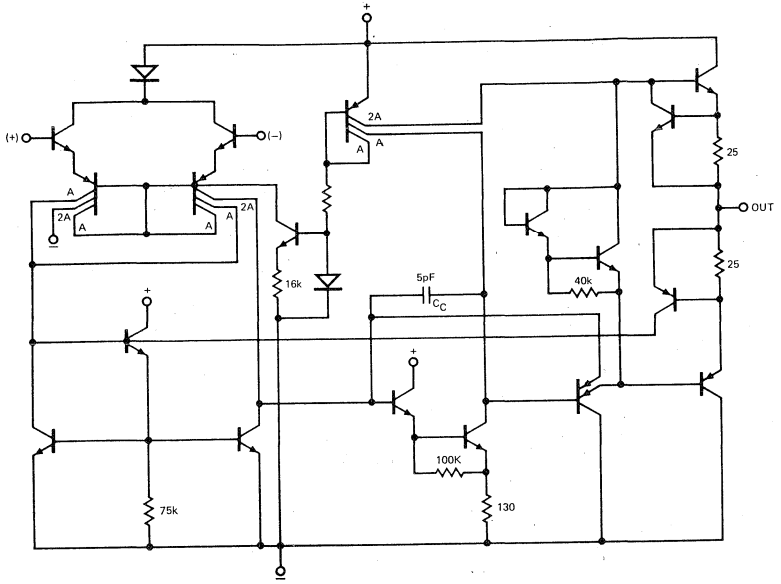



Fig. 29. Circuit for optimized gain cell which has been fabricated in one-fourth the die size of the equivalent μA741.

In a good layout, for example, all resistors are combined into islands with transistors. If this is not possible initially, circuit and device changes are made to allow it. The resulting device geometries within the islands are further modified in shape to allow maximum "packing" of the islands. That is, when the layout is complete, the islands should have shapes which fit together as in a picture puzzle, with no waste of space. Further area reductions can be had by modifying the isolation process to one having minimum spacing between the isolation diffusion and adjacent p-regions.

An example of a gain cell which employs both circuit and layout optimization is shown in Fig. 29. This circuit uses the $g_m$ reduction technique of Fig. 28(a) which results in a compensation capacitor size of only 5 pF rather than the normal 30 pF. The device achieves a full 1-MHz bandwidth, a 0.67-V/μs slew rate, a gain greater than 100 000, typical offset voltages less than 1 mV, and other characteristics normally associated with an LM107 or μA741. In quad form each amplifier requires an area of only 23 × 35 mils which is one-fourth the size of today's industry standard μA741 (typically 56 × 56 mils). This allows over 8000 possible gain cells to be fabricated on a single 3-inch wafer. Further, it appears quite feasible to fabricate larger arrays of gain cells, with six or eight on a single chip. Only packaging and applications questions need be resolved before pursuing such a step.


## Acknowledgment

Many important contributions were made in the gain cell and FET/bipolar op amp areas by R. W. Russell. The author gratefully acknowledges his very competent efforts.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Milt Wilcox
OCTOBER 1975

# A COLOR T.V. PRIMER FOR THE E.E.

## Section 1 — The Color TV Receiver

Let's look at a color TV in terms of signal flow, from antenna to picture tube.

Although the frequencies used will be for the American NTSC system (National Television System Committee), the basic theory also applies to the European PAL system (Phase Alternating Line). Only in the chroma section do the two systems differ significantly.

### RF AND IF SECTIONS

The first part is easy — all signal components received from the antenna pass through a tuner and IF amplifier to the video detector as shown in *Figure 1.*

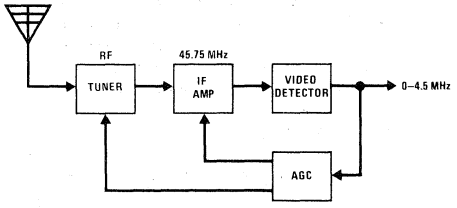


**FIGURE 1**

The RF signal received ranges in frequency from 55 MHz for channel 2 up to 885 MHz (tuned with the aid of a UHF converter) for channel 83! The tuner has the job of amplifying the desired channel frequency and converting it to an intermediate frequency (IF) of 45.75 MHz. It is then further amplified in the IF amplifier.

The 45.75 MHz signal being amplified is called the video carrier. It is amplitude-modulated (AM) with the picture information, so the video detector must strip this information from the carrier by using some form of envelope detection. So far we could be describing a basic AM radio, except for the signal being received — instead of having audio at the detector output, we have video.

The output level from the video detector is usually around 3 Vp-p. This level must be produced by as little as 10$\mu$Vrms on the antenna, which works out to 110 dB conversion gain for the three blocks shown in *Figure 1.* However, the catch is the same TV may have to receive antenna signals of up to 0.5 Vrms, and *still produce the same 3 Vp-p* at the video detector. For this reason, a TV has a very effective automatic gain control (AGC) system which detects increases in the peak amplitude of the composite video signal and automatically reduces the gain of the tuner and IF amplifier to compensate.

### SIGNAL INFORMATION

The picture you see on a color TV is actually formed by three electron beams, one each for red, blue and green being scanned horizontally and vertically over the screen. As these beams are scanned, their currents are changed to create the light and dark areas on the picture tube face which form the image you view. *Figure 2* shows the video detector output during the time that it takes the electron beams to make one horizontal scan across the screen. The output is actually a combination of four signal components which are required to form a color picture with sound. Let's look at them in turn:

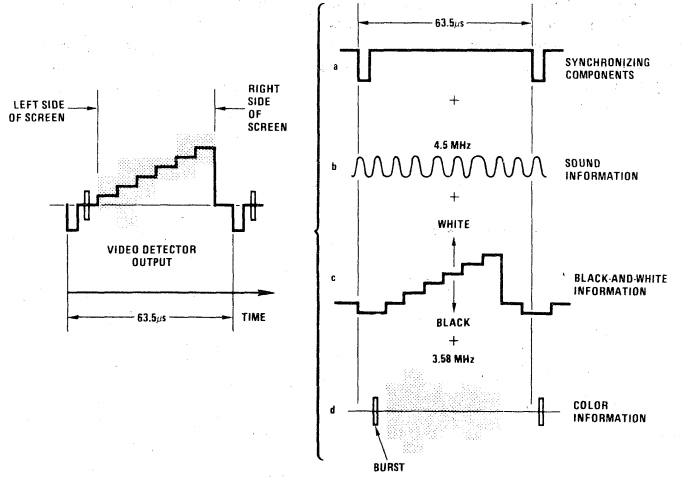


**FIGURE 2**

**a) Synchronizing Components**

The synchronizing information is a series of pulses which tell the horizontal section when to return to the left of the screen to start a new *line*, and the vertical section when to return to the top of the screen to start a new *frame*. In the NTSC system each frame contains 525 lines. This is done by scanning the horizontal at approximately 15,750 lines per second, and the vertical at 30 frames per second (the vertical scan rate is actually 60 Hz, but it takes two trips down the screen to complete one frame). The process of returning to start a new scan is called retrace or flyback.

**b) Sound Information**

The sound information is carried in the form of frequency-modulation (FM) of a 4.5 MHz carrier which in turn modulates the video carrier. (That makes the 4.5 MHz a "sub-carrier"). This sub-carrier is very similar to the IF signal in an FM radio. Although the sound sub-carrier is available at the video detector, a separate detector is often used to reduce crosstalk between signal components.

**c) Black-and-White Information** (called luminance)

This information determines the instantaneous brightness of the electron beams as they are scanned over the screen. In fact, it is all that is used for the single electron beam in a black-and-white TV set. A negative going video detector detects a luminance signal in which the negative signal extremes correspond to dark areas of the picture and positive signal extremes correspond to bright areas of the picture. Thus the waveform shown in *Figure 2(c)* would produce vertical bars of increasing brightness from left to right. Note that the output is at black during retrace so the electron beams will not be seen. The luminance signal is designated by the letter Y.

**d) Color Information** (called chrominance)

The color information (which is ignored in a black-and-white TV) is made up of the red, blue and green signals required to drive the picture tube, *minus* the luminance signal. These "color difference" signals, designated R-Y, B-Y and G-Y, modulate a second subcarrier which has a frequency of 3.58 MHz.

Although the type of modulation used on the sub-carrier is of a complex nature it boils down to a simple result:

1. The instantaneous *phase* of the 3.58 MHz signal determines *what* color will be displayed (called hue or tint).

2. The instantaneous *amplitude* of the 3.58 MHz signal determines *how much* color will be displayed (called saturation).

An obvious question is, the phase and amplitude of the 3.58 MHz signal relative to what? The answer is a short burst of 3.58 MHz (simply called the *burst*) which has constant phase and amplitude. The burst will be used to determine the tint and saturation of the color to be displayed. For the waveform shown in *Figure 2(d)* each bar would have a different saturation.

The four signal components are separated and sent to their respective sections in the TV according to the type of signal. Since the sync pulses are the negative peaks of the composite video signal, a peak-detector circuit called a *sync-separator* is used to separate them. The sound and chroma information is contained in sub-carriers which are separated with 4.5 MHz and 3.58 MHz tuned-circuits respectively. The luminance information combines frequency components from 0–4 MHz and therefore uses wideband dc-coupling.

## SIGNAL PROCESSING

The remaining sections of the Receiver will now be covered.

**Scanning and High Voltage**

The sync section is shown in *Figure 3.*

The sync pulses separated in the sync-separator are divided into vertical and horizontal components according to their pulse widths, the vertical sync pulse being a string of wide horizontal sync pulses. When these wide pulses are fed through an integrator, they average to form the vertical sync pulse. The vertical oscillator is "injection-locked" by the vertical sync pulse to initiate vertical retrace at the correct time. The output stage then delivers a ramp of current to the vertical deflection coils to produce vertical scan.

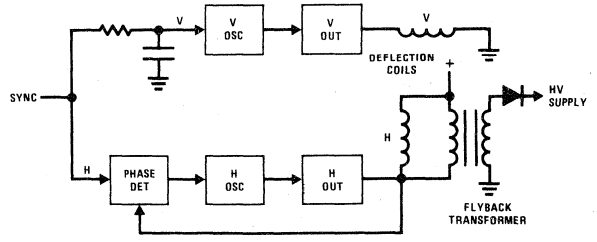


**FIGURE 3**

The horizontal section uses a different locking system, since horizontal retrace is started *before* the sync pulse is received in order to assure correct centering of the picture. This is done with a phase-locked loop (PLL) in which the oscillator is controlled by a phase detector to insure correct timing between the horizontal sync pulse and the flyback pulse produced by the output stage during horizontal retrace. The horizontal output stage does double duty – besides driving the horizontal deflection coils, it drives the flyback transformer for the picture tube anode high voltage supply. The 25–30 thousand volts dc required is generated either by directly rectifying or by tripling a hv flyback pulse derived from a large turns ratio on the flyback transformer.

**The Sound Channel**

The 4.5 MHz sound-subcarrier signal is amplified and limited in the sound IF to remove undesired amplitude information. The frequency modulation is then detected by an FM detector and applied to the audio amplifier.

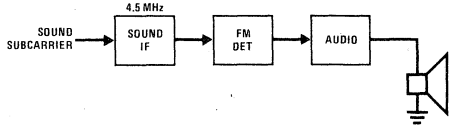


**FIGURE 4**

Limiting sensitivity for the sound section is typically 100μV and the output power requirement is from 1W to 4W depending on receiver size.

**Luma Processing**

The luminance signal Y must be amplified and delayed some 0.8μs on its way to the picture tube as shown in *Figure 5*. The delay is required to insure that the black and white information does not arrive at the picture tube before the color information, which is delayed by the comparatively narrow bandwidth of the 3.58 MHz chroma section.

The contrast and brightness controls are also located in the luminance amplifier. The *contrast* control changes the *peak-to-peak* amplitude of the signal, while the *brightness* control changes the *dc* level of the signal.

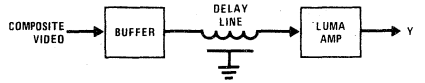


**FIGURE 5**

**Chroma Processing**

From the signal taken off the 3.58 MHz tuned circuit the chroma section must derive two signals:

1) The 3.58 MHz chroma sub-carrier signal of the correct amplitude and

2) A continuous 3.58 MHz chroma reference signal of the correct phase relative to the burst.

These two signals, when applied to the chroma demodulator, will produce the desired color difference signals R-Y, B-Y and G-Y. The chroma section is shown in *Figure 6*.

The first problem is that even though the AGC system holds the peak-to-peak video level constant, the chroma sub-carrier itself can vary in amplitude with transmission, antenna and fine-tuning changes, to name a few. Therefore, the chroma section requires an AGC loop of its own, which is called the Automatic Chroma Control stage, or ACC. This block compares the amplitude of the burst to a reference to keep the chroma output signal constant over a 20 dB input range.

The chroma signal is then gated into two components by a pulse derived from the horizontal section. The chroma sub-carrier (during horizontal scan) is sent to the chroma amplifier in which a gain control varies the saturation of the color picture. If *no* burst was present in the ACC stage, the output of the amplifier is "killed" completely for black and white reception.

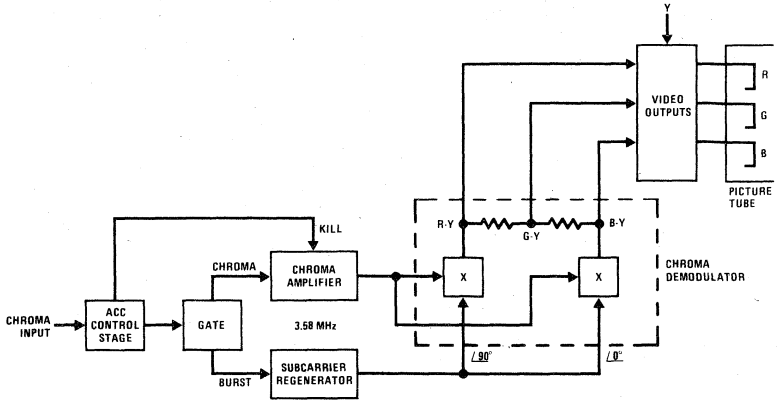


**FIGURE 6**

The burst (during horizontal retrace) is sent to the sub-carrier regenerator. This is actually a fancy name for a crystal-controlled 3.58 MHz oscillator which is locked to the frequency and phase of the incoming burst by either an injection-lock or phase-lock technique. This forms the reference output, which is passed through a variable phase-shift network to vary the tint of the color picture.

The outputs of the chroma amplifier and sub-carrier regenerator are the signals required by the chroma demodulator, which consists of two synchronous detectors operated in quadrature. What this means is that the reference phase applied to the B-Y detector makes it responsive only to chroma input phases corresponding to blue. The reference applied to the R-Y detector, which is 90° out of phase with the B-Y detector, makes it responsive only to red. The G-Y signal is derived by combining the R-Y and B-Y outputs in the correct ratios.

Finally, the luminance signal Y is added to the chroma difference signals R-Y, B-Y and G-Y to arrive at the desired red, blue and green signals. These signals are further amplified to 100 Vp-p in the video output stage and applied to the appropriate cathodes of the picture tube.

## CONVERGENCE

One other messy, but needed, function remains in a color TV receiver – color convergence. The need for convergence results from the origination of the three electron beams in different locations and the fact that they are being scanned over a flat, instead of round, surface. Therefore, the deflection of each beam must be modified separately such that it lands in the same location as the other beams over the entire face of the picture tube.

A complete block diagram of the color TV receiver is shown for reference in *Figure 7.*

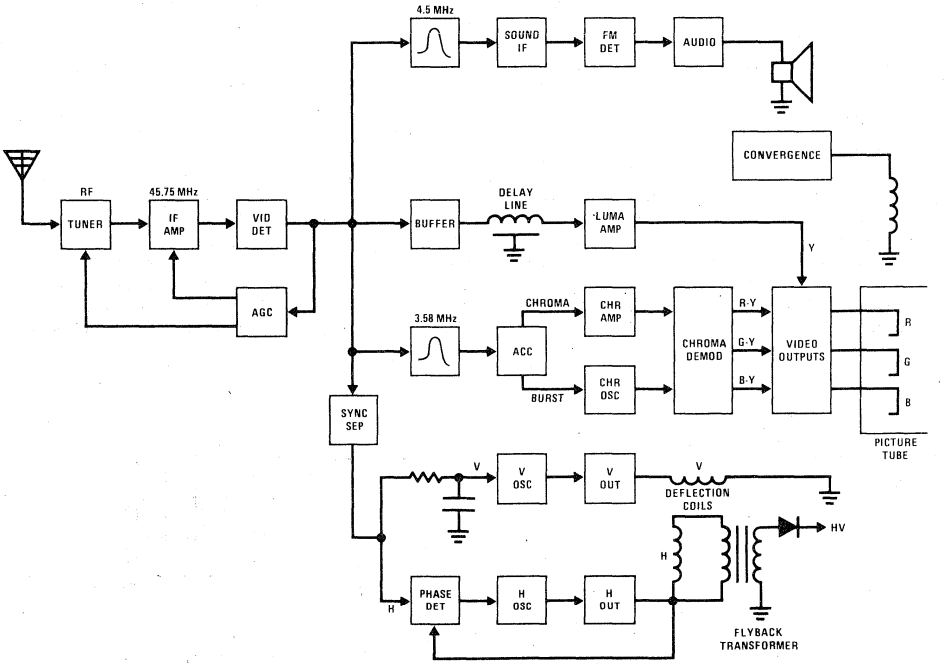


**FIGURE 7**

## Section 2 — Integrated Circuits in Television

Here we will look at the integrated circuits used in television including a glimpse inside TV ICs.

Every area of the television which does not have too high a frequency or voltage requirement has been integrated at least once, and many are on second and third generation IC's. The only areas that have been "off-limits" to date are the tuner, video outputs, and horizontal/HV output sections.

### RF AND IF SECTIONS

Monolithic circuits have been made to work very well at 45 MHz. The first IC IF systems used 2 chips: one for a 2-stage gain-controlled IF amplifier (Motorola MC1349, 52) and the second for a video detector with gain (Motorola MC1330). The major obstacle to combining these two chips into a single chip has been stability problems due to internal and/or external coupling output to input. However a one chip IF amplifier and video detector is now widely used in Europe (Telefunken TDA 440). The AGC system is also often included in these chips. Another IF function used in most color TV receivers today is automatic fine tuning (AFT) which keeps the tuner correctly tuned to the IF frequency (LM3064 type).

The first chip to incorporate all of the above functions into a single chip is the National LM1807. The chip uses a phase-locked loop to tune the tuner to the IF frequency set by a local oscillator on the chip. This concept is new to TV and is generating a lot of interest.

Rapid progress is also being made in periphery circuits to tuners. Present IC tuning systems control the voltage on a varactor in the tuner to tune the desired channel. However, new systems will actually "synthesize" the tuner local oscillator frequency for each channel.

### SCANNING

The deflection area is one of the last to be integrated. While only low-level horizontal circuits have been integrated, vertical drivers and even output stages have been attempted. Current IC's include the Motorola MC1391 or Philips TBA 920 for horizontal and the SGS TDS 1270 for vertical.

In the standard U.S. television system, the vertical and horizontal scanning frequencies are related by the formula $f_V = 2f_H/525$. The National DM8890 makes use of this fact by dividing down a horizontal signal to generate vertical timing, thus eliminating the need for a vertical hold control. Although previous combined vertical/horizontal chips have been unsuccessful, the digital approach holds much promise and TI has announced a combined chip using $I^2L$.

### THE SOUND CHANNEL

The LM3065 type sound IF/FM Detector is currently used in most TV receivers along with a class B discrete or IC audio amplifier. However, virtually every IC manufacturer has announced a one chip "sound system" combining the IF, detector, and audio amplifier. National's entry is the LM1808 which has been well received.

### LUMA PROCESSING

Standard IC's have not been developed for the Luma area because of questionable economics. Instead, most of the efforts so far have been custom, with different IC's being used by Zenith, Sylvania and several European TV companies.

### CHROMA PROCESSING

The first IC in TV was the chroma demodulator. Today every color TV has one, usually an LM746 or LM1828 type. In one variation the luminance signal is added to the color difference outputs on the chip (Motorola MC1324).

The chroma amplifier and subcarrier regenerator sections have been integrated using a phase-locked loop system with two chips (LM3070 and LM3071 types) and an injection-locked system with one chip (Motorola MC1398). Both of these systems are widely used. Second generation systems which do the phase-locked system with one chip (RCA CA3126 or Motorola MC1399) are gaining acceptance. All of these systems can be used with the above-mentioned demodulators.

Thus, so far the chroma section takes a minimum of two chips, including the demodulator. When will the demodulator be combined with the rest of the system for a true one-chip chroma? Hitachi has just introduced the first practical attempt and others are sure to follow.

### WHAT'S A JUNGLE?

A "jungle" IC is a combination of miscellaneous TV functions on one chip. For example, the Zenith jungle (LM1845 type) does the sync-separator and AGC functions. The term is also sometimes applied to deflection IC's which include other functions.

### INSIDE TV IC's

Next to the basic differential amplifier, the most widely used linear circuits in TV IC's are probably the current-sharing gain control stage and the linear multiplier.

#### Gain Control

The current-sharing gain control stage is so named because the input current is shared between two outputs depending on the dc control voltage $V_C$. For the circuit shown in *Figure 8,* the small signal gain at room temperature is given by:

$$A = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \cong \frac{R_L/R_e}{1 + \exp\left(\frac{V_C \text{ in mV}}{26}\right)}$$

As $V_C$ is increased, the circuit acts as a logarithmic attenuator, yielding a gain reduction of approximately 20 dB for each 60 mV of applied voltage. This same basic gain control stage is used in IF AGC and chroma ACC circuits, as well as for volume, contrast, and chroma controls.

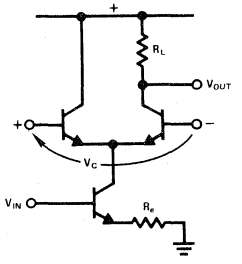


**FIGURE 8**

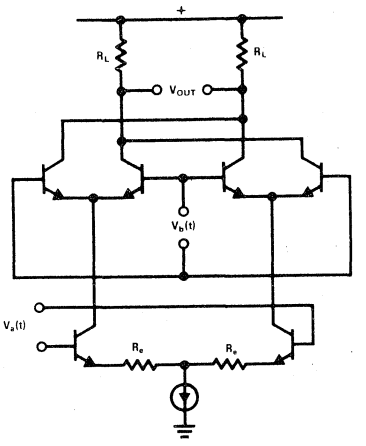


**FIGURE 9**

**Multiplier**

The multiplier is widely used in television IC's for amplitude, phase, and frequency detection. *Figure 9* shows a typical configuration in which the bottom pair is degenerated for linear operation while the top quad is switched. If $V_a(t)$ is an amplitude modulated carrier $F_m(t)\cos \omega t$ and $v_b$ (t) is a square wave of the same frequency $\omega$ and relative phase $\phi$, then the filtered output is given by:

$$V_{OUT} \cong \frac{2}{\pi} \frac{R_L}{R_e} F_m(t) \cos\phi$$

Thus the output depends on the amplitude of $V_a$ and the relative phase $\phi$ between $V_a$ and $V_b$.

If $\phi$ is made 0 degrees so COS $\phi$ is 1, then the multiplier acts as an amplitude detector and can be used to detect the video modulation on the IF carrier. Note that around 0 degrees COS $\phi$ changes very little with phase. To use the multiplier as a phase or frequency detector, $V_a(t)$ is limited to remove amplitude information and $\phi$ is centered at 90 degrees where COS $\phi$ produces the largest change in output for a given change in phase. This operation mode is used for chroma burst phase detectors and sound FM detectors. Both the amplitude and phase sensitive properties of the multiplier are used in chroma demodulators.

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